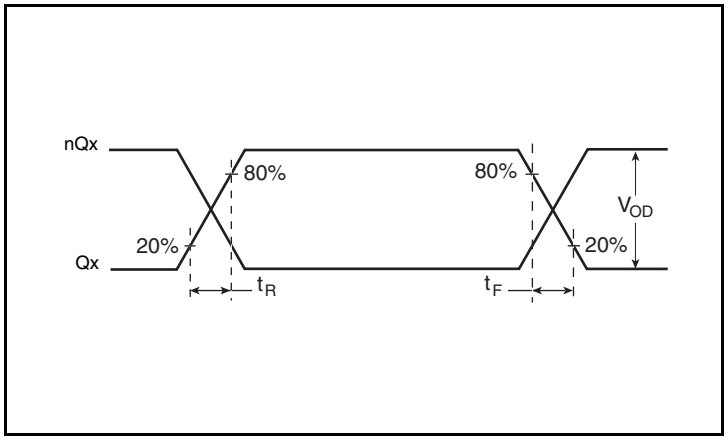
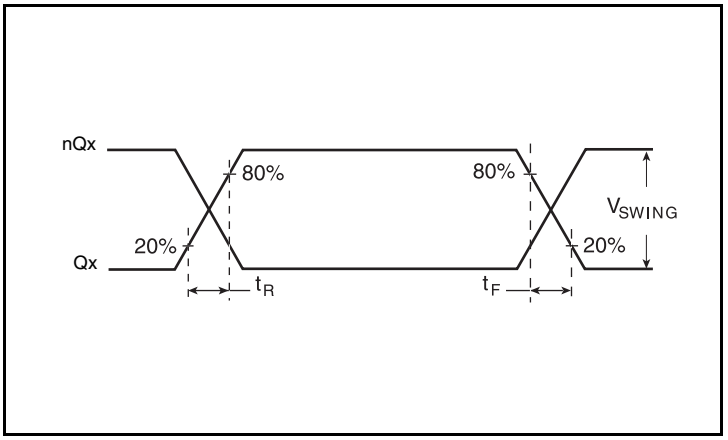
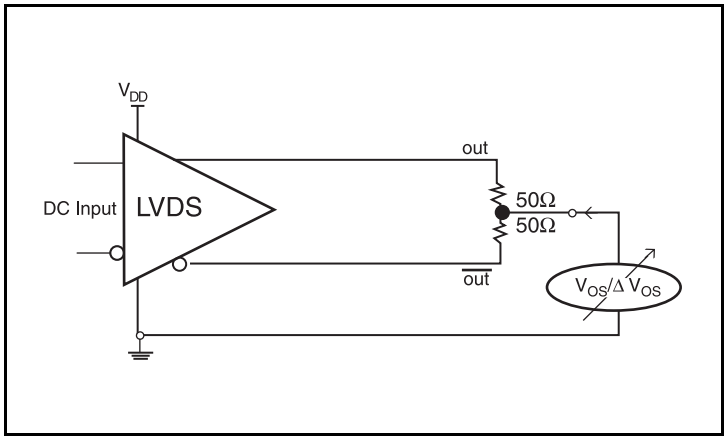
Parameter Measurement Information, continued



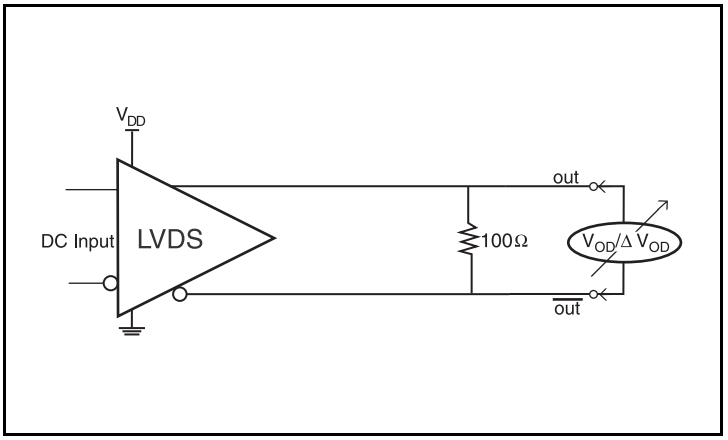
LVDS Output Rise/Fall Time



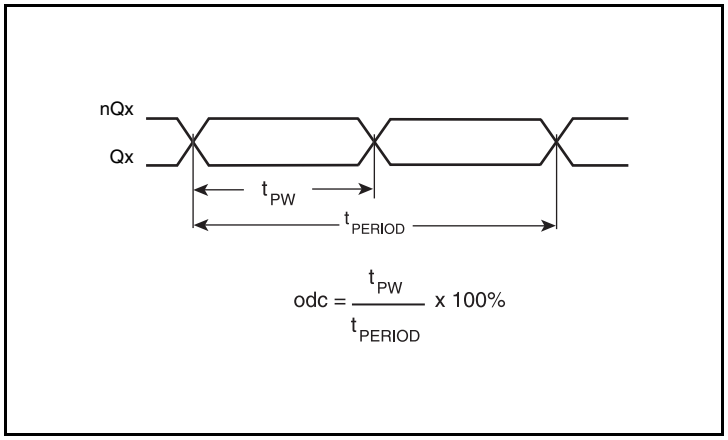
LVPECL Output Rise/Fall Time



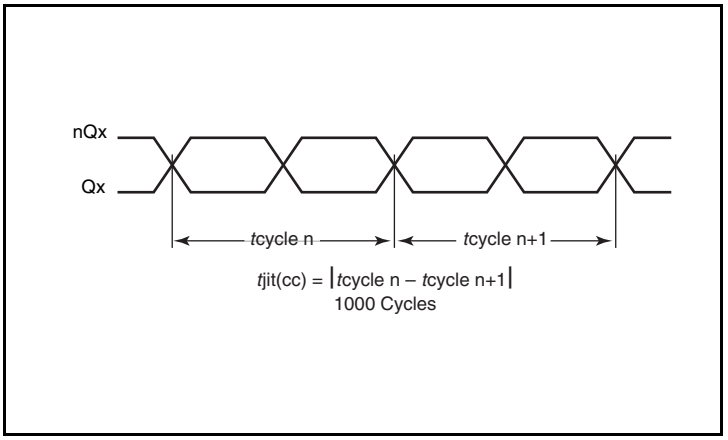
Offset Voltage Setup



Differential Output Voltage Setup



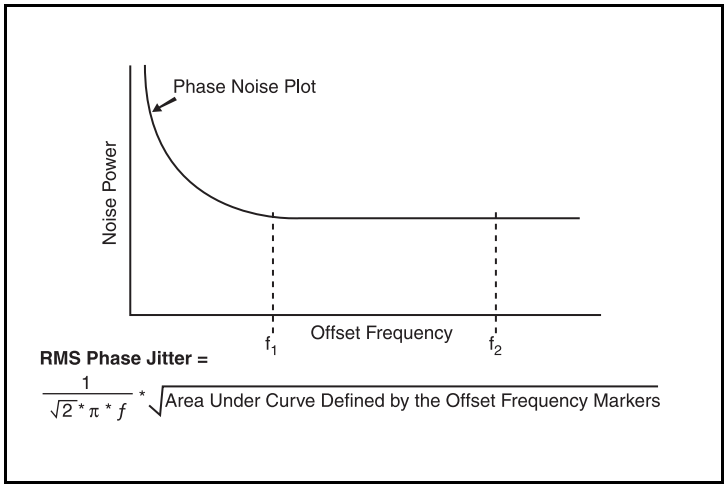
Differential Output Duty Cycle/Output Pulse Width/Period



Cycle-to-Cycle Jitter

Parameter Measurement Information, continued

RMS Phase Jitter



Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLKx/nCLKx Inputs

For applications not requiring the use of either differential input, both CLKx and nCLKx can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground. It is recommended that CLKx, nCLKx be left unconnected in frequency synthesizer mode.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Recommended Values for Low-Bandwidth Mode Loop Filter

External loop filter components are not needed in Frequency Synthesizer or High-Bandwidth modes. In Low-Bandwidth mode, the loop filter structure and components are recommended, refer to the Application Schematic. Please consult IDT if other values are needed.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 4 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

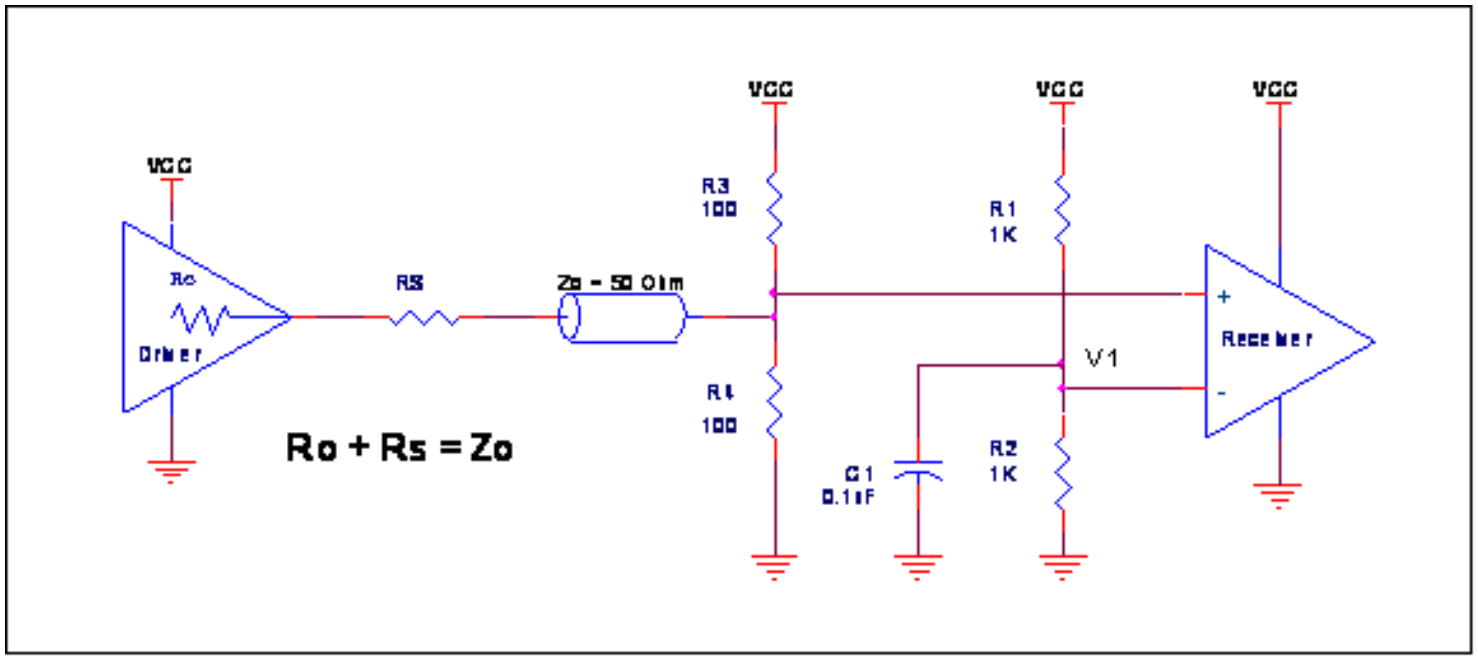


Figure 4. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

The CLKx /nCLKx inputs accept LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 5A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

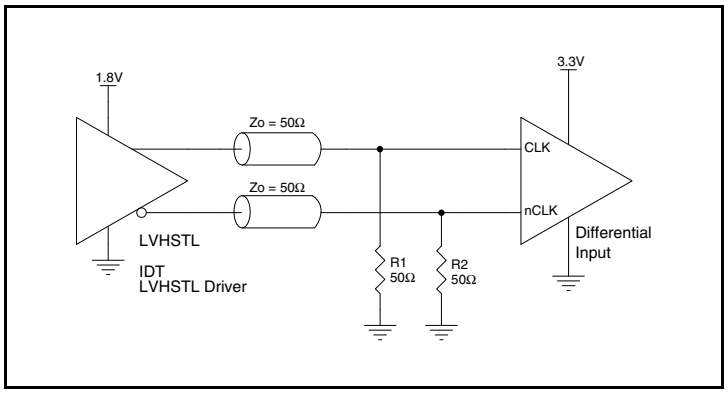


Figure 5A. CLK/nCLK Input driven by an IDT Open Emitter LVHSTL driver

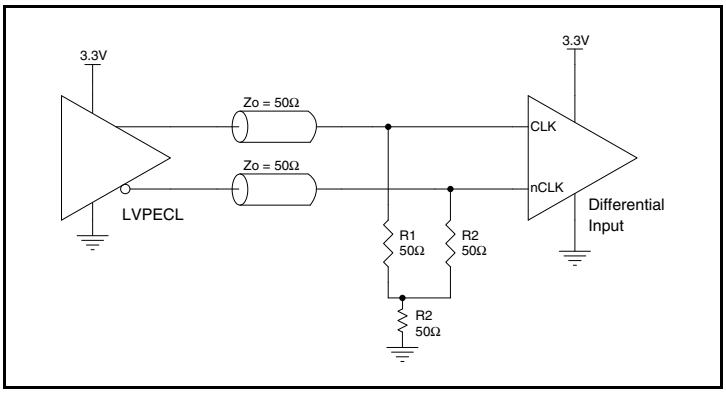


Figure 5B. CLK/nCLK Input driven by a 3.3V LVPECL driver

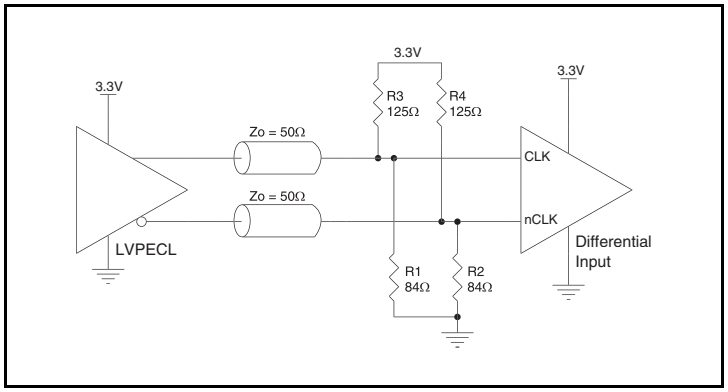


Figure 5C. CLK/nCLK Input driven by a 3.3V LVPECL driver

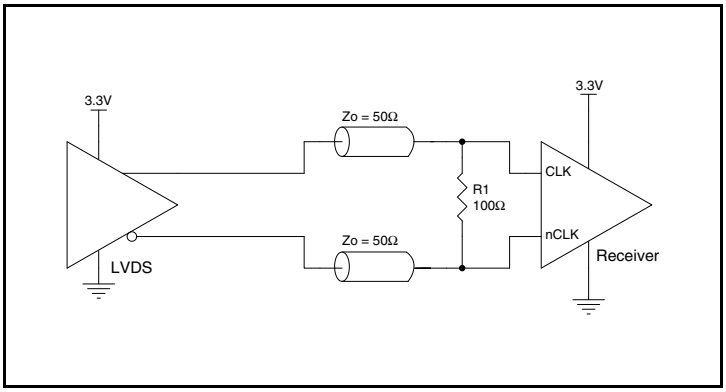


Figure 5D. CLK/nCLK Input driven by a 3.3V LVDS driver

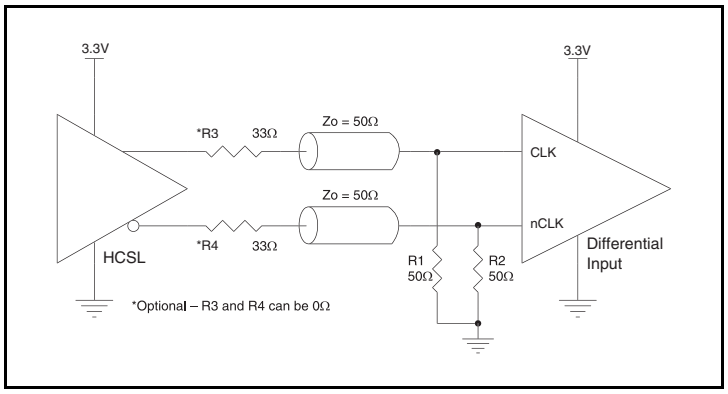


Figure 5E. CLK/nCLK Input driven by a 3.3V HCSL driver

2.5V Differential Clock Input Interface

Each CLKnx /nCLKnx input accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 6A to 6E* show interface examples for the CLKnx /nCLKnx input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 6A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

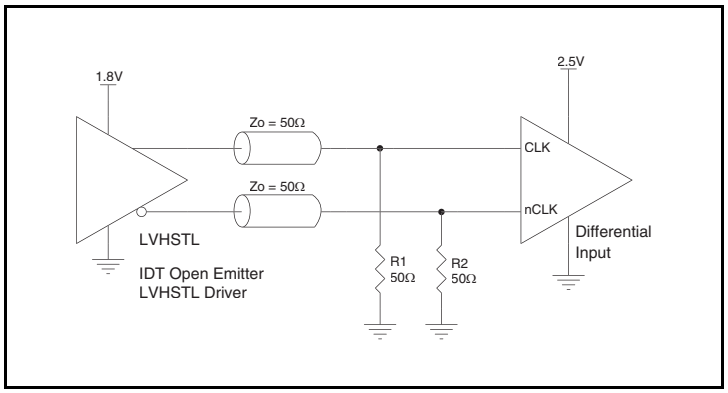


Figure 6A. CLKnx / nCLKnx Input driven by an IDT Open Emitter LVHSTL driver

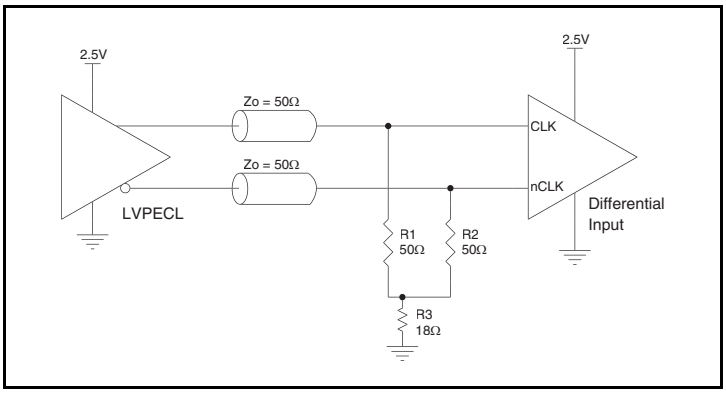


Figure 6B. CLKnx / nCLKnx Input driven by a 2.5V LVPECL driver

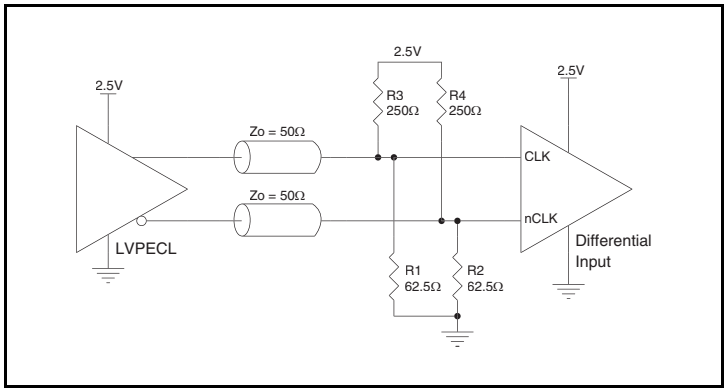


Figure 6C. CLKnx / nCLKnx Input driven by a 2.5V LVPECL driver

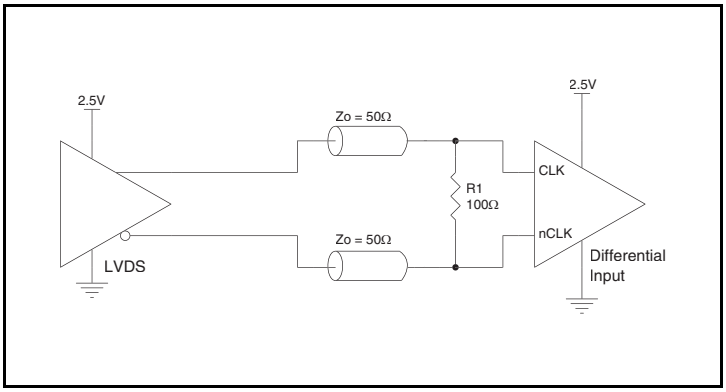


Figure 6D. CLKnx / nCLKnx Input driven by a 2.5V LVDS driver

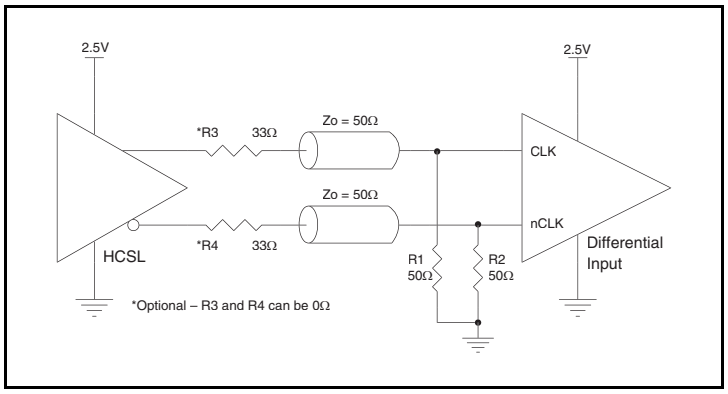


Figure 6E. CLKnx / nCLKnx Input driven by a 2.5V HCSL driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 7A* can be used with either type of output structure. *Figure 7B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

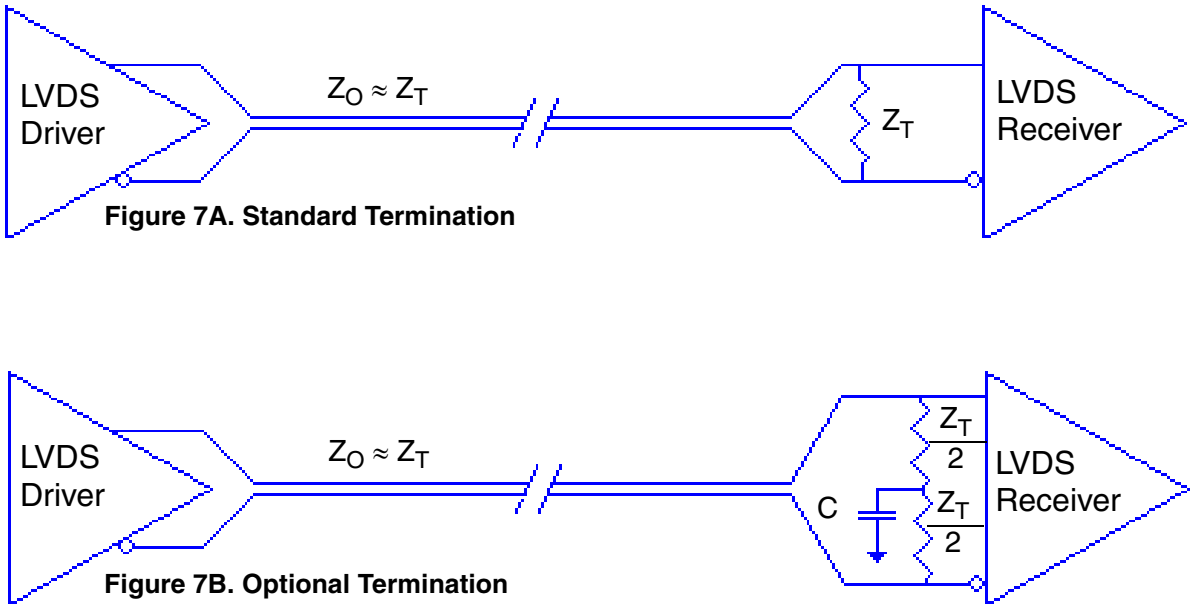


Figure 7A. Standard Termination

Figure 7B. Optional Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 8A and 8B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

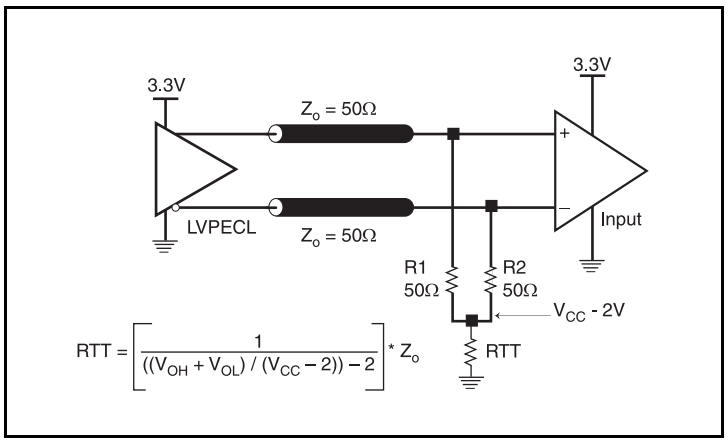


Figure 8A. 3.3V LVPECL Output Termination

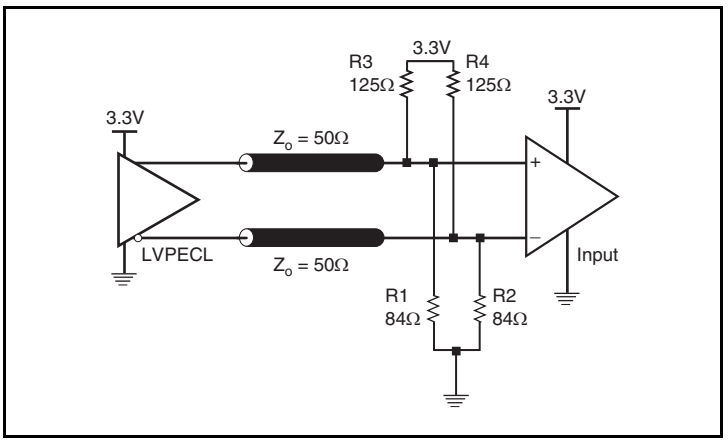


Figure 8B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 9A and *Figure 9B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CCO\_X} - 2V$. For $V_{CCO\_X} = 2.5V$, the $V_{CCO\_X} - 2V$ is very close to ground level. The R3 in Figure 9B can be eliminated and the termination is shown in *Figure 9C.*

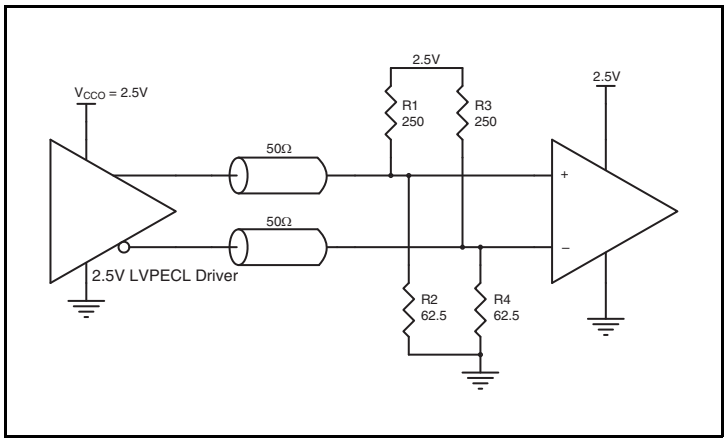


Figure 9A. 2.5V LVPECL Driver Termination Example

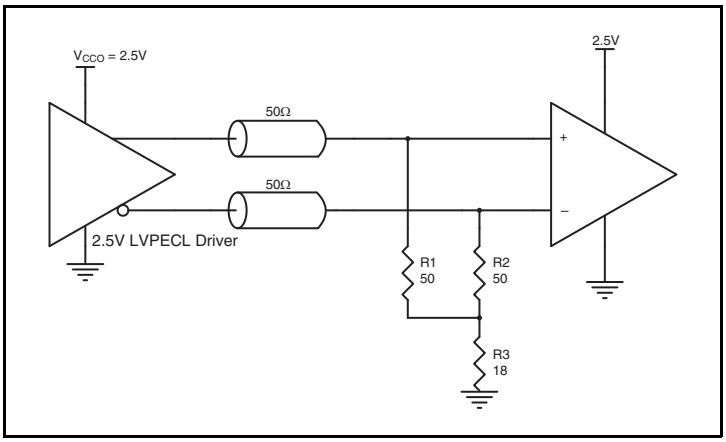


Figure 9B. 2.5V LVPECL Driver Termination Example

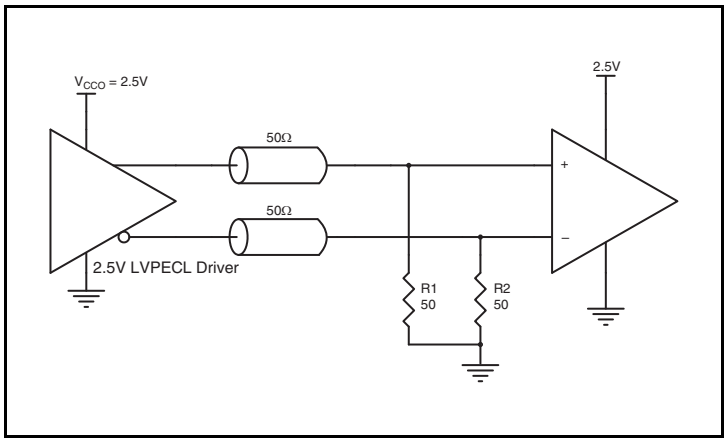


Figure 9C. 2.5V LVPECL Driver Termination Example

Schematic Example

Figure 10 (next page) shows an example IDT8T49N244I application schematic. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that PLL_BYPASS and the CLK_SELx pins are properly set. Input and output terminations shown are intended as examples only and may not match the exact user application. To promote readability in this schematic, only Frequency Translator B and the global pins PLL_BYPASS, REF_CLK and SDATA and SCLK are shown connected.

Frequency Translators A and B are fully independent. Therefore use of Frequency Translator A requires that the power filters shown in the schematic for Frequency Translator B are duplicated for A. However different signal path input and output terminations and loop filters may be used for Frequency Translator A than are shown for Frequency Translator B.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8T49N244I provides separate V_{CC}, V_{CCA_X} and V_{CCO_X} power supplies for each Frequency Translator to isolate any high switching noise from coupling into the internal PLLs.

In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors on the device side of the ferrite beads be placed on the device side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite beads, 10uf and 0.1uF capacitor connected to 2.5V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

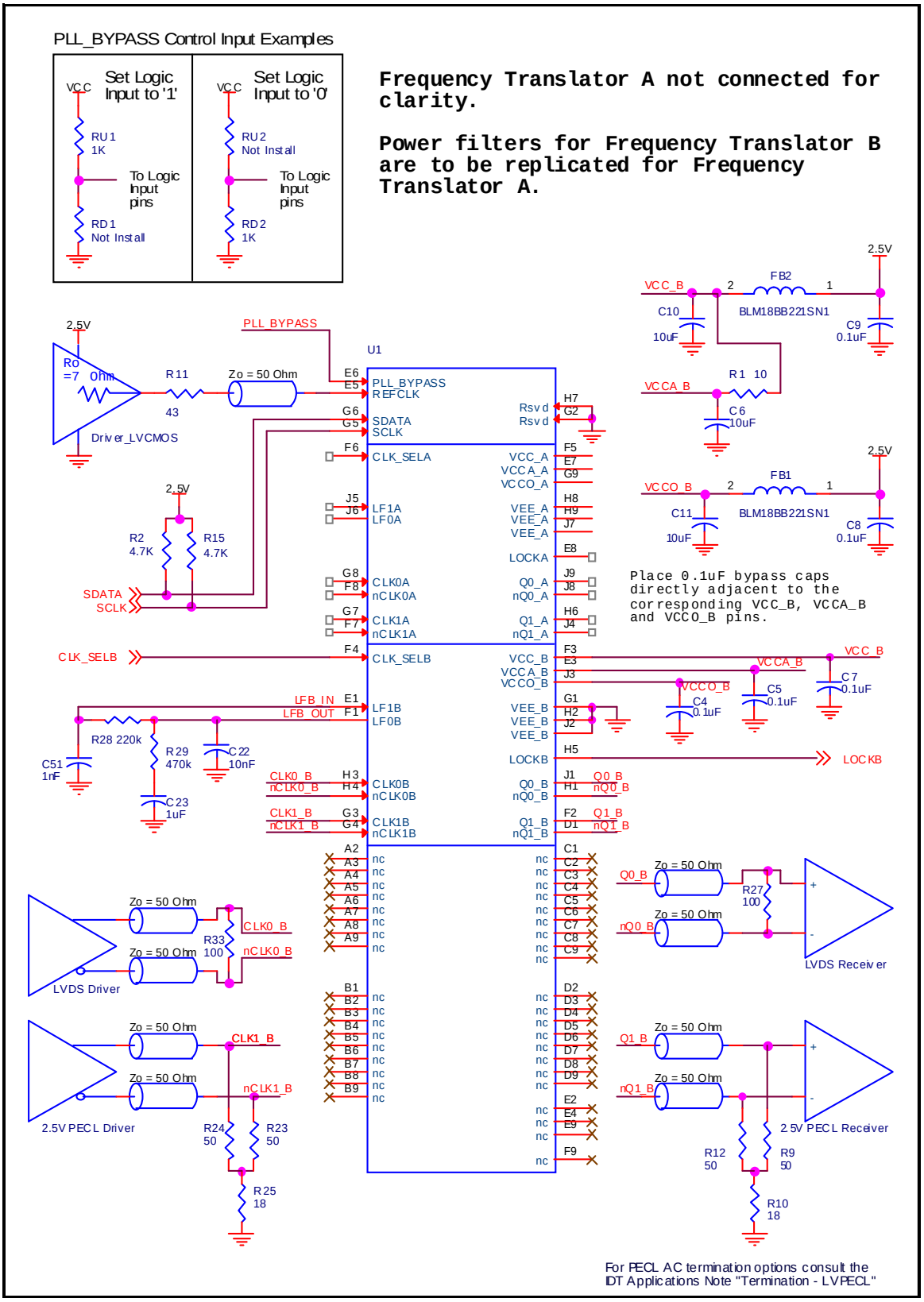


Figure 10. IDT8T49N244I Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N244I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T49N244I is the sum of the core power plus the output power dissipated due to the load.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating output power dissipated due to the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 624mA = **2162.15mW**
- Power (outputs)$_{MAX}$ = **33.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 33.2mW = **132.8mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 2162.15mW + 132.8mW = **2227.56mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 12.4°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 2.228W * 12.4°C/W = 112.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8. θ_{JA} vs. Air FlowTable for an 80-Ball CABGA

θ_{JA} **vs. Air Flow**				
Meters per Second	0	1	2	3
Multi-Layer PCB, NOTE 1	12.4°C/W	11°C/W	10.3°C/W	10°C/W

NOTE 1: θ_{JA} simulation is performed with 8-layers, 8in. x 8in. PCB for the 10x10, 1mm ball pitch BGA package.

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 11.*

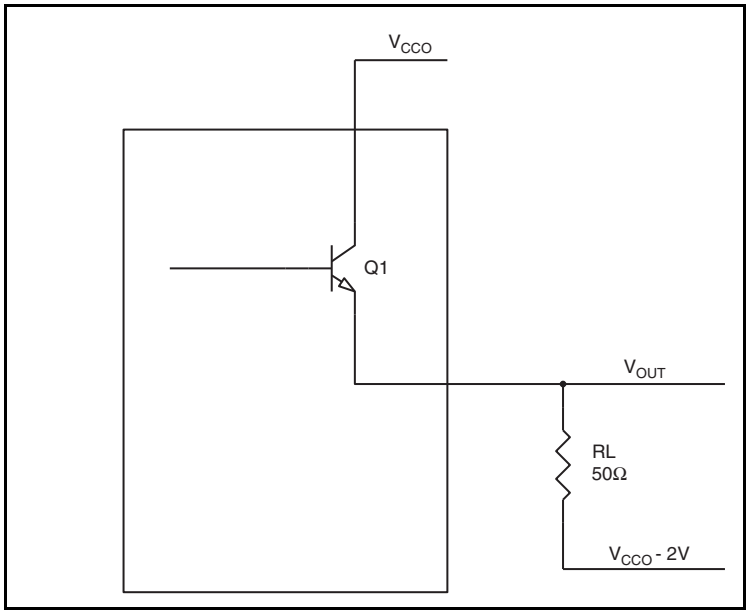


Figure 11. LVPECL Driver Circuit and Termination

To calculate power dissipation per output pair due to the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.7V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.7V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.5V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.5V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – 0.7V)/50Ω] * 0.7V =$ **18.2mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_{L]} * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – 1.5V)/50Ω] * 1.5V =$ **15mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **33.2mW**

LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N244I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T49N244I is the sum of the core power plus the analog power plus the output power dissipated due to loading. The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{CC\_MAX} * (I_{CC\_x\_MAX} + \_) = 3.465V * (526mA + 64mA) =$ **2044.35mW**
- Power $(outputs)_{MAX} = V_{CCO\_X\_MAX} * I_{CCO\_X\_MAX} = 3.465V * 88mA =$ **304.92mW**

Total Power$_{\_MAX}$ = 2044.35mW + 304.92mW = **2349.27mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 12.4°C/W per Table 9 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 2.349W * 12.4°C/W = 114.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 9. θ_{JA} vs. Air FlowTable for an 80-Ball CABGA

θ_{JA} **vs. Air Flow**				
Meters per Second	0	1	2	3
Multi-Layer PCB, NOTE 1	12.4°C/W	11°C/W	10.3°C/W	10°C/W

NOTE 1: θ_{JA} simulation is performed with 8-layers, 8in. x 8in. PCB for the 10x10, 1mm ball pitch BGA package.

Reliability Information

Table 10A. θ_{JA} vs. Air Flow Table for an 80-Ball CABGA

θ_{JA} vs. Air Flow				
Meters per Second	0	1	2	3
Multi-Layer PCB, NOTE 1	12.4°C/W	11°C/W	10.3°C/W	10°C/W

NOTE 1: θ_{JA} simulation is performed with 8-layers, 8in. x 8in. PCB for the 10x10, 1mm ball pitch BGA package.

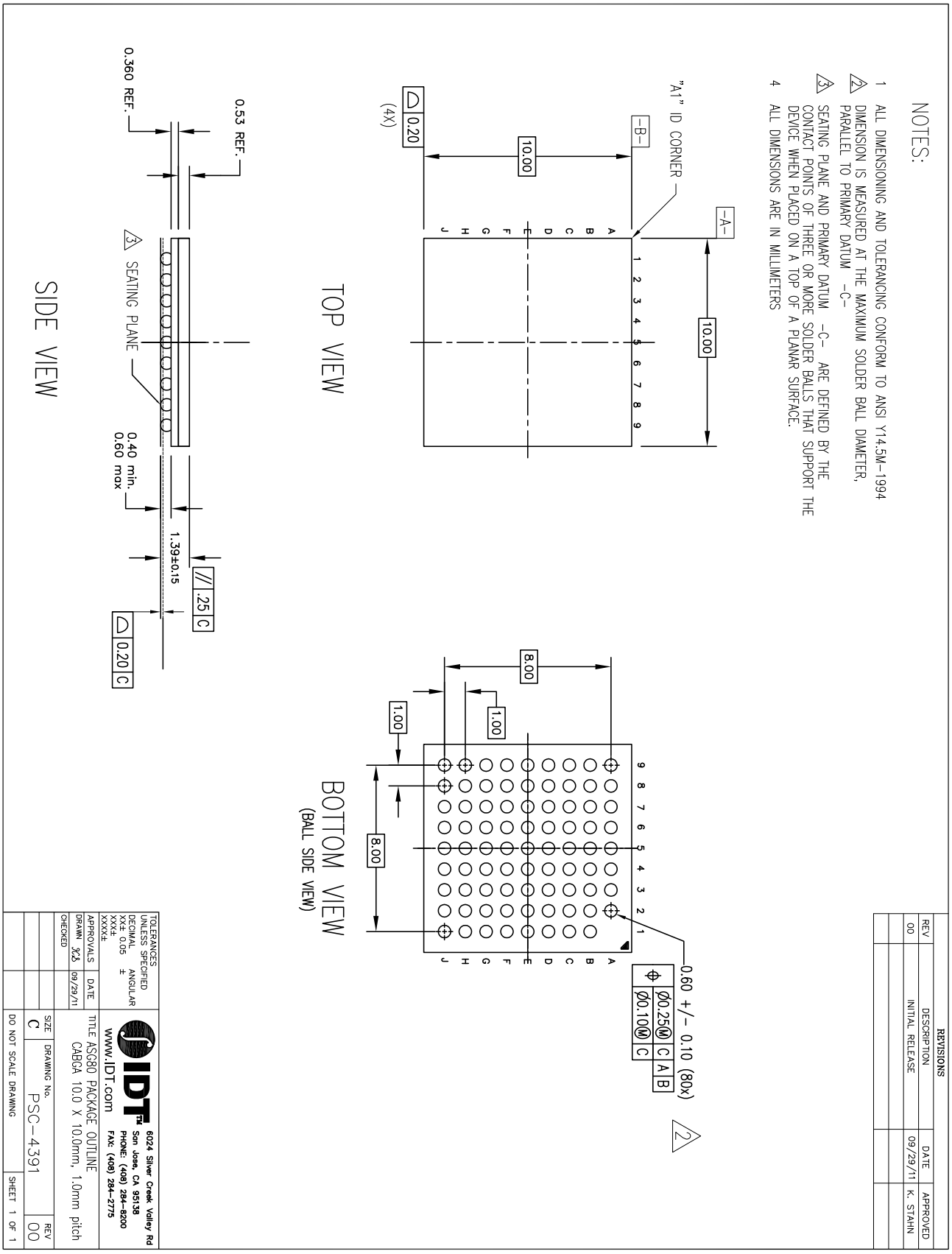
Table 10B. θ_{JC} Table for an 80-Ball CABGA

θ_{JC}	
Meters per Second	0
Multi-Layer PCB, NOTE 1	12.5°C/W

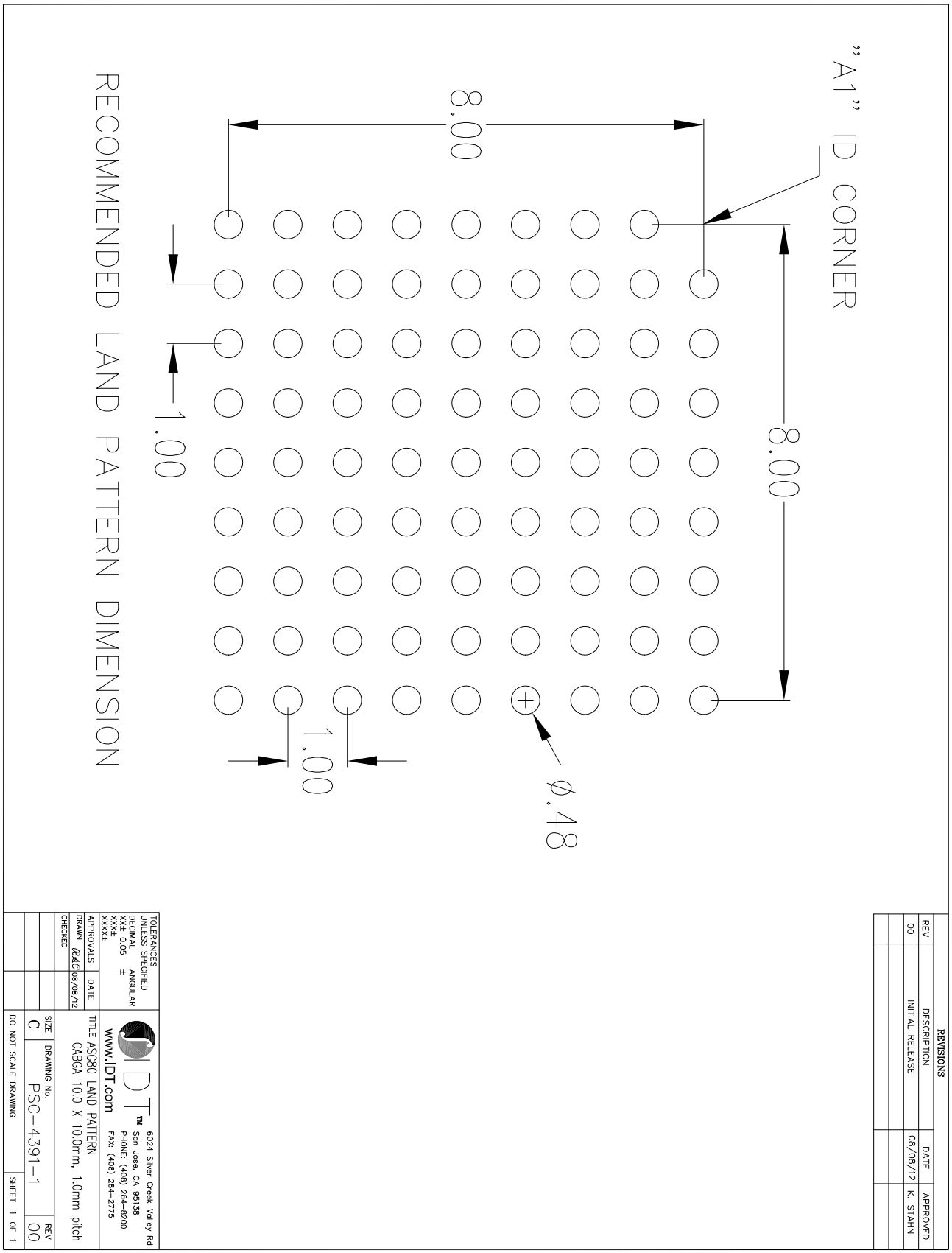
Transistor Count

The transistor count for IDT8T49N244I is: 101,286

80-Ball CABGA (AS) Package Outline and Package Dimensions



80-Ball CABGA (AS) Land Pattern



Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N244A-dddASGI	IDT8T49N244A-dddASGI	“Lead-Free” Plastic 80-Ball CABGA	Tray	-40°C to +85°C
8T49N244A-dddASGI8	IDT8T49N244A-dddASGI	“Lead-Free” Plastic 80-Ball CABGA	Tape & Reel	-40°C to +85°C

NOTE: For the specific -ddd order codes, refer to *FemtoClock NG Universal Frequency Translator Ordering Product Information* document.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T2 T5F	4 16	Pin Characteristics Table - added PLL_BYPASS to $R_{Pulldown}$ row. LVCMOS DC Characteristics Table - added NOTE 1 to I_{IH}, I_{IL}.	2/15/13
A	T4E	11	Corrected typo: M_INTx[8:0] to M_INTx[7:0]	6/28/13