FemtoClock® Crystal - to - 3.3 V, 2.5 LVPECL Frequencey Synthesizer

IDT8R43002I-01

DATA SHEET

General Description

The IDT8R43002I-01 is a two output LVPECL synthesizer optimized to generate Ethernet reference clock frequencies. Using a 25MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the two frequency select pins (F_SEL[1:0]): 156.25MHz, 125MHz, and 62.5MHz. The IDT8R43002I-01 uses IDT's FemtoClock® low phase noise VCO technology and can achieve 1ps or lower typical RMS phase jitter, easily meeting Ethernet jitter requirements. The IDT8R43002I-01 is packaged in a small 20-pin TSSOP package.

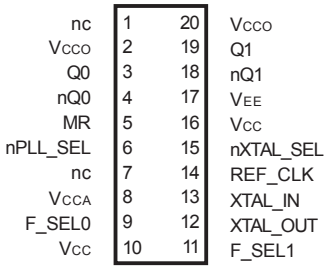
Features

- Two 3.3V or 2.5V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 156.25MHz, 125MHz and 62.5MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz-20MHz): 0.55ps (typical)
- Output skew: 30ps (maximum)
- Supply Voltage Modes
  Core/Outputs
  3.3/3.3
  2.5/2.5
- -40°C to 85°C ambient operating temperature
- Available in lead-free RoHS-compliant packages

Table 1. Frequency Select Function Table

Inputs				Output Frequency (25MHz Ref.)
F_SEL1	F_SEL0	M Divider Value	N Divider Value	
0	0	25	4	156.25 (default)
0	1	25	5	125
1	0	25	10	62.5
1	1	25	5	125

Pin Assignment



IDT8R43002I-01
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm
package body
G Package
Top View

Block Diagram

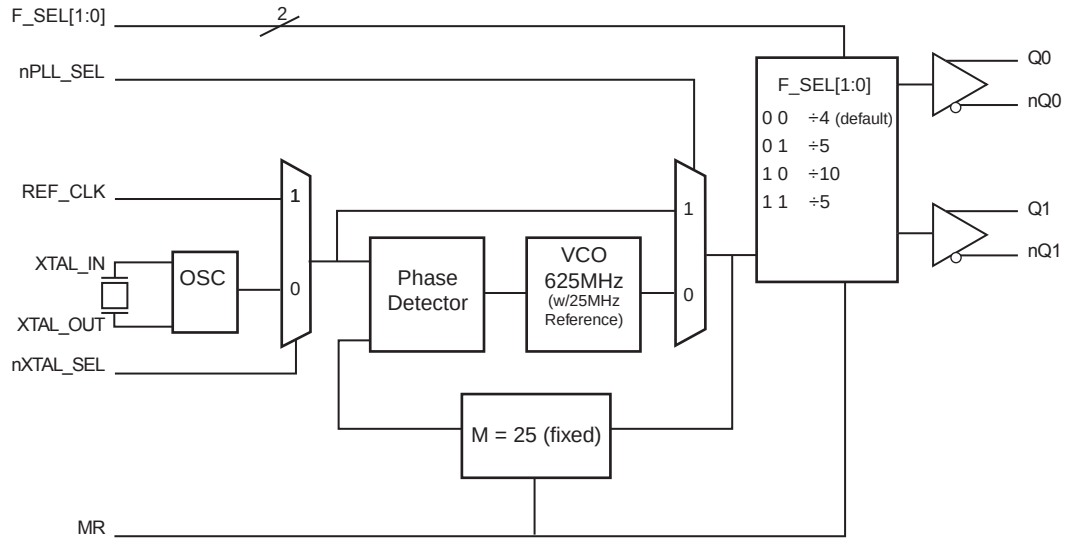


TABLE 2. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 7	nc	Unused		No connect.
2, 20	V_{CCO}	Power		Output supply pins.
3, 4	Q0, nQ0	Ouput		Differential output pair. LVPECL interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	nPLL_SEL	Input	Pulldown	Determines whether synthesizer is in PLL or bypass mode. LVCMOS/LVTTL interface levels.
8	V_{CCA}	Power		Analog supply pin.
9, 11	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
10, 16	V_{CC}	Power		Core supply pin.
12, 13	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
14	REF_CLK	Input	Pulldown	LVCMOS/LVTTL reference clock input.
15	nXTAL_SEL	Input	Pulldown	Selects between crystal or REF_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects REF_CLK when HIGH. LVCMOS/LVTTL interface levels.
17	V_{EE}	Power		Negative supply pins.
18, 19	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 3. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.97	3.3	3.63	V
V_{CCA}	Analog Supply Voltage		2.97	3.3	3.63	V
V_{CCO}	Output Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current				130	mA
I_{CCA}	Analog Supply Current				13	mA

Table 4B. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				115	mA
I_{CCA}	Analog Supply Current				12	mA

Table 4C. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±10% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	REF_CLK, MR, nPLL_SEL, nXTAL_SEL	$V_{CC} = V_{IN}$ = 3.63V or 2.625V			150	µA
I_{IL}	Input Low Current	REF_CLK, MR, nPLL_SEL, nXTAL_SEL	$V_{CC} = V_{IN}$ = 3.63V or 2.625V	-5			µA

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±10% OR 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		22.4	25	27.2	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±10%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	140		170	MHz
		F_SEL[1:0] = 01	112		136	MHz
		F_SEL[1:0] = 10	56		68	MHz
*t*sk(o)	Output Skew; NOTE 1, 2				30	ps
*t*jit(Ø)	RMS Phase Jitter; NOTE 2, 3	156.25MHz, (1.875MHz - 20MHz)		0.55		ps
		125MHz, (1.875MHz - 20MHz)		0.60		ps
		62.5MHz, (1.875MHz - 20MHz)		0.70		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	350		650	ps
odc	Output Duty Cycle		48		52	%

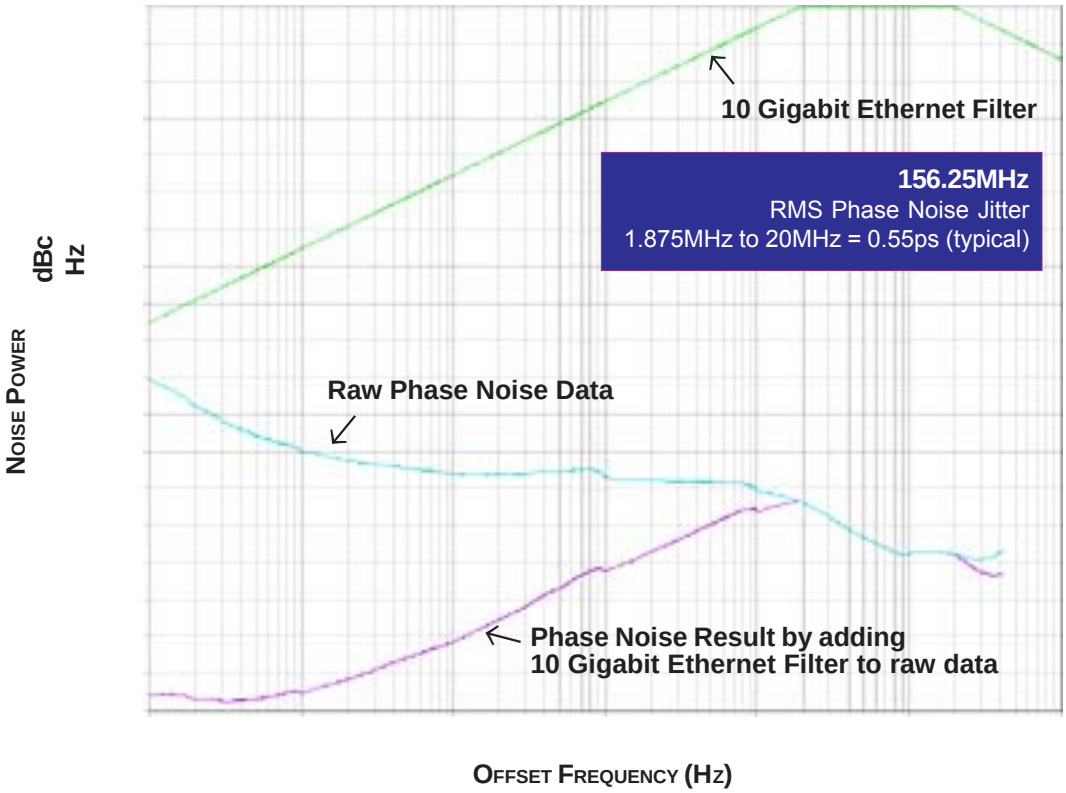
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Measured using crystal input.

TABLE 6B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 2.5V±5%, T_A = -40°C TO 85°C

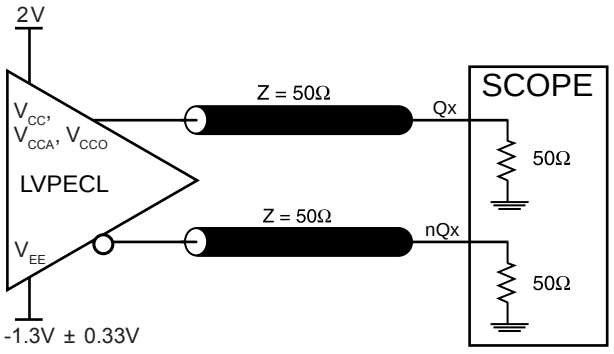
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	140		170	MHz
		F_SEL[1:0] = 01	112		136	MHz
		F_SEL[1:0] = 10	56		68	MHz
*t*sk(o)	Output Skew; NOTE 1, 2				30	ps
*t*jit(Ø)	RMS Phase Jitter; NOTE 2, 3	156.25MHz, (1.875MHz - 20MHz)		0.55		ps
		125MHz, (1.875MHz - 20MHz)		0.60		ps
		62.5MHz, (1.875MHz - 20MHz)		0.74		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	350		650	ps
odc	Output Duty Cycle		48		52	%

For Notes, see Table 5A above.

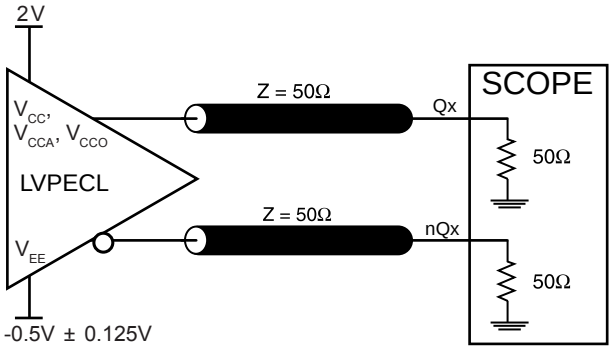
TYPICAL PHASE NOISE AT 156.25MHZ @ 3.3V



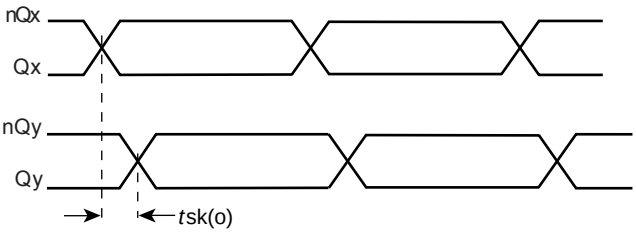
PARAMETER MEASUREMENT INFORMATION



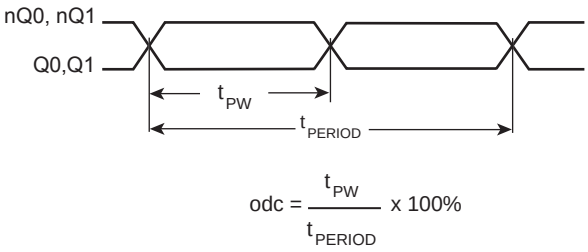
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



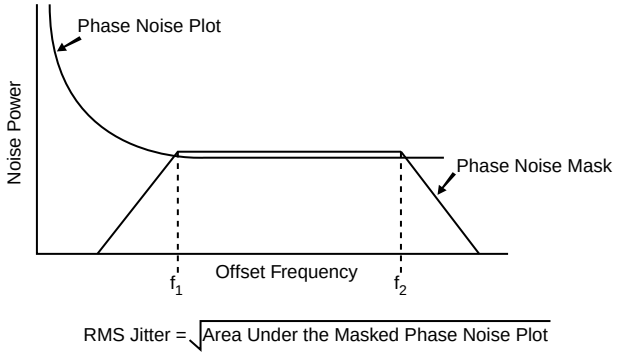
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



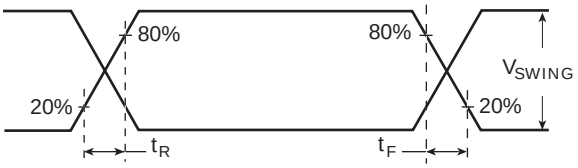
OUTPUT SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



RMS PHASE JITTER



OUTPUT RISE/FALL TIME

APPLICATIONS INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT:
For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 1A and1B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

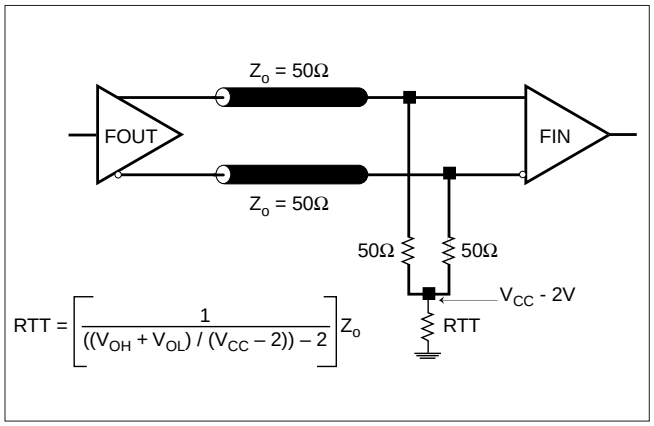


FIGURE 1A. LVPECL OUTPUT TERMINATION

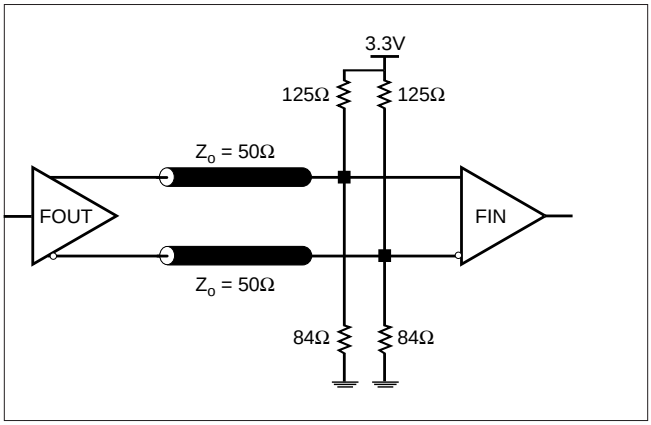


FIGURE 1B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 2A and *Figure 2B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} - 2V. For V_{CCO} = 2.5V, the V_{CCO} - 2V is very close to ground level. The R3 in Figure 2B can be eliminated and the termination is shown in *Figure 2C.*

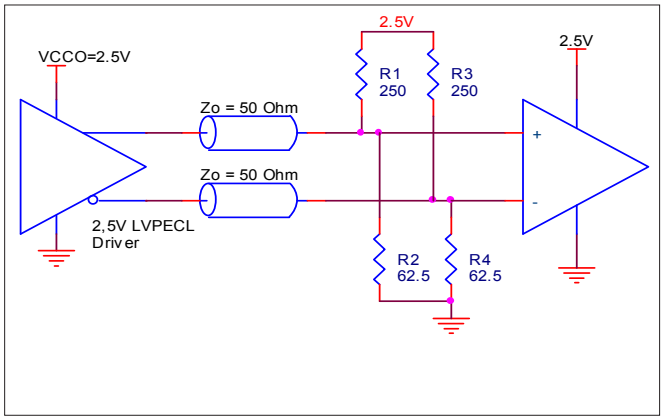


FIGURE 2A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

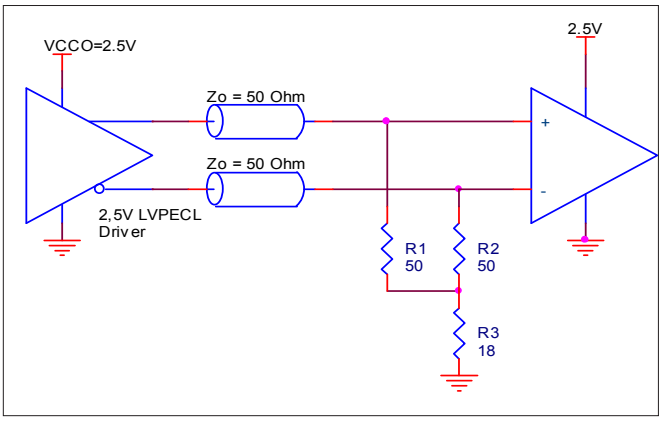


FIGURE 2B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

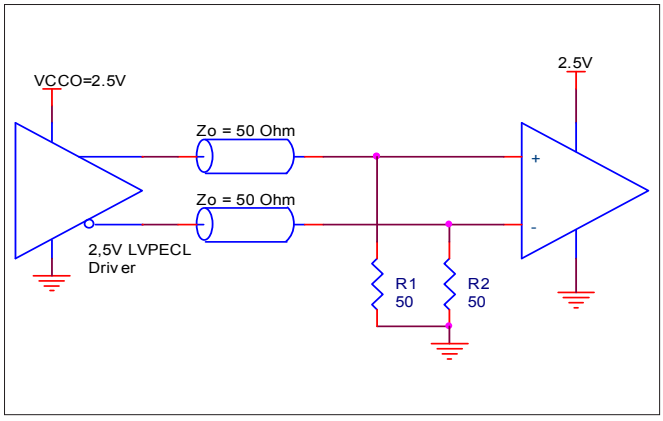


FIGURE 2C. 2.5V LVPECL TERMINATION EXAMPLE

APPLICATION SCHEMATIC EXAMPLE

Figure 3 shows an example IDT8R43002I-01 application schematic. Input and output terminations shown are intended as examples only and may not represent the exact user configuration. Resistor R10 represents an external padding resistor so that the LVCMOS driver presents a 50 ohm source impedance to the transmission line driving REF_CLK. Load caps C7 and C8 are required for frequency accuracy, but these may be adjusted for different board layouts. If different crystal types are used, please consult IDT for recommendations.

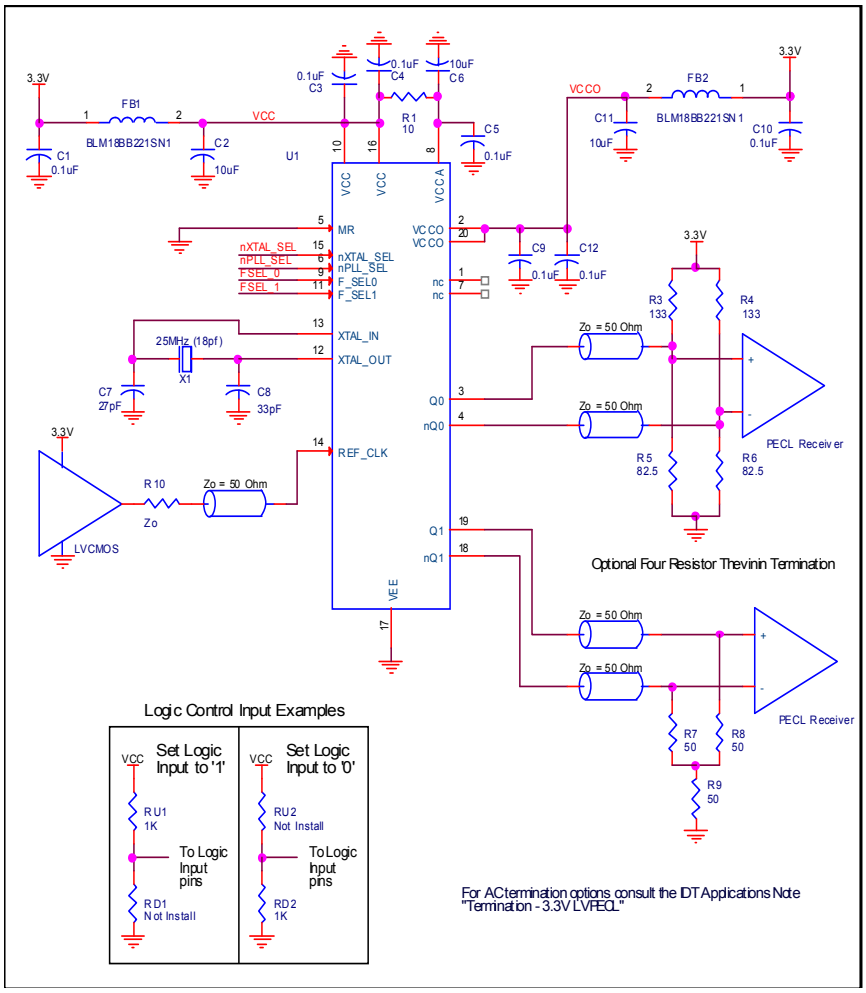


FIGURE 3. IDT8R43002I-01 SCHEMATIC EXAMPLE

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8R43002i-01 provides separate V_{CC}, V_{CCO} and V_{CCA} power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors be placed on the device side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite bead, 10uf and 0.1uF capacitors connected to 3.3V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. If AC coupling for PECL levels is required to the CLK/nCLK and/or Q0 and Q1 outputs, please refer to the IDT application note, “Termination – 3.3V PECL”

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the IDT8R43002I-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8R43002I-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 10% = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.63V * 130mA = **471.9mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

  Total Power$_{_MAX}$ (3.63V, with all outputs switching) = 471.9mW + 60mW = **531.9mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.532W * 66.6°C/W = 120.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

θ_{JA} by Velocity (Linear Feet per Minute)

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 20-PIN TSSOP, FORCED CONVECTION

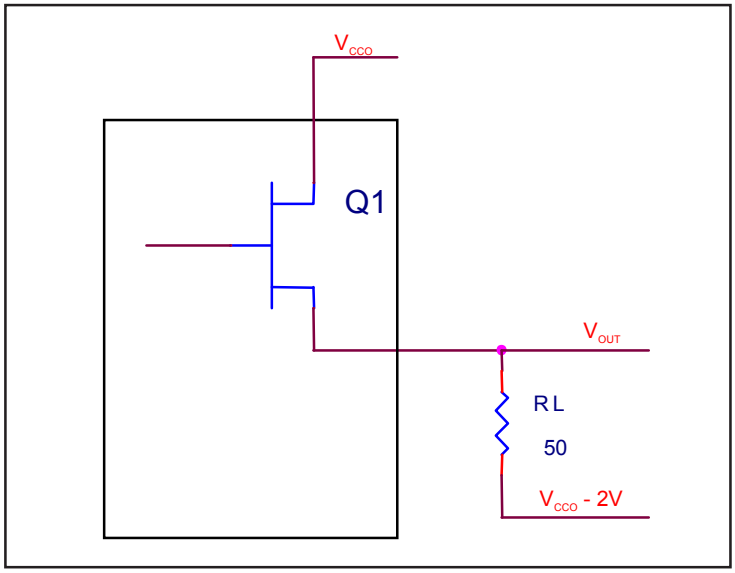
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8R43002I-01 is: 2955

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

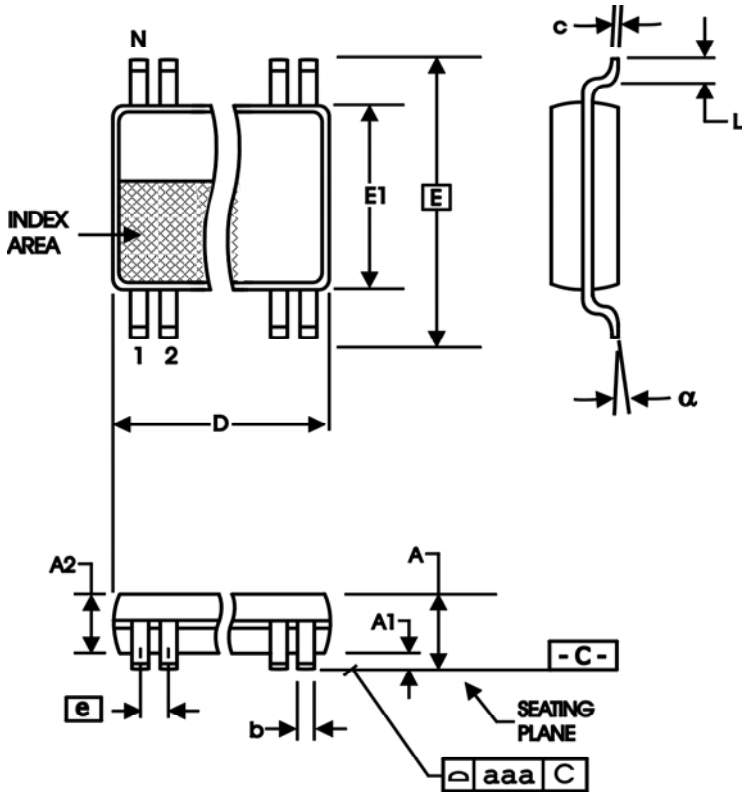


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8R43002A-01PGGI	IDT8R43002A01PGGI	20 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
8R43002A-01PGGI8	IDT8R43002A01PGGI	20 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with a "G" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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