LVPECL Dual-Frequency Programmable VCXO

IDT8N3DV85

DATASHEET

General Description

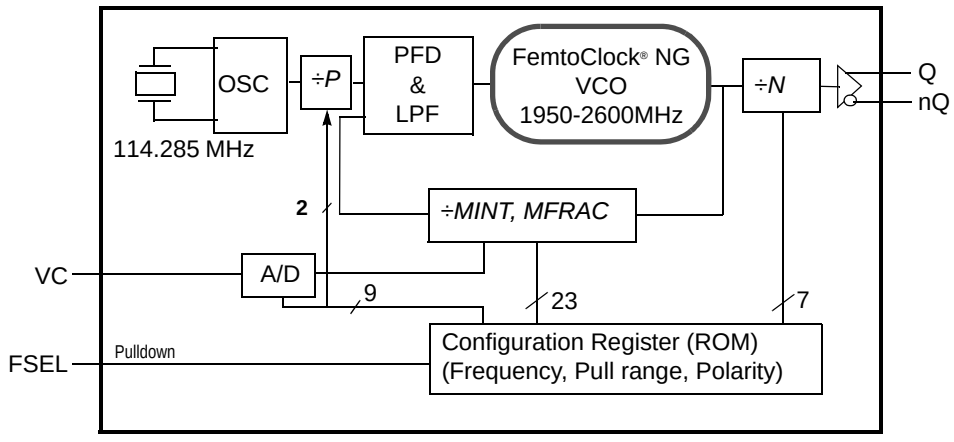
The IDT8N3DV85 is a LVPECL Dual-Frequency Programmable VCXO with very flexible frequency and pull-range programming capabilities. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance. The device accepts 2.5V or 3.3V supply and is packaged in a small, lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package.

The device can be factory-programmed to any two frequencies in the range of 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz to the very high degree of frequency precision of 218Hz or better. The output frequency is selected by the FSEL pin. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

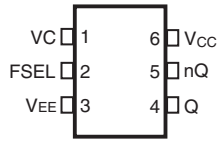
Features

- Fourth Generation FemtoClock® NG technology
- Programmable clock output frequency from 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz
- Two factory-programmed output frequencies
- VCO frequency programming resolution is 218Hz and better
- Factory-programmable VCXO pull range and control voltage polarity
- VCXO pull range programmable from typical ±12.5 to ±787.5ppm
- One 2.5V or 3.3V LVPECL clock output
- FSEL control input for frequency selection, LVCMOS/LVTTL compatible
- RMS phase jitter @ 622.08MHz (12kHz - 20MHz):0.46ps (typical)
- RMS phase jitter @ 622.08MHz (50kHz - 80MHz): 0.47ps (typical)
- 2.5V or 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package

Block Diagram



Pin Assignment



IDT8N3DV85
6-lead ceramic 5mm x 7mm x 1.55mm package body
CD Package
Top View

Pin Description and Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	VC	Input		VCXO Control Voltage input.
2	FSEL	Input	Pulldown	Frequency select pin. See Table 3A for function. LVCMOS/LVTTL interface levels.
3	V_{EE}	Power		Negative power supply.
4, 5	Q, nQ	Output		Differential clock output. LVPECL interface levels.
6	V_{CC}	Power		Positive power supply.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	FSEL			5.5		pF
		VC			10		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				50		kΩ

Function Tables

Table 3A. Frequency Selection

Input FSEL	Operation
0 (default)	Frequency 0
1	Frequency 1

NOTE: Frequency 0 and 1 are factory-programmed by IDT. Any frequency combination within the available frequency range can be ordered. For order information, see *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document. .

Table 3B. Output Frequency Range

15.476MHz to 866.67MHz
975MHz to 1,300MHz

NOTE: Supported output frequency range. The output frequency can be programmed to any frequency in this range and to a precision of 218Hz or better.

Principles of Operation

The block diagram consists of the internal 3rd overtone crystal and oscillator which provide the reference clock f_{XTAL} of 114.285MHz. The PLL includes the FemtoClock® VCO along with the Pre-divider (*P*), the feedback divider (*M*) and the post divider (*N*). The *P*, *M*, and *N* dividers determine the output frequency based on the f_{XTAL} reference. The feedback divider is fractional supporting a huge number of output frequencies. Internal registers are used to hold up to two different factory pre-set configuration settings. The configuration is selected via the FSEL pin. Changing the FSEL control results in an immediate change of the output frequency to the selected register values. The *P*, *M*, and *N* frequency configurations support an output frequency range 15.476MHz to 866.67MHz and 975MHz to 1,300MHz.

The devices use the fractional feedback divider with a delta-sigma modulator for noise shaping and robust frequency synthesis capability. The relatively high reference frequency minimizes phase noise generated by frequency multiplication and allows more efficient shaping of noise by the delta-sigma modulator. The output frequency is determined by the 2-bit pre-divider (*P*), the feedback divider (M) and the 7-bit post divider (*N*). The feedback divider (*M*) consists of both a 7-bit integer portion (*MINT*) and an 18-bit fractional portion (*MFRAC*) and provides the means for high-resolution frequency generation. The output frequency f_{OUT} is calculated by:

$$f_{OUT} = f_{XTAL} \cdot \frac{1}{P \cdot N} \cdot \left[MINT + \frac{MFRAC + 0.5}{2^{18}} \right] \quad (1)$$

Table 3A. Frequency Selection

Input	
FSEL	**Selects**
0 (default)	Frequency 0
1	Frequency 1

Frequency Configuration

An order code is assigned to each frequency configuration and the VCXO pull-range programmed by the factory (default frequencies). For more information on the available default frequencies and order codes, please see the Ordering Information Section in this document. For available order codes, see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.

For more information on programming capabilities of the device for custom frequency and pull-range configurations, see the *FemtoClock NG Ceramic 5x7 Module Programming Guide.*

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.71V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	49.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			130	160	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			120	155	mA

Table 4C. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4D. LVPECL DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4E. LVCMOS/LVTTL DC Characteristic, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = V_{IN} = 3.465V	-0.3		0.7	V
			V_{CC} = V_{IN} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	FSEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	FSEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA

AC Electrical Characteristics

Table 5A. AC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Q, nQ		15.476		866.67	MHz
			975		1,300	MHz
f_I	Initial Accuracy	Measured @ 25°C, $V_C = V_{CC}/2$			±10	ppm
f_S	Temperature Stability	Option code = A or B			±100	ppm
		Option code = E or F			±50	ppm
		Option code = K or L			±20	ppm
f_A	Aging	Frequency drift over 10 year life			±3	ppm
		Frequency drift over 15 year life			±5	ppm
f_T	Total Stability	Option code A, B (10 year life)			±113	ppm
		Option code E, F (10 year life)			±63	ppm
		Option code K, L (10 year life)			±33	ppm
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1	622.08MHz		6	12	ps
*t*jit(per)	RMS Period Jitter			2	3	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	622.08MHz, Integration Range: 12kHz - 20MHz		0.46	0.71	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	622.08MHz, Integration Range: 50kHz - 80MHz		0.47	0.72	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2,3,4 f_{XTAL} = 114.285MHz	500MHz < f_{OUT} ≤ 1300MHz		0.44	0.77	ps
		125MHz < f_{OUT} ≤ 500MHz		0.52	0.90	ps
		15MHz ≤ f_{OUT} ≤ 125MHz		0.74	1.2	ps
Φ_N(100)	Single-side band phase noise, 100Hz from Carrier	622.08MHz		-68		dBc/Hz
Φ_N(1k)	Single-side band phase noise, 1kHz from Carrier	622.08MHz		-89		dBc/Hz
Φ_N(10k)	Single-side band phase noise, 10kHz from Carrier	622.08MHz		-113		dBc/Hz
Φ_N(100k)	Single-side band phase noise, 100kHz from Carrier	622.08MHz		-118		dBc/Hz
Φ_N(1M)	Single-side band phase noise, 1MHz from Carrier	622.08MHz		-127		dBc/Hz
Φ_N(10M)	Single-side band phase noise, 10MHz from Carrier	622.08MHz		-137		dBc/Hz
t_R / t_F	Output Rise/Fall Time	20% to 80%	80		500	ps
odc	Output Duty Cycle		45		55	%
PSNR	Power Supply Noise Rejection	50mV sinusoidal Noise 1kHz - 50MHz		-71.2		dBc
$t_{STARTUP}$	Device Startup Time after Power-up				10	ms
t_{SET}	Output Frequency Settling Time after FSEL value is changed				1	ms

Notes continued on next page.

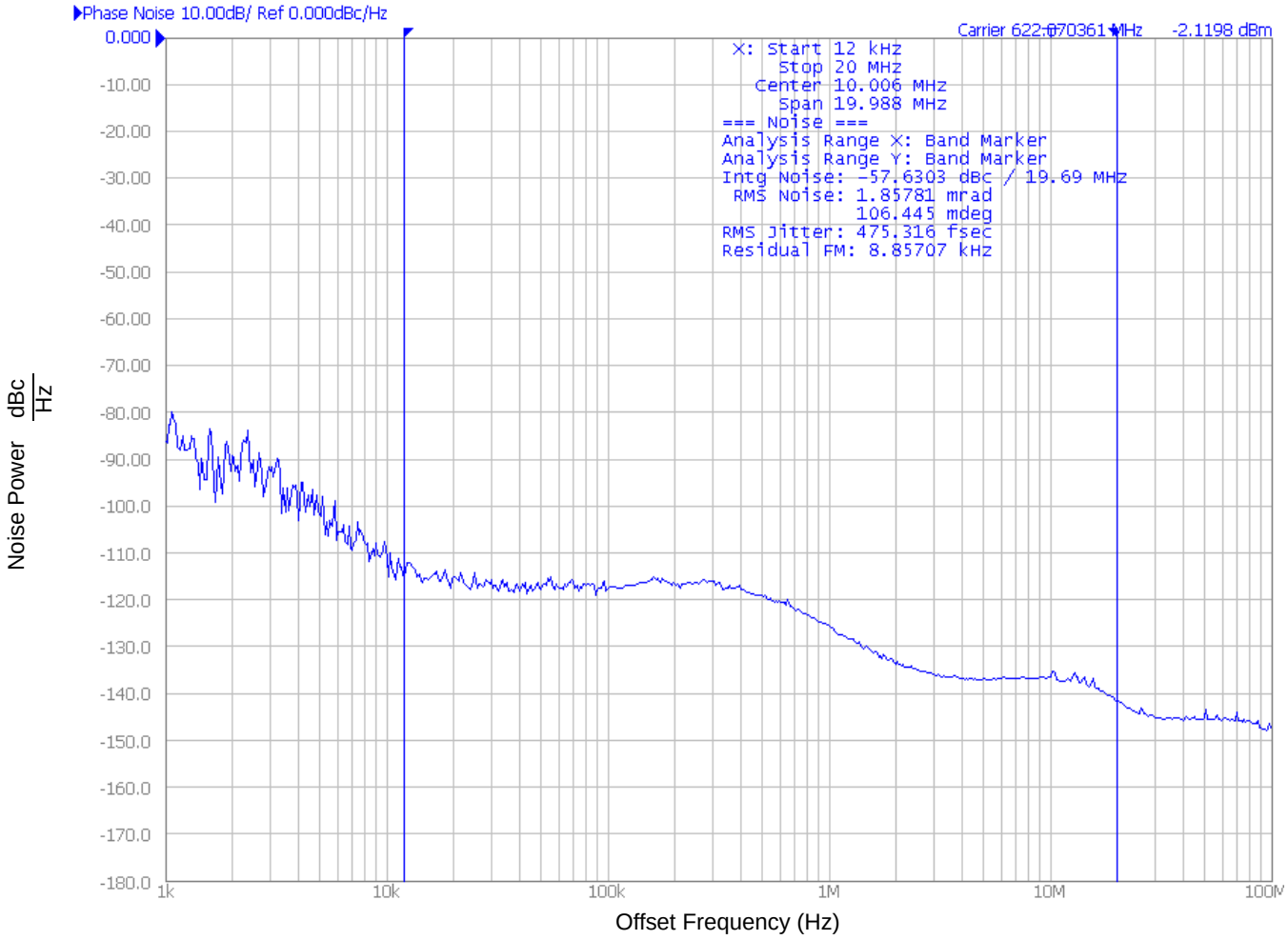
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: XTAL parameters (initial accuracy, temperature stability, aging and total stability) are guaranteed by manufacturing.
NOTE: Characterized with $V_C = V_{CC}/2$
NOTE 1: This parameter is defined in accordance with JEDEC standard 65.
NOTE 2: Refer to the phase noise plot.
NOTE 3: Please see the FemtoClock Ceramic 5x7 Modules Programming Guide for more information on PLL feedback modes and the optimum configuration for phase noise.

Table 5B. VCXO Control Voltage Input (V_C) Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

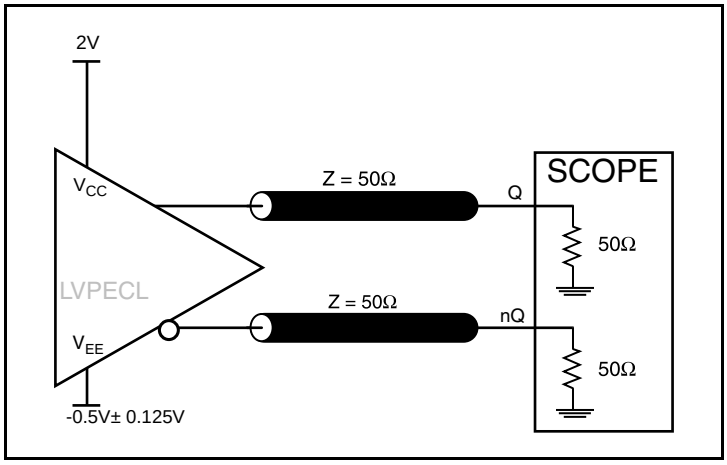
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
K_V	Oscillator Gain, NOTE 1, 2, 3	V_{CC} = 3.3V	7.57		477.27	ppm/V
	Oscillator Gain, NOTE 1, 2, 3	V_{CC} = 2.5V	10		630	ppm/V
L_{VC}	Control Voltage Linearity; NOTE 4	BSL Variation	-5	±0.4	+5	%
BW	Modulation Bandwidth			100		kHz
Z_{VC}	VC Input Impedance			500		kΩ
VC_{NOM}	Nominal Control Voltage			$V_{CC}/2$		V
V_C	Control Voltage Tuning Range; NOTE 4		0		V_{CC}	V

NOTE 1: V_C = 0V to V_{CC}. Oscillator gain is programmed by IDT. Gain = (25 · n) ÷ V_{CC} and is in the range of n=1 to n = 63.
NOTE 2: Nominal oscillator gain: Pull range from Table 3B divided by the control voltage tuning range of 3.3V.
NOTE 3: For best phase noise performance, use the lowest K_V that meets the requirements of the application.
NOTE 4: BSL = Best Straight Line Fit: Variation of the output frequency vs. control voltage V_C, in percent. V_C ranges from 10% to 90% V_{CC}.

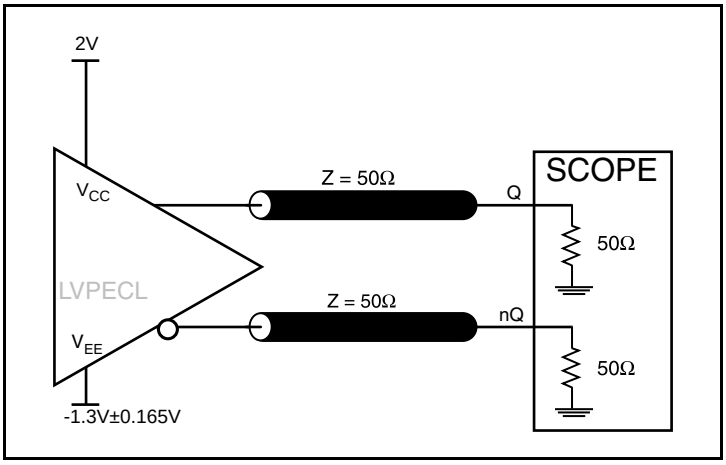
Typical Phase Noise at 622.08MHz (12kHz - 20MHz)



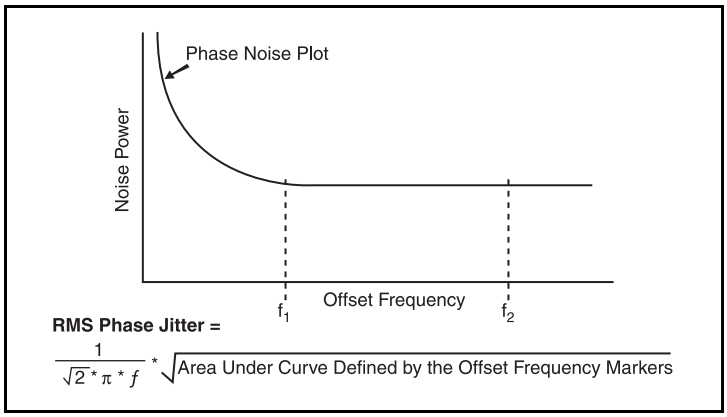
Parameter Measurement Information



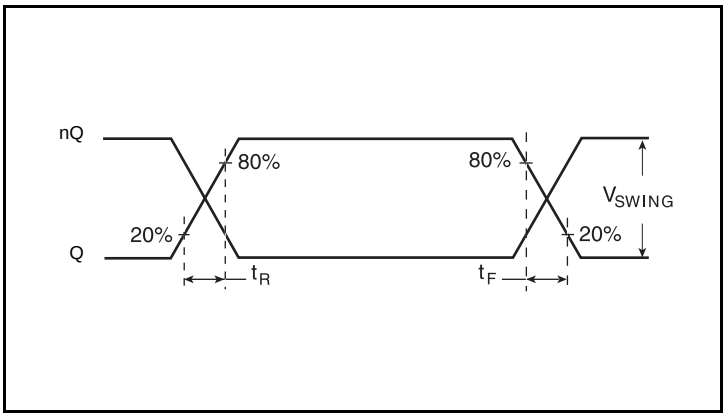
2.5V LVPECL Output Load AC Test Circuit



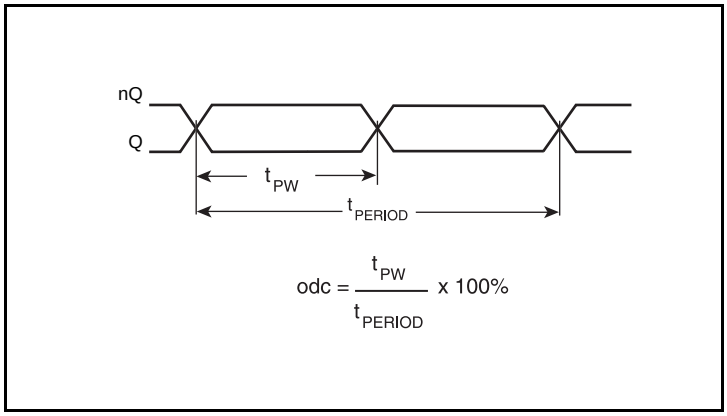
3.3V LVPECL Output Load AC Test Circuit



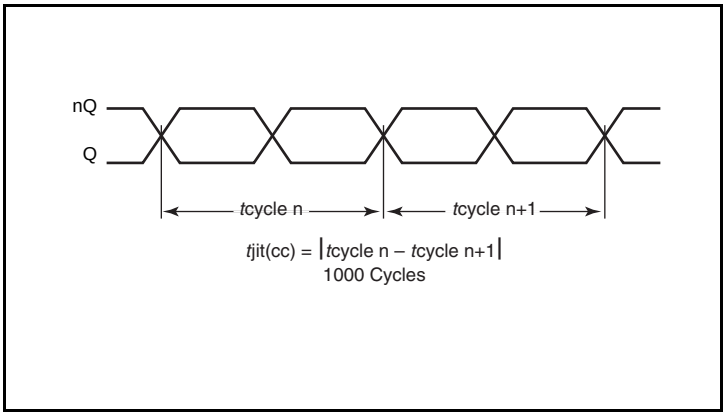
RMS Phase Jitter



Output Rise/Fall Time

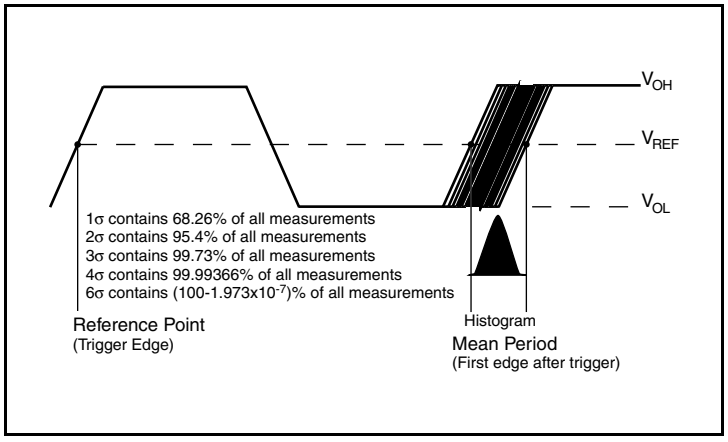


Output Duty Cycle/Pulse Width/Period



Cycle-to-Cycle Jitter

Parameter Measurement Information, continued



RMS Period Jitter

Applications Information

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 1A and 1B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

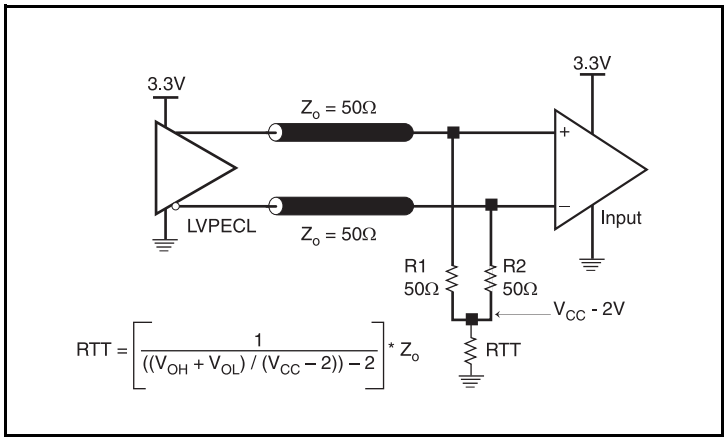


Figure 1A. 3.3V LVPECL Output Termination

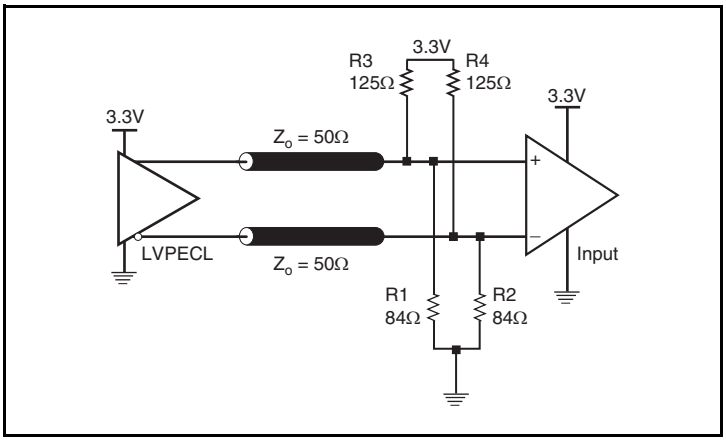


Figure 1B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 2A and *Figure 2B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 2B can be eliminated and the termination is shown in *Figure 2C.*

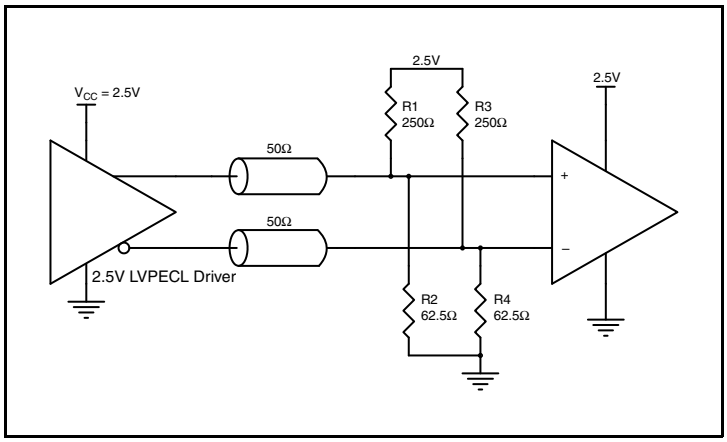


Figure 2A. 2.5V LVPECL Driver Termination Example

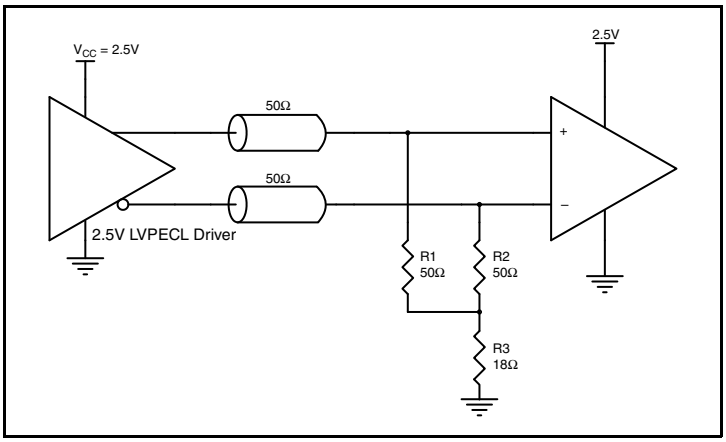


Figure 2B. 2.5V LVPECL Driver Termination Example

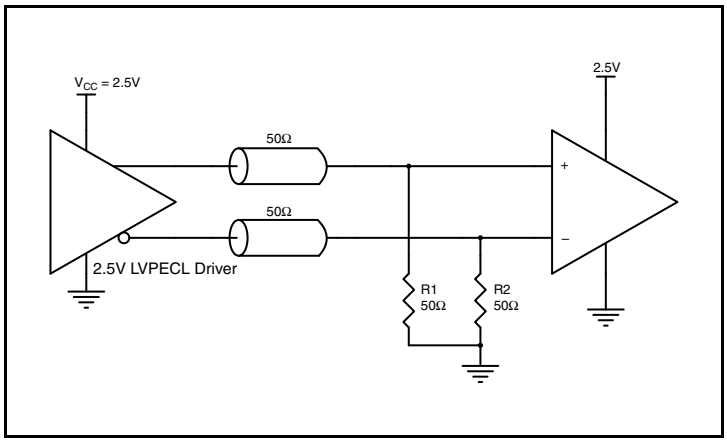


Figure 2C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8N3DV85.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8N3DV85 is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 160mA = **554.40mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 554.40mW + 30mW = **584.40mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.4°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.584W * 49.4°C/W = 113.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 6 Lead Ceramic VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	42.1°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 3.*

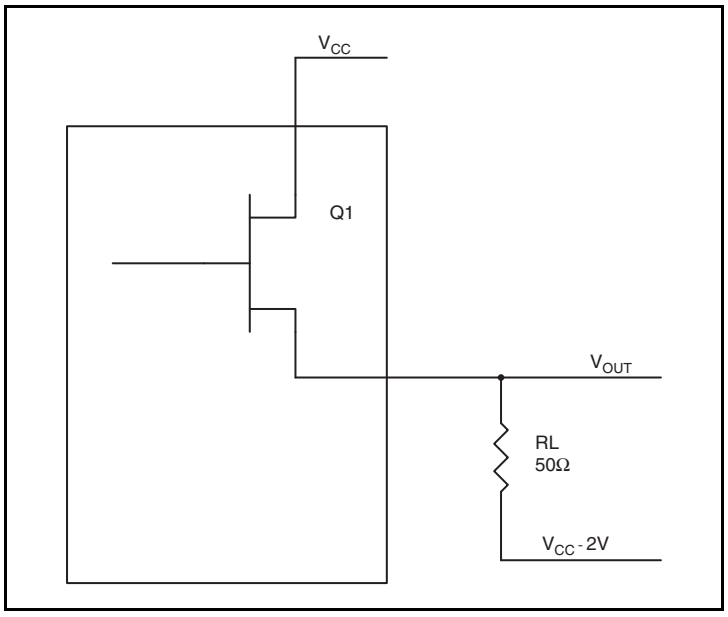


Figure 3. LVPECL Driver Circuit and Termination

To calculate power dissipation due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

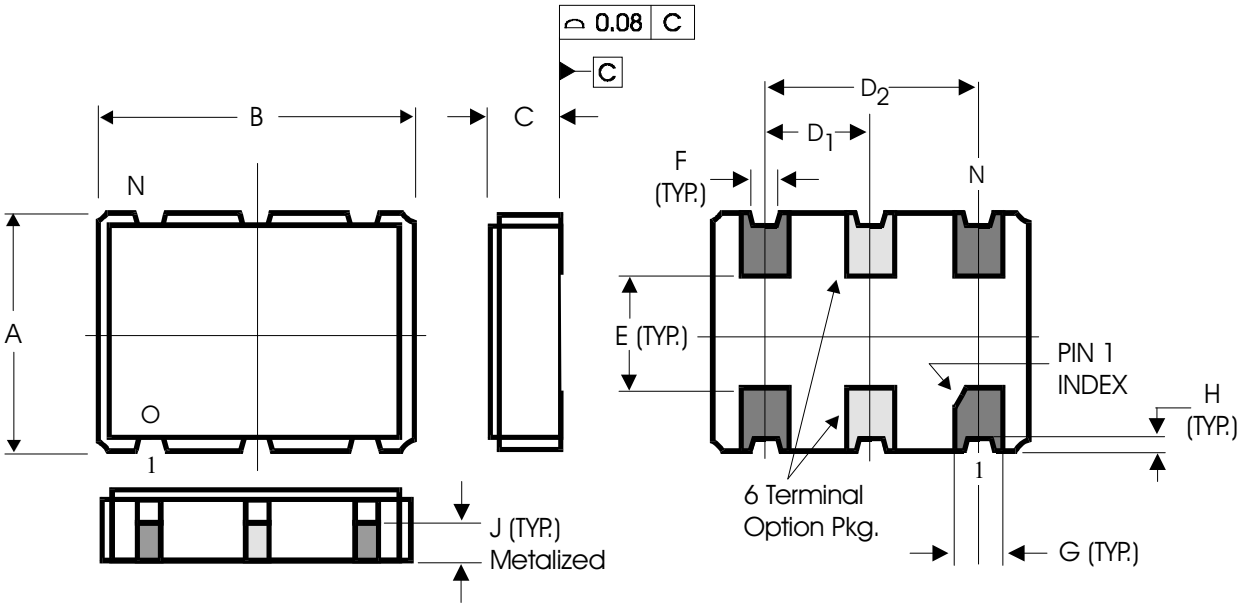
Table 7. θ_{JA} vs. Air Flow Table for a 6-lead Ceramic 5mm x 7mm Package

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	42.1°C/W

Transistor Count

The transistor count for IDT8N3DV85 is: 47,511

Package Outline and Package Dimensions



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	4.85	5.00	5.15
B	6.85	7.00	7.15
C	1.35	1.50	1.65
D_1	2.41	2.54	2.67
D_2	4.95	5.08	5.21
E	2.47	2.6	2.73
F	0.47	0.60	0.73
G	1.27	1.40	1.53
H	-	0.15 Ref.	-
J	-	0.65 Ref.	-

Ordering Information for FemtoClock® NG Ceramic-Package XO and VCXO Products

The programmable VCXO and XO devices support a variety of devices options such as the output type, number of default frequencies, internal crystal frequency, power supply voltage, ambient temperature range and the frequency accuracy. The device options, default frequencies and default VCXO pull range must be specified at the time of order and are programmed by IDT before the shipment. The table below specifies the available order codes, including the device options and default frequency configurations. Example part number: the order code 8N3QV01FG-0001CDI specifies a programmable, quad default-frequency VCXO with a voltage supply of 2.5V, a LVPECL output, a ±50 ppm crystal frequency accuracy, contains a 114.285MHz internal crystal as frequency source, industrial temperature range, a lead-free (6/6 RoHS) 6-lead ceramic 5mm x 7mm x 1.55mm package and is factory-programmed to the default frequencies of 100MHz, 122.88MHz, 125MHz and 156.25MHz and to the VCXO pull range of minimum ±100 ppm.

Other default frequencies and order codes are available from IDT on request. For more information on available default frequencies, see the *FemtoClock N Ceramic-Package XO and VCXO Ordering Product Information* document.

Part/Order Number

8N X X XXX X X - dddd XX X X

FemtoClock NG

I/O Identifier
0: LVCMOS
3: LVPECL
4: LVDS

Number of Default Frequencies
S: 1: Single
D: 2: Dual
Q: 4: Quad

Part Number

	Function	#pins	OE fct. at pin
001	XO	10	OE@2
003	XO	10	OE@1
V01	VCXO	10	OE@2
V03	VCXO	10	OE@1
V75	VCXO	6	OE@2
V76	VCXO	6	nOE@2
V85	VCXO	6	—
085	XO	6	OE@1
270	XO	6	OE@1
271	XO	6	OE@2
272	XO	6	nOE@2
273	XO	6	nOE@1

Shipping Package
8: Tape & Reel
(no letter): Tray

Ambient Temperature Range
"**I**": Industrial: (T_A = -40°C to 85°C)
(no letter): (T_A = 0°C to 70°C)

Package Code
CD: Lead-Free, 6/10-lead ceramic 5mm x 7mm x 1.55mm

Default-Frequency and VCXO Pull Range
See document *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information.*

dddd	f_{XTAL} (MHz)	PLL feedback	Use for
0000 to **0999**	114.285	Fractional	VCXO, XO
1000 to **1999**	100.000	Integer	XO
2000 to **2999**		Fractional	XO

Last digit = **L**: configuration pre-programmed and not changeable

Die Revision
C

Option Code (Supply Voltage and Frequency-Stability)
A: V_{CC} = 3.3V±5%, ±100ppm
B: V_{CC} = 2.5V±5%, ±100ppm
E: V_{CC} = 3.3V±5%, ±50ppm
F: V_{CC} = 2.5V±5%, ±50ppm
K: V_{CC} = 3.3V±5%, ±20ppm
L: V_{CC} = 2.5V±5%, ±20ppm

Table 8. Device Marking

Marking	Industrial Temperature Range (T_A = -40°C to 85°C)	Commercial Temperature Range (T_A = 0°C to 70°C)
	IDT8N3DV85**y**C- **dddd**CDI	IDT8N3DV85**y**C- **dddd**CD
	y = Option Code, **dddd**=Default-Frequency and VCXO Pull Range	

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T6	6	Absolute Maximum Rating - corrected Package Thermal Impedance.	4/27/12
		12	Added RMS Period Jitter diagram	
		14	Power Considerations - corrected Thermal Resistance table, updated Junction Temperature calculation.	
	T7	13	Corrected Air Flow table.	
A	AMR	6	Absolute Maximum Rating; V_{CC} = 3.71V	2/5/13
A	T5A	7	AC Characteristic Tables - RMS Phase Jitter changed test conditions from: 500MHz ≤ f_{OUT} to 500MHz < f_{OUT}; 125MHz ≤ f_{OUT} to 125MHz < f_{OUT}.	10/30/13

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