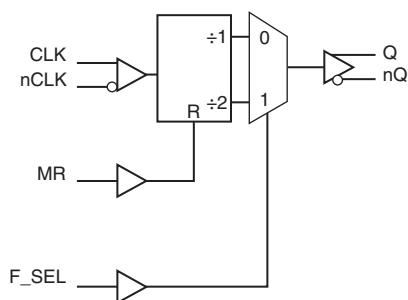
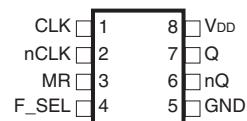


**PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017****GENERAL DESCRIPTION**

The 87421I is a high performance  $\div 1/\div 2$  Differential-to-LVDS Clock Generator. The CLK, nCLK pair can accept most standard differential input levels. The 87421I is characterized to operate from a 3.3V power supply. Guaranteed part-to-part skew characteristics make the 87421I ideal for those clock distribution applications demanding well defined performance and repeatability.

**FEATURES**

- One differential LVDS output
- One differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum clock input frequency: 1GHz
- Translates any single ended input signal (LVCMS, LVTTL, GTL) to LVDS levels with resistor bias on nCLK input
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 1.7ns (maximum)
- Additive phase jitter, RMS @ 155.52MHz: 0.17ps (typical)
- Full 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- **For functional replacement device use 87321**

**BLOCK DIAGRAM****PIN ASSIGNMENT**

**87421I**  
**8-Lead SOIC**  
3.90mm x 4.90mm x 1.37mm package body  
**M Package**  
Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name            | Type   |          | Description  |
|--------|-----------------|--------|----------|--|
| 1      | CLK             | Input  | Pulldown | Non-inverting differential clock input.  |
| 2      | nCLK            | Input  | Pullup   | Inverting differential clock input.  |
| 3      | MR              | Input  | Pulldown | Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true output (Q) to go low and the inverted output (nQ) to go high. When logic LOW, the internal dividers and the output are enabled. LVCMS / LVTTL interface levels. See Table 3. |
| 4      | F_SEL           | Input  | Pulldown | Selects divider value for Q, nQ outputs as described in Table 3. LVCMS / LVTTL interface levels.   |
| 5      | GND             | Power  |          | Power supply ground.   |
| 6, 7   | Q, nQ           | Output |          | Differential output pair. LVDS interface levels.   |
| 8      | V <sub>DD</sub> | Power  |          | Positive supply pin.   |

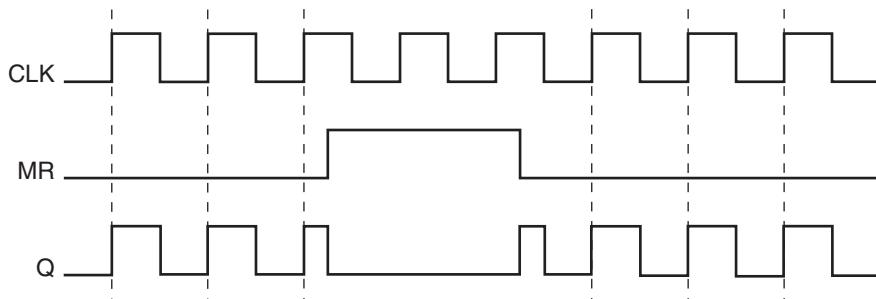
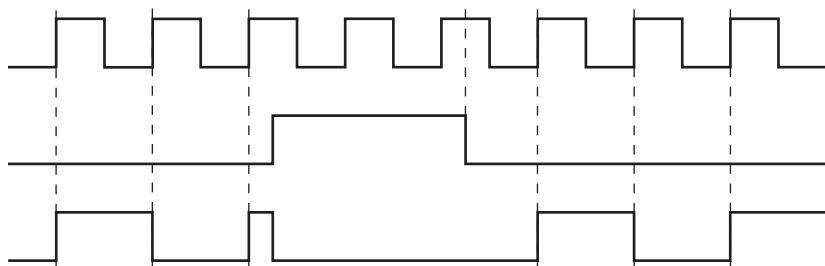
NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 4       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |

TABLE 3. FUNCTION TABLE

| MR | F_SEL | Divide Value                        |
|----|-------|-------------------------------------|
| 1  | X     | Reset: Q output low, nQ output high |
| 0  | 0     | ÷1                                  |
| 0  | 1     | ÷2                                  |

FIGURE 1A.  $\div 1$  CONFIGURATION TIMING DIAGRAMFIGURE 1B.  $\div 2$  CONFIGURATION TIMING DIAGRAM

## ABSOLUTE MAXIMUM RATINGS

|  |                           |
|--|---------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                      |
| Inputs, $V_I$                            | -0.5V to $V_{DD}$ + 0.5 V |
| Outputs, $I_O$                           |                           |
| Continuous Current                       | 10mA                      |
| Surge Current                            | 15mA                      |
| Package Thermal Impedance, $\theta_{JA}$ | 96°C/W (0 mps)            |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C            |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$ 

| Symbol   | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$ | Positive Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{DD}$ | Power Supply Current    |                 |         | 55      |         | mA    |

TABLE 4B. LVCMS/LVTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$ 

| Symbol   | Parameter          | Test Conditions | Minimum                        | Typical | Maximum        | Units         |
|----------|--------------------|-----------------|--------------------------------|---------|----------------|---------------|
| $V_{IH}$ | Input High Voltage |                 | 1.37                           |         | $V_{DD} + 0.3$ | V             |
| $V_{IL}$ | Input Low Voltage  |                 | -0.3                           |         | 0.7            | V             |
| $I_{IH}$ | Input High Current | MR, F_SEL       | $V_{DD} = V_{IN} = 3.465V$     |         | 150            | $\mu\text{A}$ |
| $I_{IL}$ | Input Low Current  | MR, F_SEL       | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5      |                | $\mu\text{A}$ |

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$ 

| Symbol    | Parameter                            | Test Conditions | Minimum                        | Typical   | Maximum         | Units         |
|-----------|--------------------------------------|-----------------|--------------------------------|-----------|-----------------|---------------|
| $I_{IH}$  | Input High Current                   | CLK             | $V_{DD} = V_{IN} = 3.465V$     |           | 150             | $\mu\text{A}$ |
|           |                                      | nCLK            | $V_{DD} = V_{IN} = 3.465V$     |           | 5               | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current                    | CLK             | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5        |                 | $\mu\text{A}$ |
|           |                                      | nCLK            | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150      |                 | $\mu\text{A}$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage           |                 | 0.15                           |           | 1.3             | V             |
| $V_{CMR}$ | Common Mode Input Voltage;<br>NOTE 1 |                 |                                | GND + 0.5 | $V_{DD} - 0.85$ | V             |

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

**TABLE 4D. LVDS DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

| Symbol          | Parameter                   | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| $V_{OD}$        | Differential Output Voltage |                 | 350     | 470     | 540     | mV    |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change   |                 |         |         | 50      | mV    |
| $V_{OS}$        | Offset Voltage              |                 | 1.1     | 1.25    | 1.4     | V     |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change   |                 |         |         | 50      | mV    |

**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

| Symbol      | Parameter  | Test Conditions                                | Minimum | Typical | Maximum | Units |
|-------------|--|--|---------|---------|---------|-------|
| $f_{CLK}$   | Clock Input Frequency  |  |         |         | 1       | GHz   |
| $t_{PD}$    | Propagation Delay; CLK to Q (Dif)<br>NOTE 1                          |  | 1.0     |         | 1.7     | ns    |
| tsk(pp)     | Part-to-Part Skew; NOTE 2, 3   |  |         |         | 500     | ps    |
| $t_{JIT}$   | Additive Phase Noise, RMS;<br>refer to Additive Phase Jitter Section | 155.52MHz, Integration Range:<br>12kHz – 20MHz |         | 0.17    |         | ps    |
| $t_R / t_F$ | Output Rise/Fall Time  | 20% to 80%                                     | 150     |         | 500     | ps    |
| odc         | Output Duty Cycle  | $f_{IN} < 500MHz$                              | 43      |         | 57      | %     |

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

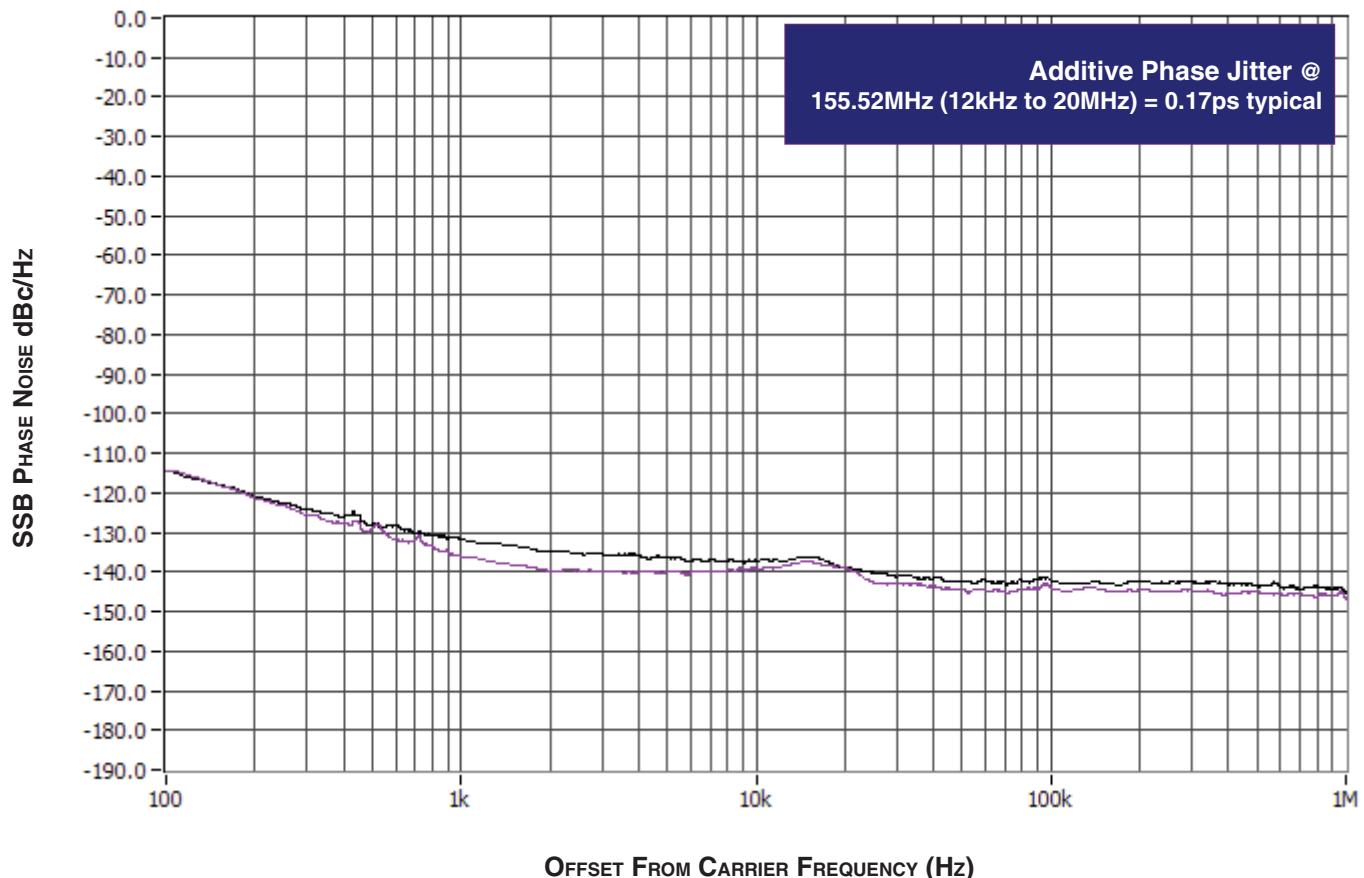
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

## ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels

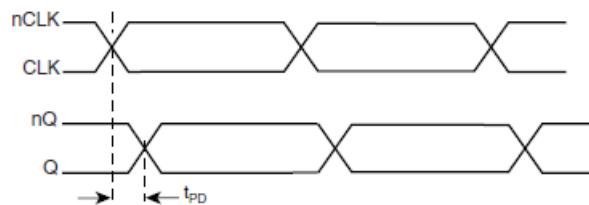
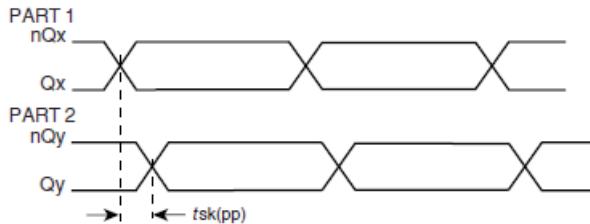
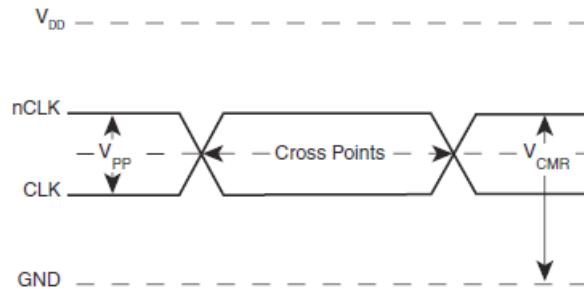
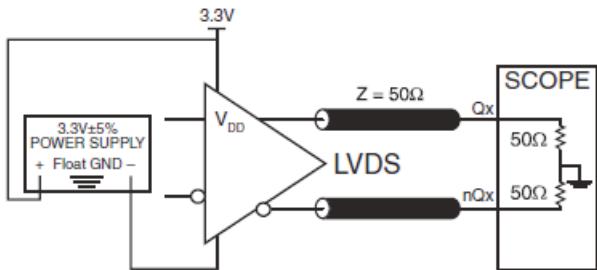
(dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



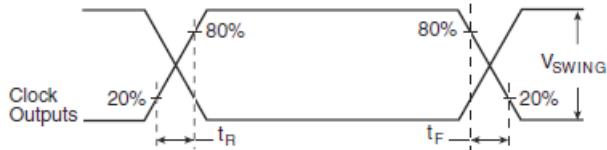
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor

of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

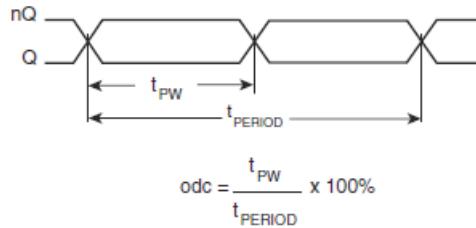
## PARAMETER MEASUREMENT INFORMATION



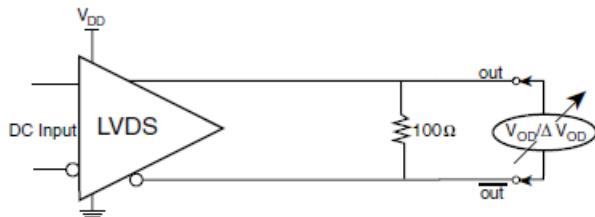
## PART-TO-PART SKEW



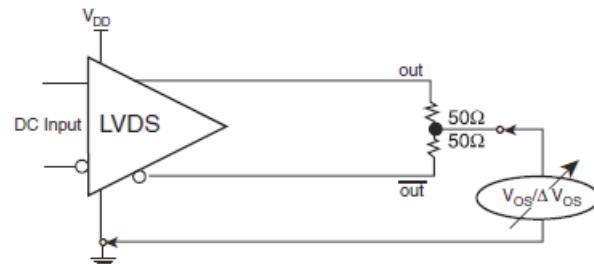
## PROPAGATION DELAY



## OUTPUT RISE/FALL TIME



## OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



## DIFFERENTIAL OUTPUT VOLTAGE SETUP

## OFFSET VOLTAGE SETUP

## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

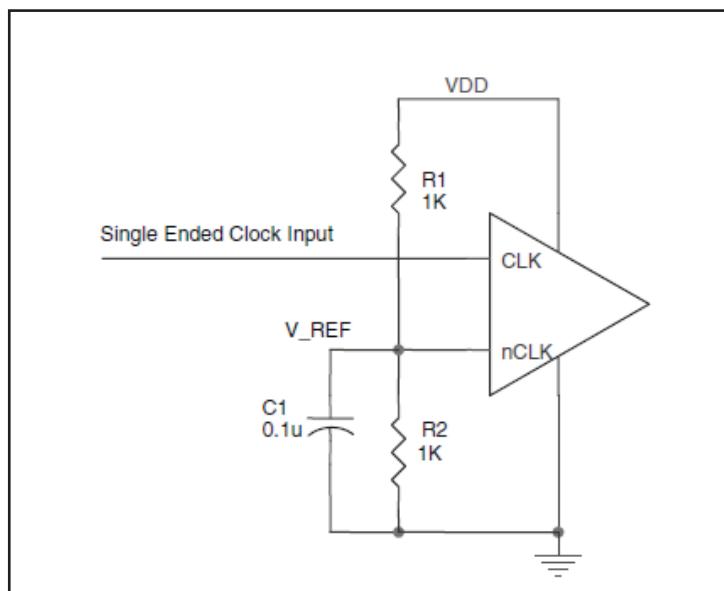


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

### RECOMMENDATIONS FOR UNUSED INPUT PINS

#### INPUTS:

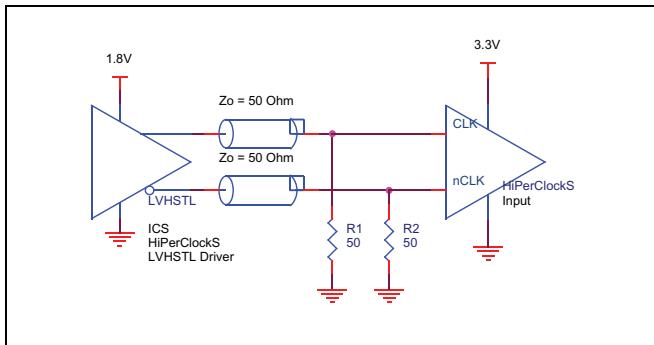
##### LVC MOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A  $1k\Omega$  resistor can be used.

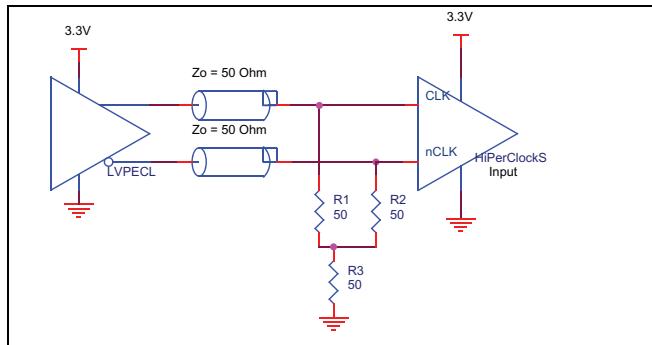
## DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

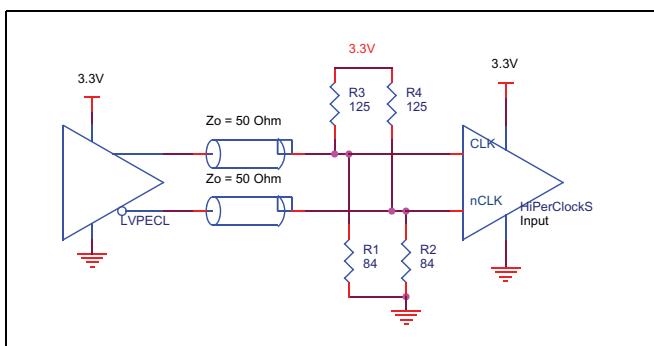
Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



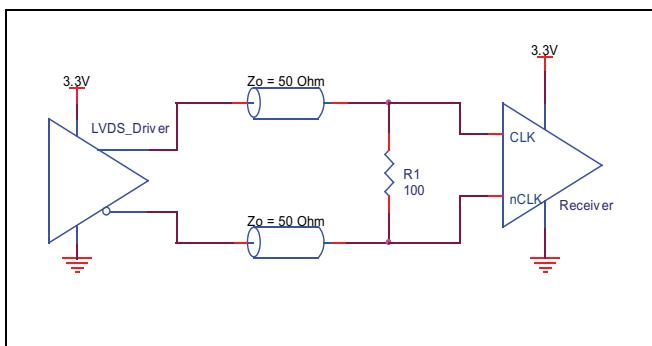
**FIGURE 3A. HiPerClockS CLK/nCLK INPUT  
DRIVEN BY AN IDT OPEN Emitter  
HiPerClockS LVHSTL DRIVER**



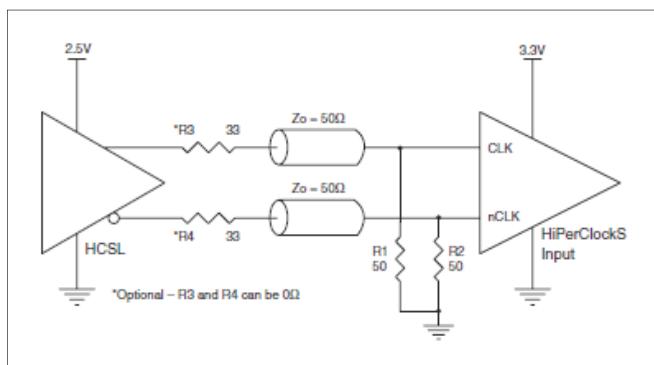
**FIGURE 3B. HiPerClockS CLK/nCLK INPUT  
DRIVEN BY A 3.3V LVPECL DRIVER**



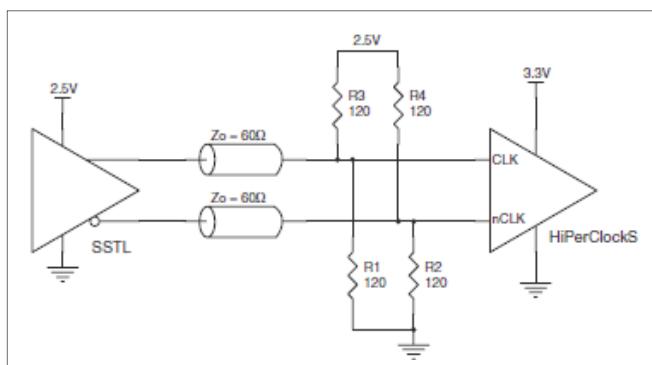
**FIGURE 3C. HiPerClockS CLK/nCLK INPUT  
DRIVEN BY A 3.3V LVPECL DRIVER**



**FIGURE 3D. HiPerClockS CLK/nCLK INPUT  
DRIVEN BY A 3.3V LVDS DRIVER**



**FIGURE 3E. HiPerClockS CLK/nCLK INPUT  
DRIVEN BY A 3.3V HCSL DRIVER**



**FIGURE 3F. HiPerClockS CLK/nCLK INPUT  
DRIVEN BY A 2.5V SSTL DRIVER**

## LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4*. In a  $100\Omega$  differential transmission line environment, LVDS drivers require a matched load termination of  $100\Omega$  across near the receiver input. For a

multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

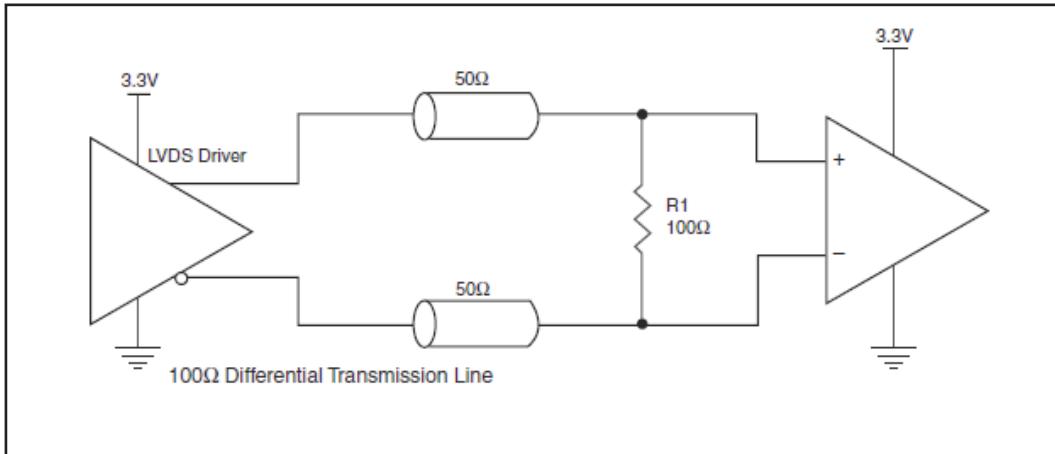


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 87421I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 87421I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

$$\text{Power}_{\text{MAX}} = V_{DD_{\text{MAX}}} * I_{DD_{\text{MAX}}} = 3.465V * 55\text{mA} = 198.58\text{mW}$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * P_{d\_total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$P_{d\_total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 96°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.199W \* 96°C/W = 104.1°C. This is well below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-PIN SOIC, FORCED CONVECTION

| $\theta_{JA}$ by Velocity (Meters per Second) |        |        |        |
|---|--------|--------|--------|
|   | 0      | 1      | 2.5    |
| Multi-Layer PCB, JEDEC Standard Test Boards   | 96°C/W | 87°C/W | 82°C/W |

## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 8 LEAD SOIC

| $\theta_{JA}$ by Velocity (Meters per Second) |        |        |        |
|---|--------|--------|--------|
|   | 0      | 1      | 2.5    |
| Multi-Layer PCB, JEDEC Standard Test Boards   | 96°C/W | 87°C/W | 82°C/W |

### TRANSISTOR COUNT

The transistor count for 874211 is: 417

## PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

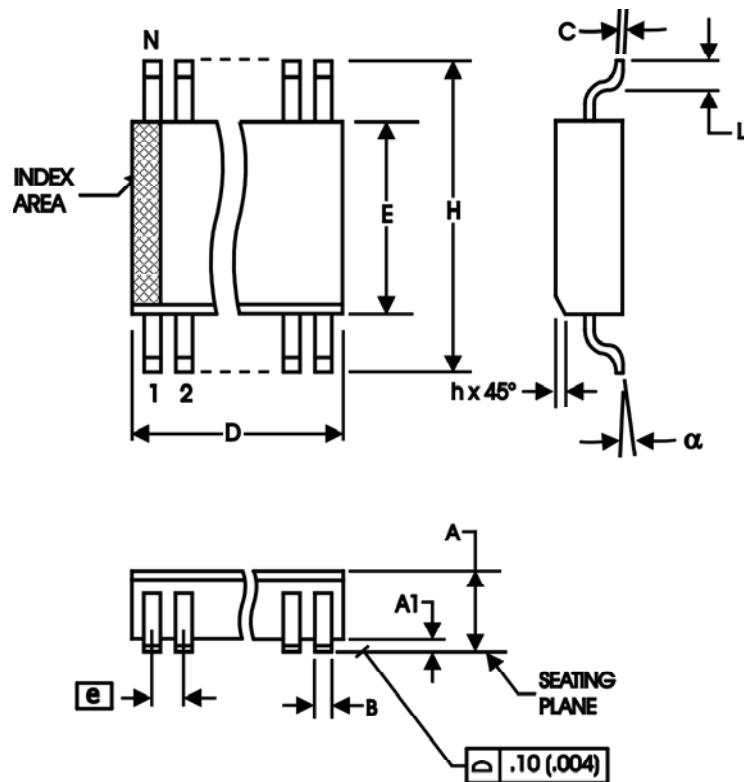


TABLE 8. PACKAGE DIMENSIONS

| SYMBOL   | Millimeters |           |
|----------|-------------|-----------|
|          | MINIMUM     | MAXIMUM   |
| N        | 8           |           |
| A        | 1.35        | 1.75      |
| A1       | 0.10        | 0.25      |
| B        | 0.33        | 0.51      |
| C        | 0.19        | 0.25      |
| D        | 4.80        | 5.00      |
| E        | 3.80        | 4.00      |
| e        | 1.27 BASIC  |           |
| H        | 5.80        | 6.20      |
| h        | 0.25        | 0.50      |
| L        | 0.40        | 1.27      |
| $\alpha$ | $0^\circ$   | $8^\circ$ |

Reference Document: JEDEC Publication 95, MS-012

**TABLE 9. ORDERING INFORMATION**

| Part/Order Number | Marking  | Package                 | Shipping Packaging | Temperature   |
|-------------------|----------|-------------------------|--------------------|---------------|
| 87421AMILF        | 87421AIL | 8 lead "Lead-Free" SOIC | tube               | -40°C to 85°C |
| 87421AMIFT        | 87421AIL | 8 lead "Lead-Free" SOIC | tape & reel        | -40°C to 85°C |

## REVISION HISTORY SHEET

| Rev | Table | Page | Description of Change  | Date    |
|-----|-------|------|--|---------|
| A   | T9    | 13   | Ordering Information - removed leaded devices.<br>Updated data sheet format.   | 7/20/15 |
| A   | T9    | 13   | Product Discontinuation Notice - Last time buy expires May 6, 2017.<br>PDN CQ-16-01<br>Ordering Information - Deleted LF note below table.<br>Updated header and footer. | 6/24/16 |



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