Differential-to-LVCMOS/LVTTL Fanout Buffer w/Divider and Glitchless Switch

ICS870S208

DATASHEET

General Description

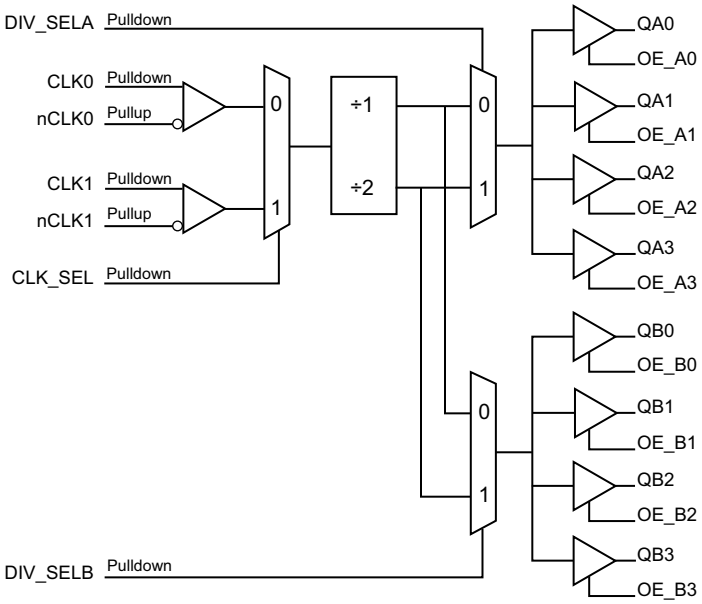
The ICS870S208 is a low skew, eight output LVCMOS / LVTTL Fanout Buffer with selectable divider. The ICS870S208 has two selectable inputs that accept a variety of differential input types. The device provides the capability to suppress any glitch at the outputs of the device during an input clock switch to enhance clock redundancy in fault tolerant applications. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 8 to 16 by utilizing the ability of the outputs to drive two series terminated lines. The divide select inputs, DIV_SELA and DIV_SELB, control the output frequency of each bank. The output banks can be independently selected for ÷1 or ÷2 operation. The output enable pins assigned to each output, support enabling and disabling of each output individually.

The ICS870S208 is characterized at full 3.3V and 2.5V, and mixed 3.3V/2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the ICS870S208 ideal for high performance, single ended applications.

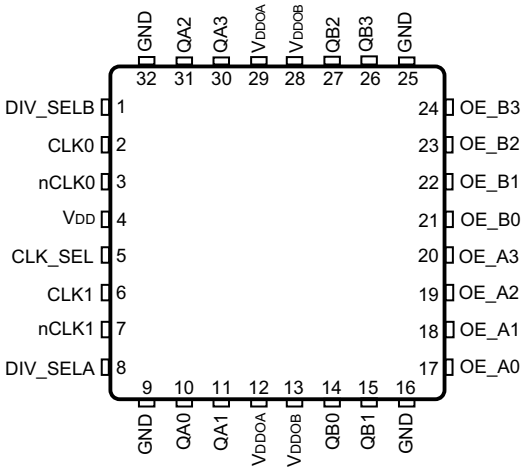
Features

- Eight LVCMOS/LVTTL outputs, (2 banks of 4 outputs)
  Each output has individual synchronous output enable
- Two selectable differential CLKx, nCLKx inputs
- Dual differential input pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL
- Maximum output frequency: 250MHz
- Selectable ÷1 or ÷2 operation
- Glitchless output behavior during input switch
- Output skew: 120ps (maximum), 3.3V
- Bank skew: 65ps (maximum), 3.3V
- Supply modes:
  Core/Output
  3.3V/3.3V
  2.5V/2.5V
  3.3V/2.5V
- 0°C to 70°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



ICS870S208
32-Lead VFQFN
5mm x 5mm x 0.9mm package body
3.15mm x 3.15mm EPad Size
K Package
Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	DIV_SELB	Input	Pulldown	Controls frequency division for Bank B outputs. LVCMOS / LVTTL interface levels.
2	CLK0	Input	Pulldown	Non-inverting differential clock input.
3	nCLK0	Input	Pullup	Inverting differential clock input.
4	V_{DD}	Power		Power supply pin.
5	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1 inputs, When LOW, selects CLK0, nCLK0 inputs. LVCMOS / LVTTL interface levels.
6	CLK1	Input	Pulldown	Non-inverting differential clock input.
7	nCLK1	Input	Pullup	Inverting differential clock input.
8	DIV_SELA	Input	Pulldown	Controls frequency division for Bank A outputs. LVCMOS / LVTTL interface levels.
9, 16, 25, 32	GND	Power		Power supply ground.
10, 11, 30, 31	QA0, QA1, QA3, QA2	Output		Single-ended Bank A clock outputs. LVCMOS / LVTTL interface levels.
12, 29	V_{DDOA}	Power		Output supply pins for Bank A outputs.
13, 28	V_{DDOB}	Power		Output supply pins for Bank B outputs.
14, 15 26, 27	QB0, QB1, QB3, QB2	Output		Single-ended Bank B clock outputs. LVCMOS / LVTTL interface levels.
17	OE_A0	Input	Pullup	Output enable for QA0 output. Active HIGH. If OE pin is LOW, outputs will drive in high-impedance. See Table 3. LVCMOS / LVTTL interface levels.
18	OE_A1	Input	Pullup	Output enable for QA1 output. Active HIGH. If OE pin is LOW, outputs will drive in high-impedance. See Table 3. LVCMOS / LVTTL interface levels.
19	OE_A2	Input	Pullup	Output enable for QA2 output. Active HIGH. If OE pin is LOW, outputs will drive in high-impedance. See Table 3. LVCMOS / LVTTL interface levels.
20	OE_A3	Input	Pullup	Output enable for QA3 output. Active HIGH. If OE pin is LOW, outputs will drive in high-impedance. See Table 3. LVCMOS / LVTTL interface levels.
21	OE_B0	Input	Pullup	Output enable for QB0 output. Active HIGH. If OE pin is LOW, outputs will drive in high-impedance. See Table 3. LVCMOS / LVTTL interface levels.
22	OE_B1	Input	Pullup	Output enable for QB1 output. Active HIGH. If OE pin is LOW, outputs will drive in high-impedance. See Table 3. LVCMOS / LVTTL interface levels.
23	OE_B2	Input	Pullup	Output enable for QB2 output. Active HIGH. If OE pin is LOW, outputs will drive in high-impedance. See Table 3. LVCMOS / LVTTL interface levels.
24	OE_B3	Input	Pullup	Output enable for QB3 output. Active HIGH. If OE pin is LOW, outputs will drive in high-impedance. See Table 3. LVCMOS / LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD} = $V_{DDOA, B}$ = 3.465V		8		pF
		V_{DD} = $V_{DDOA, B}$ = 2.625V		7		pF
		V_{DD} = 3.465V, $V_{DDOA, B}$ = 2.625V		7		pF
R_{PULLUP}	Input Pullup Resistor			50		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ
R_{OUT}	Output Impedance			15		Ω

Function Tables

Table 3. Output Enable Function Table

Control Inputs	Outputs
OE_x [0:3]	**QA[0:3], QB[0:3]**
0	High-Impedance
1 (default)	Active

NOTE: Where x = A or B.

Function Description

Two Valid Clocks

The ICS87S0208 has a glitch free input mux that is controlled by the CLK_SEL pin. It is designed to switch between 2 input clocks whether running or not. In the case where both clocks are running, when CLK_SEL changes, the output clocks go low after one cycle of the output clock (nominally). The outputs then stay low for one cycle of the new input clock (nominally) and then begin to follow the new input clock. This is shown in *Figure 1A.*

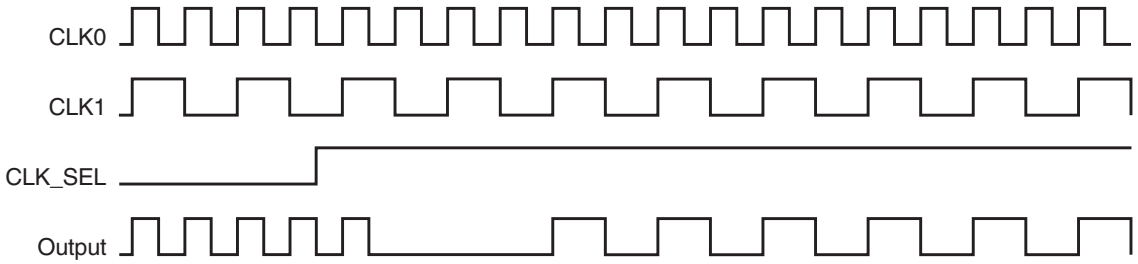


Figure 1A. CLK_SEL Timing Diagram

When DIV_SEL changes, the part waits for the output to complete the cycle of the selected divider then changes seamlessly to the new divider.

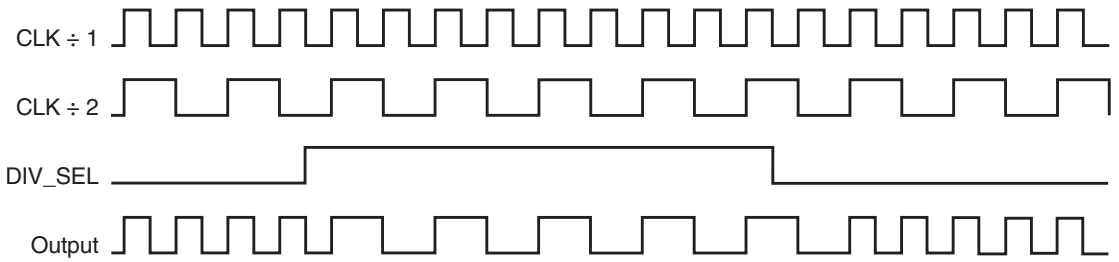


Figure 1B. DIV_SELx Timing Diagram

When an output enable pin is pulled low, the part waits for the output to complete its period, then transitions to an High-Impedance state. When output enable is asserted, the output transitions from a High-Impedance to a low state to ensure a clean rising edge of the first output clock.

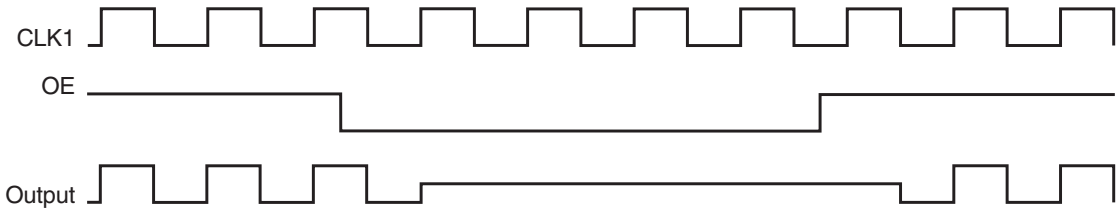


Figure 1C. OEx Timing Diagram

Bad Input Clock

An internal timer monitors the state of both input clocks. If a clock is stopped (stuck high or low for over approximately 200ns), its internal input bad flag is set and the part will perform as depicted in the following diagrams. If the clock is restored, the internal input bad detector waits for 4 full clock periods before clearing the input bad flag and returning to normal operation.

If the selected input clock goes bad (stuck high or low for over approximately 200ns), an internal input bad flag is set. When the input bad flag is set, the output goes low until the next valid clock event. If the selected clock is restored, the input bad detector waits 4 full clock periods before clearing the flag and returning to normal operation. If CLK_SEL is changed to select a valid input clock, the output will stay low for one full period of the new input clock, then return to normal operation.

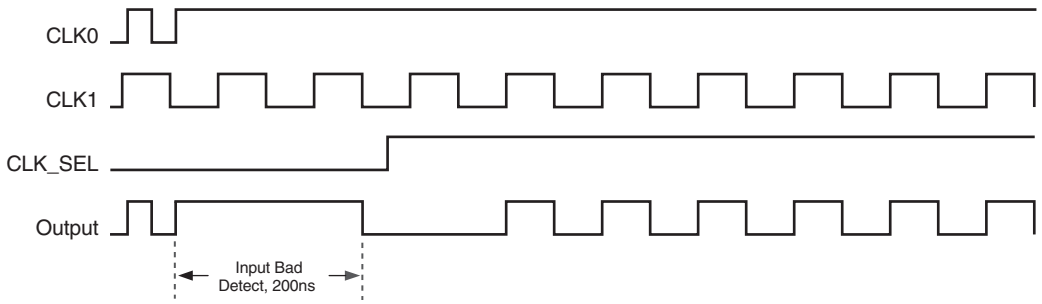


Figure 1D. CLK_SEL with Bad Input Timing Diagram

If the selected input clock goes bad (stuck high or low for over approximately 200ns), an internal input bad flag is set. When the input bad flag is set, the output goes low until the next valid clock event. If DIV_SEL is changed, the output will transition from the low state following the selected divide when a valid input clock is restored.

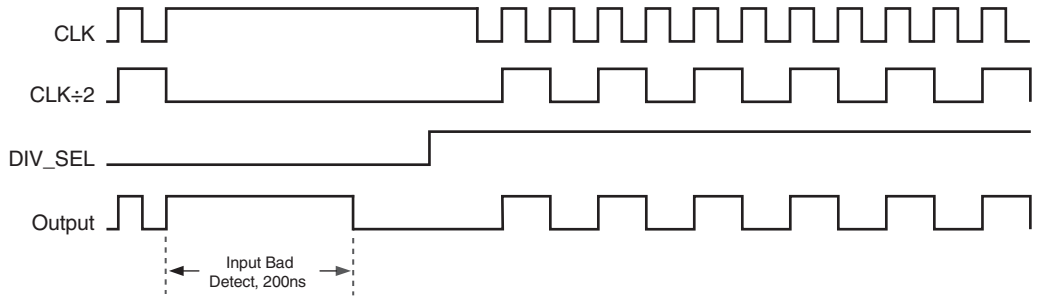


Figure 1E. DIV_SELx with Bad Input Timing Diagram

If the input bad flag has been set (The input has been stuck high or low for over approximately 200ns), and OEx is pulled low, the output will immediately go to a High-Impedance state. If the clock is restored while the OEx is low, the output will transition from the High-Impedance to a low state to ensure a clean rising edge of the first output clock when the Oex is pulled high again.

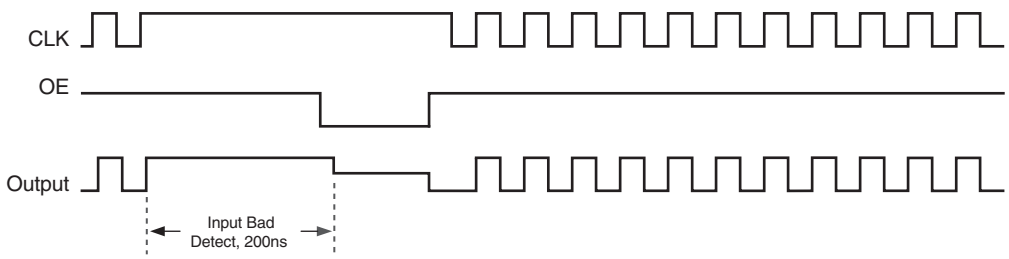


Figure 1F. OEx with Bad Input Timing Diagram

Switch During an Input Bad Detect

If a CLK_SEL, DIV_SEL, or OE event happens after a clock has stopped, but before the input bad flag has been set (during the ~200ns detect period) the output change will not take effect until the internal bad flag has been set. The output will go low after the input bad flag is set and follow the second period of the new clock input. Although no glitches will occur, due to the unknown state of the failing clock, a transition may take up to 1us to execute.

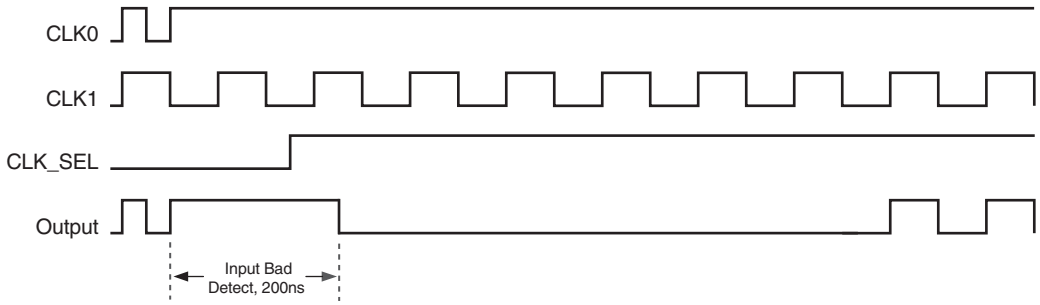


Figure 1G. CLK_SEL with Bad Input Timing Diagram

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to $V_{DDOA, B}$ + 0.5V
Package Thermal Impedance, θ_{JA}	42.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				80	mA
I_{DDOA}, I_{DDOB}	Output Supply Current	No Load			1	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 2.5V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				80	mA
I_{DDOA}, I_{DDOB}	Output Supply Current	No Load			1	mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDOA} = V_{DDOB} = 2.5V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				80	mA
I_{DDOA}, I_{DDOB}	Output Supply Current	No Load			1	mA

Table 4D. LVCMOS/LVTTL DC Characteristics, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V ± 5%	2.2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V ± 5%	-0.3		0.8	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
I_{IH}	Input High Current	CLK_SEL, DIV_SELA, DIV_SELB	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
		OE_A[0:3], OE_B[0:3]	V_{DD} = V_{IN} = 3.465V or 2.625V			10	µA
I_{IL}	Input Low Current	CLK_SEL, DIV_SELA, DIV_SELB	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA
		OE_A[0:3], OE_B[0:3]	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDOA, VDDOB}$ = 3.465V	2.6			V
			$V_{DDOA, VDDOB}$ = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDOA, VDDOB}$ = 3.465V or 2.625V			0.55	V

NOTE 1: Outputs are terminated with 50Ω to $V_{DDOA, B}$/2. See Parameter Measurement section, *Load Test Circuit* diagrams.

Table 4E. Differential DC Characteristics, V_{DD} = 3.3V ± 5% or 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1	V_{DD} = V_{IN} = 3.465V or 2.625V			10	µA
		CLK0, CLK1	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		CLK0, CLK1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\% = T_A = 0°C$ to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{out}	Output Frequency					250	MHz
t_{PD}	Propagation Delay; NOTE 1			2.3		3.8	ns
*t*sk(o)	Output Skew; NOTE 2, 3					120	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					225	ps
*t*sk(b)	Bank Skew; NOTE 3, 5	QA[0:3], nQA[0:3]				65	ps
		QB[0:3], nQB[0:3]				60	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	150		600	ps
t_{EN}	Output Enable Time; NOTE 6					10	ns
t_{DIS}	Output Disable Time; NOTE 6					10	ns
odc	Output Duty Cycle			45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crosspoint to $V_{DDOA, B}/2$ of the output.
NOTE 2: Defined as between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOA, B}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOA, B}/2$.
NOTE 5: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

Table 5B. AC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 2.5V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{out}	Output Frequency					250	MHz
t_{PD}	Propagation Delay; NOTE 1			2.4		4.0	ns
*t*sk(o)	Output Skew; NOTE 2, 3					135	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					225	ps
*t*sk(b)	Bank Skew; NOTE 3, 5	QA[0:3], nQA[0:3]				70	ps
		QB[0:3], nQB[0:3]				60	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	150		600	ps
t_{EN}	Output Enable Time; NOTE 6					10	ns
t_{DIS}	Output Disable Time; NOTE 6					10	ns
odc	Output Duty Cycle			44		56	%

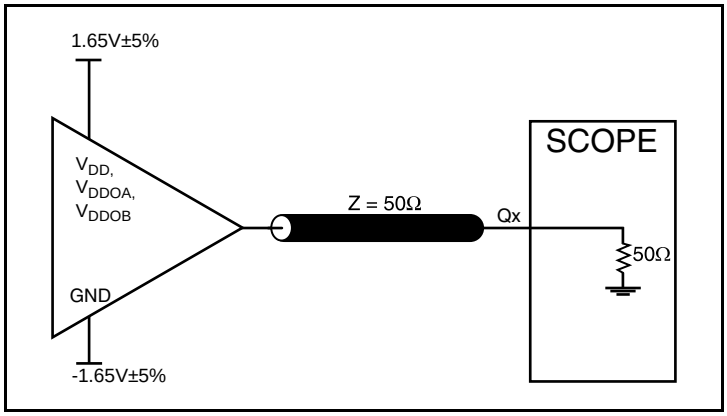
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crosspoint to $V_{DDOA, B}/2$ of the output.
NOTE 2: Defined as between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOA, B}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOA, B}/2$.
NOTE 5: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

Table 5C. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDOA} = V_{DDOB} = 2.5V ± 5%, T_A = 0°C to 70°C

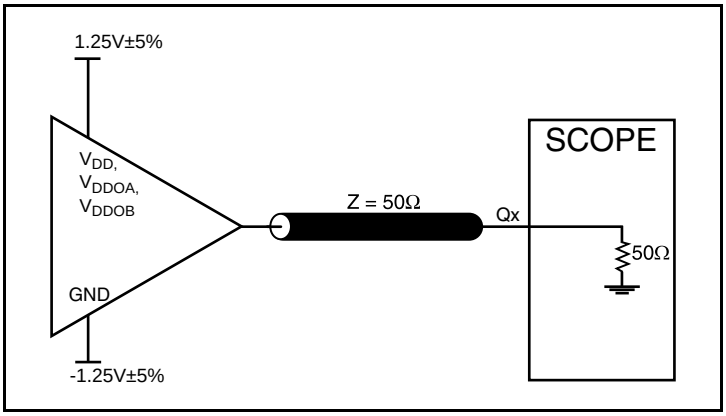
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{out}	Output Frequency					250	MHz
t_{PD}	Propagation Delay; NOTE 1			2.5		4.1	ns
*t*sk(o)	Output Skew; NOTE 2, 3					140	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					225	ps
*t*sk(b)	Bank Skew; NOTE 3, 5	QA[0:3], nQA[0:3]				70	ps
		QB[0:3], nQB[0:3]				60	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	150		600	ps
t_{EN}	Output Enable Time; NOTE 6					10	ns
t_{DIS}	Output Disable Time; NOTE 6					10	ns
odc	Output Duty Cycle			40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crosspoint to $V_{DDOA, B}$/2 of the output.
NOTE 2: Defined as between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOA, B}$/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOA, B}$/2.
NOTE 5: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

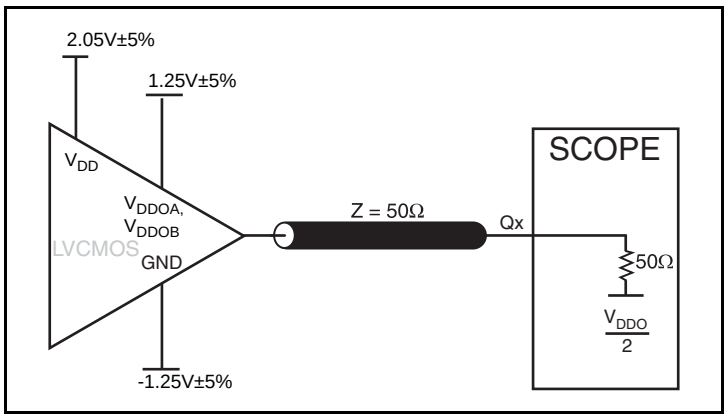
Parameter Measurement Information



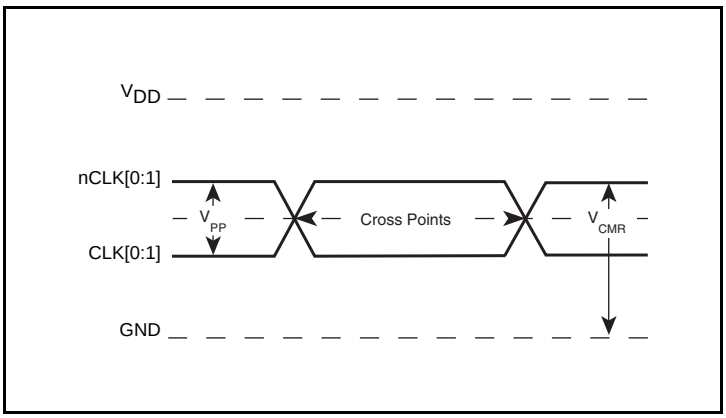
3.3V Output Load Test Circuit



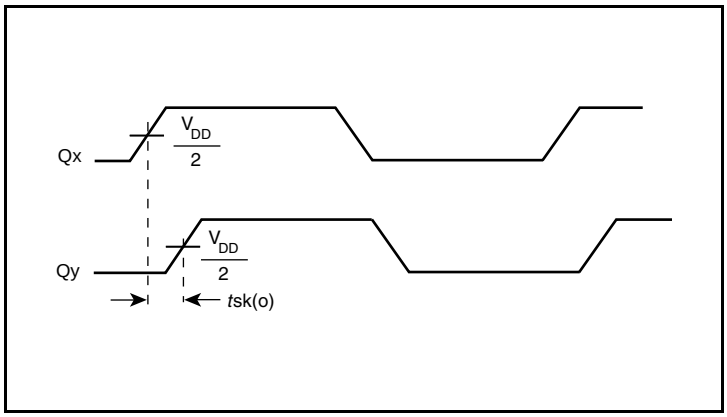
2.5V Output Load Test Circuit



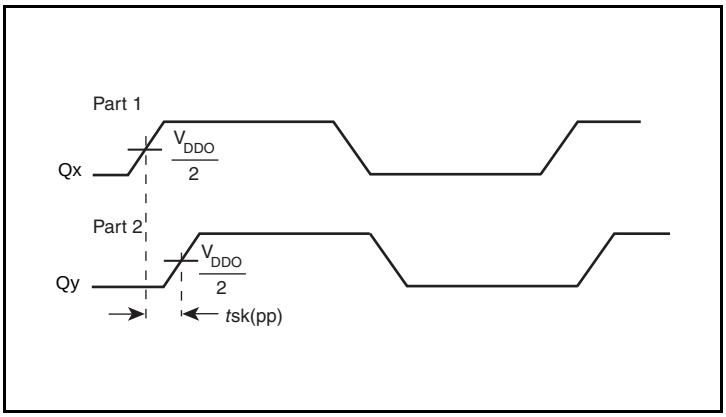
3.3V Core/2.5V Output Load Test Circuit



Differential Input Level

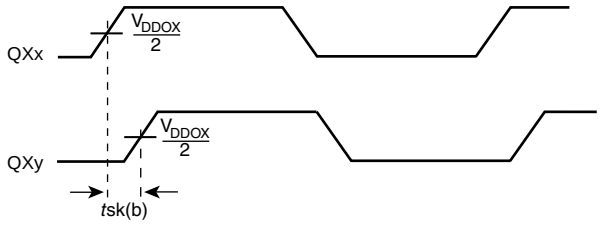


Output Skew



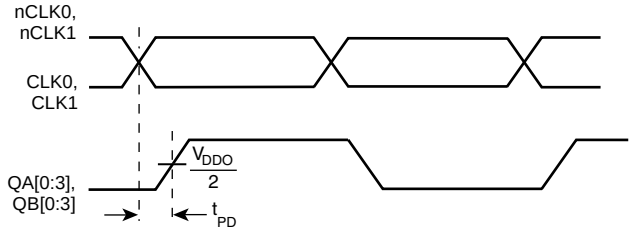
Part-to-Part Skew

Parameter Measurement Information, continued

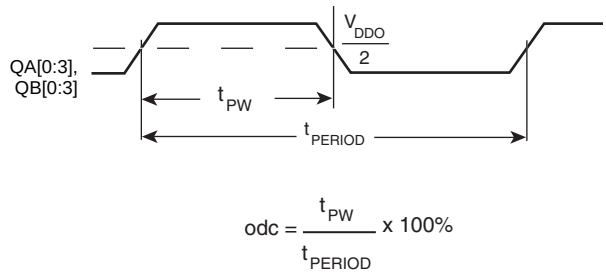


Where X denotes Bank A or Bank B outputs

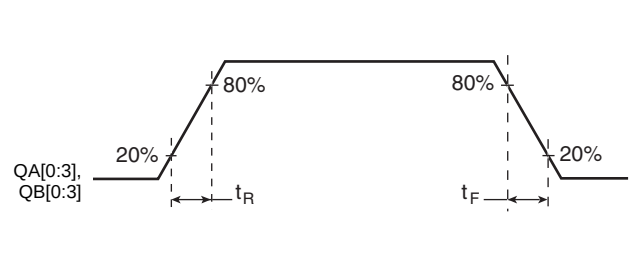
Bank Skew



Propagation Delay



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLKx and nCLKx can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

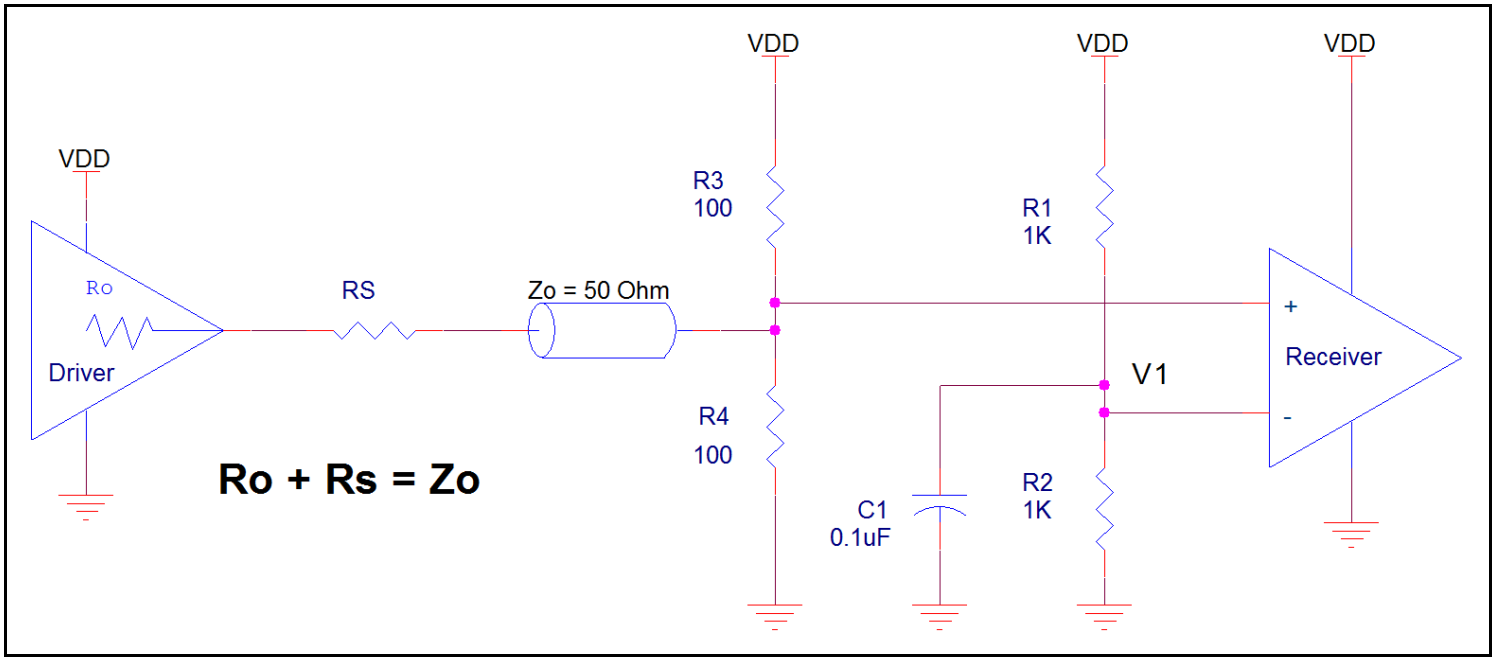


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLKx /nCLKx accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

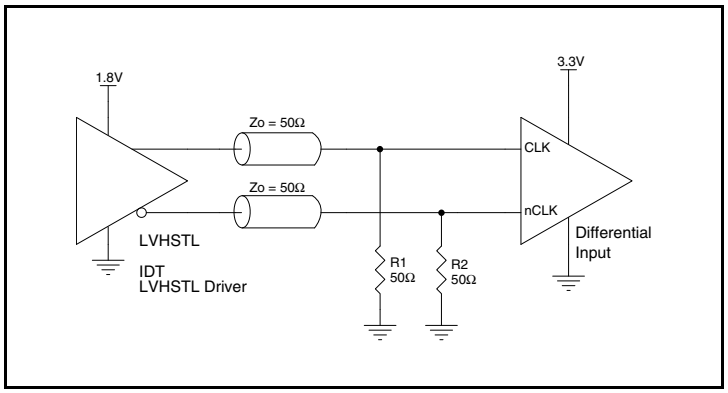


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

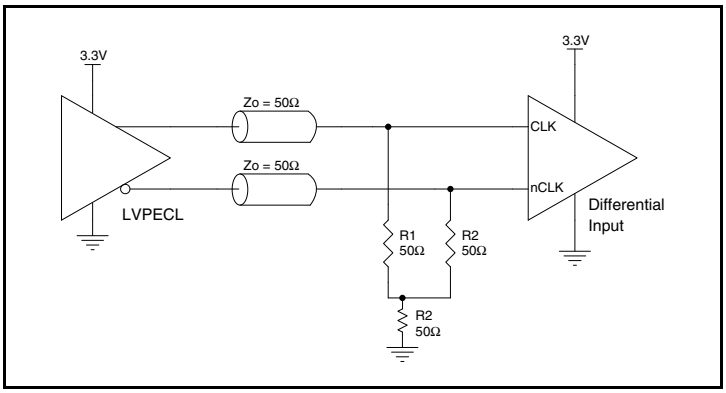


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

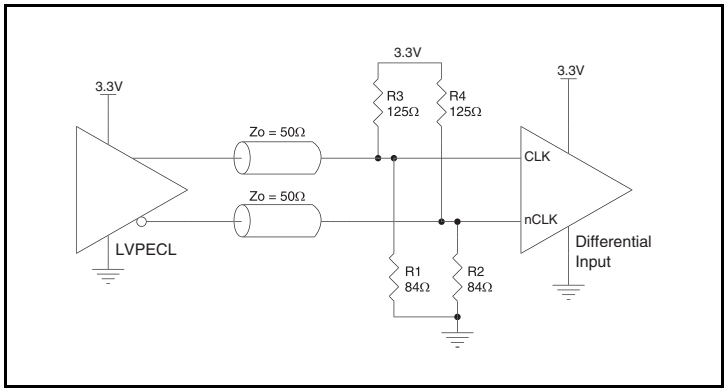


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

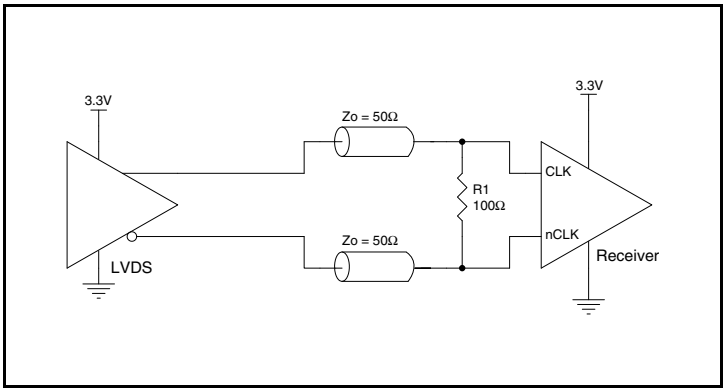


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

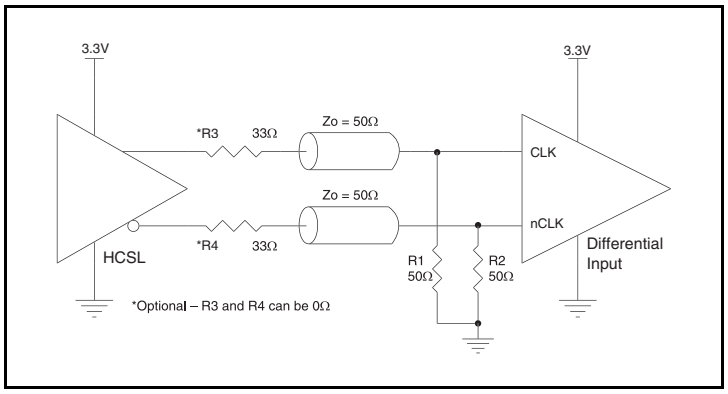


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

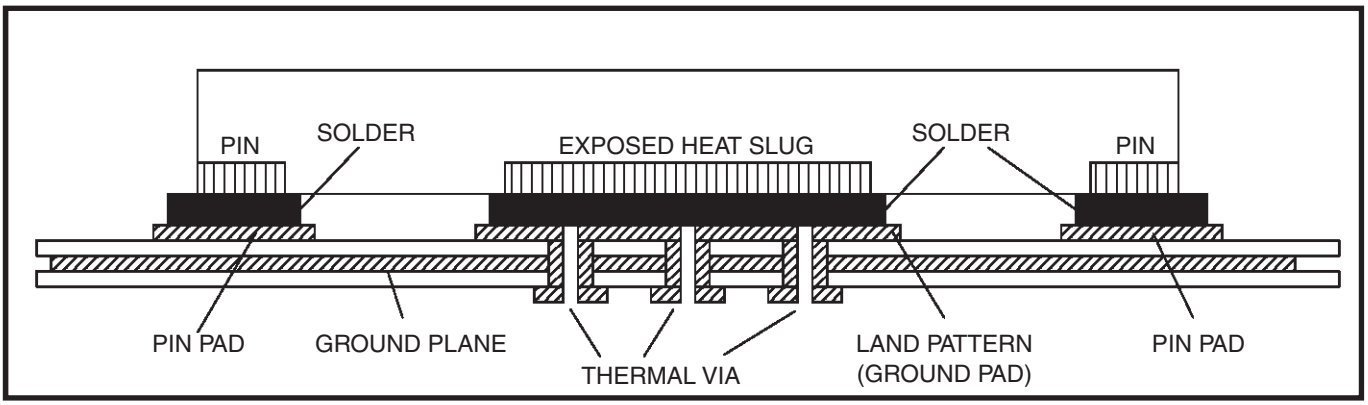


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS870S208.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS870S208 is the sum of the core power plus the analog power plus the power dissipated due to into the load. The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD}$ = 3.465V *80mA = **277.2mW**
- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD\_MAX} / [2 * (50Ω + R_{OUT})]$ = 3.465V / [2 * (50Ω + 15Ω)] = **26.7mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 15Ω * $(26.7mA)^2$ = **10.69mW per output**
- Total Power (R_{OUT}) = 10.69mW * 8 = **85.52mW**

Dynamic Power Dissipation at 250MHz

Power (250MHz) = C_{PD} * Frequency * $(V_{DD})^2$ = 8pF * 250MHz * $(3.465V)^2$ = **24mW per output**

Total Power (250MHz) = 24mW * 8 = **192mW**

Total Power Dissipation

- **Total Power**
  = Power $(core)_{MAX}$ + Power (R_{OUT}) + Power (250MHz)
  = 277.2mW + 85.52mW + 192mW
  = 554.72mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.555W *42.7°C/W = 93.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

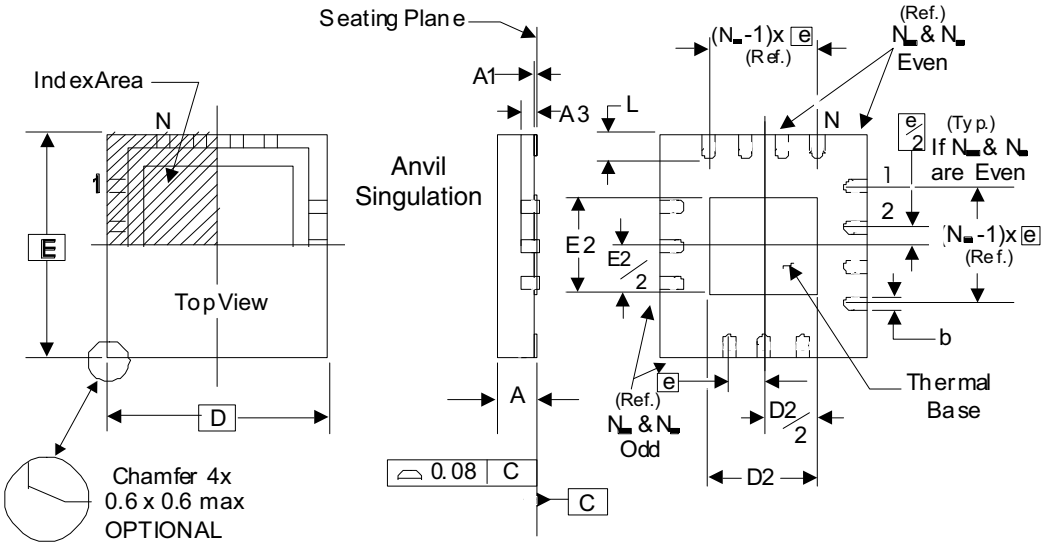
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

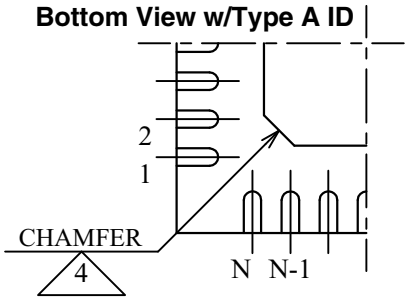
Transistor Count

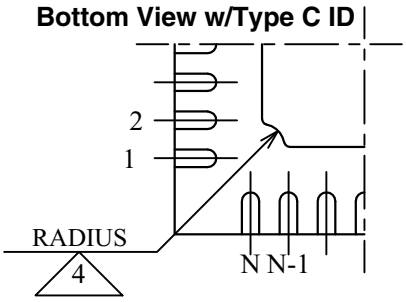
The transistor count for ICS870S208 is: 2788

Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 8. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pin-out are shown on the front page. The package dimensions are in Table 8.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
870S208BKLF	ICS870S208BL	“Lead-Free” 32 Lead VFQFN	Tray	0°C to 70°C
870S208BKLFT	ICS870S208BL	“Lead-Free” 32 Lead VFQFN	Tape & Reel	0°C to 70°C

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