

GENERAL DESCRIPTION

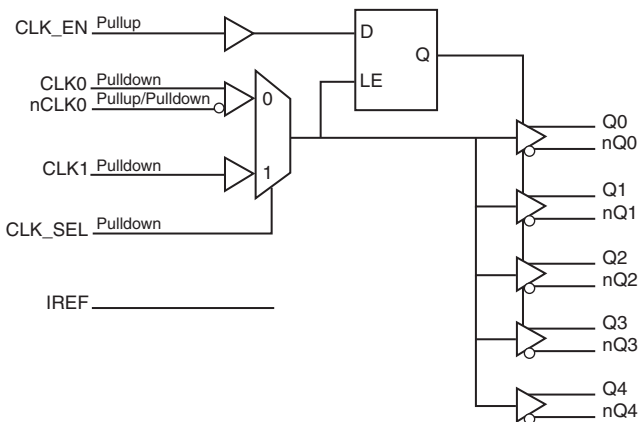
The 85105I is a low skew, high performance 1-to-5 Differential-to-0.7V HCSL Fanout Buffer. The 85105I has two selectable clock inputs. The CLK0, nCLK0 pair can accept most standard differential input levels. The single-ended CLK1 can accept LVCMOS or LVTTTL input levels. The clock enable is internally synchronized to eliminate runt clock pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the 85105I ideal for those applications demanding well defined performance and repeatability.

FEATURES

- Five 0.7V differential HCSL outputs
- Selectable differential CLK0, nCLK0 or LVCMOS inputs
- CLK0, nCLK0 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL
- CLK1 can accept the following input levels: LVCMOS or LVTTTL
- Maximum output frequency: 500MHz
- Translates any single-ended input signal to 3.3V HCSL levels with resistor bias on nCLK input
- Output skew: 100ps (maximum)
- Part-to-part skew: 600ps (maximum)
- Propagation delay: 3.2ns (maximum)
- Additive phase jitter, RMS: 0.24ps (typical)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

BLOCK DIAGRAM



PIN ASSIGNMENT

| | | | |
|-----------------|----|----|-----------------|
| GND | 1 | 20 | Q0 |
| CLK_EN | 2 | 19 | nQ0 |
| CLK_SEL | 3 | 18 | V _{DD} |
| CLK0 | 4 | 17 | Q1 |
| nCLK0 | 5 | 16 | nQ1 |
| CLK1 | 6 | 15 | Q2 |
| Q4 | 7 | 14 | nQ2 |
| nQ4 | 8 | 13 | V _{DD} |
| IREF | 9 | 12 | Q3 |
| V _{DD} | 10 | 11 | nQ3 |

85105I
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm Package Body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|------------|-----------------|--------|---------------------|--|
| 1 | GND | Power | | Power supply ground. |
| 2 | CLK_EN | Input | Pullup | Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Qx outputs are forced low, nQx outputs are forced high. LVTTTL / LVCMOS interface levels. |
| 3 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0, nCLK0 inputs. LVTTTL / LVCMOS interface levels. |
| 4 | CLK0 | Input | Pulldown | Non-inverting differential clock input. |
| 5 | nCLK0 | Input | Pullup/ Pulldown | Inverting differential clock input. |
| 6 | CLK1 | Input | Pulldown | Single-ended clock input. LVTTTL / LVCMOS interface levels. |
| 7, 8 | Q4, nQ4 | Output | | Differential output pair. HCSL interface levels. |
| 9 | IREF | Input | | An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode Qx, nQx outputs. |
| 10, 13, 18 | V _{DD} | Power | | Positive supply pins. |
| 11, 12 | nQ3, Q3 | Output | | Differential output pair. HCSL interface levels. |
| 14, 15 | nQ2, Q2 | Output | | Differential output pair. HCSL interface levels. |
| 16, 17 | nQ1, Q1 | Output | | Differential output pair. HCSL interface levels. |
| 19, 20 | nQ0, Q0 | Output | | Differential output pair. HCSL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

TABLE 3. CONTROL INPUT FUNCTION TABLE

| Inputs | | | Outputs | |
|--------|---------|-----------------|---------------|----------------|
| CLK_EN | CLK_SEL | Selected Source | Q0:Q4 | nQ0:nQ4 |
| 0 | 0 | CLK0, nCLK0 | Disabled; LOW | Disabled; HIGH |
| 0 | 1 | CLK1 | Disabled; LOW | Disabled; HIGH |
| 1 | 0 | CLK0, nCLK0 | Enabled | Enabled |
| 1 | 1 | CLK1 | Enabled | Enabled |

After CLK_EN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in Figure 1.



FIGURE 1. CLK_EN TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS

| | |
|---|--------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, I_O | -0.5V to $V_{DD} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} 20 Lead TSSOP | 91.1°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 10\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Positive Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| I_{DD} | Power Supply Current | Unterminated | | | 27 | mA |

TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 10\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|-----------------|-------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | CLK1, CLK_SEL | $V_{IN} = V_{DD} = 3.63V$ | | 150 | μA |
| | | CLK_EN | $V_{IN} = V_{DD} = 3.63V$ | | 5 | μA |
| I_{IL} | Input Low Current | CLK1, CLK_SEL | $V_{IN} = 0V, V_{DD} = 3.63V$ | -5 | | μA |
| | | CLK_EN | $V_{IN} = 0V, V_{DD} = 3.63V$ | -150 | | μA |

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 10\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------|-----------------|-------------------------------|---------|-----------------|---------|
| I_{IH} | Input High Current | CLK0, nCLK0 | $V_{DD} = V_{IN} = 3.63V$ | | 150 | μA |
| I_{IL} | Input Low Current | CLK0 | $V_{DD} = 3.63V, V_{IN} = 0V$ | -5 | | μA |
| | | nCLK0 | $V_{DD} = 3.63V, V_{IN} = 0V$ | -150 | | μA |
| V_{PP} | Peak-to-Peak Input Voltage; NOTE 1 | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | GND + 0.5 | | $V_{DD} - 0.85$ | V |

NOTE 1: V_{IL} should not be less than -0.3V.

NOTE 2: Common mode voltage is defined as V_{IH} .

TABLE 5. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 10\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---|-----------------------------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | CLK_SEL = 0 | | | 500 | MHz |
| | | CLK_SEL = 1 | | | 250 | MHz |
| t_{PD} | Propagation Delay; NOTE 1 | CLK_SEL = 0 | 2.0 | | 3.2 | ns |
| | | CLK_SEL = 1 | 2.0 | | 2.8 | ns |
| tsk(o) | Output Skew; NOTE 2, 4 | | | | 100 | ps |
| tsk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | 600 | ps |
| tjit | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 100MHz (12kHz - 20MHz) | | 0.24 | | ps |
| V_{MAX} | Absolute Maximum Output Voltage; NOTE 5, 10 | | | | 1150 | mV |
| V_{MIN} | Absolute Minimum Output Voltage; NOTE 5, 11 | | -300 | | | mV |
| V_{RB} | Ringback Voltage; NOTE 6, 13 | | -100 | | 100 | mV |
| t_{STABLE} | Time before V_{RB} is allowed; NOTE 6, 13 | | 500 | | | ps |
| V_{CROSS} | Absolute Crossing Voltage; NOTE 5, 8, 9 | | 250 | | 550 | mV |
| DV_{CROSS} | Total Variation of V_{CROSS} over all edges; NOTE 5, 8, 12 | | | | 140 | mV |
| | Rise/Fall Edge Rate; NOTE 6, 7 | Measured between -150mV to +150mV | 0.6 | | 5.5 | V/ns |
| odc | Output Duty Cycle; NOTE 14 | | 45 | | 55 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at $f_{out} \leq 250\text{MHz}$ unless noted otherwise.

NOTE 1: Measured from the $V_{DD}/2$ of the input to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Measurement taken from single-ended waveform.

NOTE 6: Measurement taken from differential waveform.

NOTE 7: Measured from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Parameter Measurement Information Section.

NOTE 8: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

See Parameter Measurement Information Section.

NOTE 9: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.

NOTE 10: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 11: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 12: Defined as the total variation of all crossing voltage of Rising Qx and Falling nQx. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.

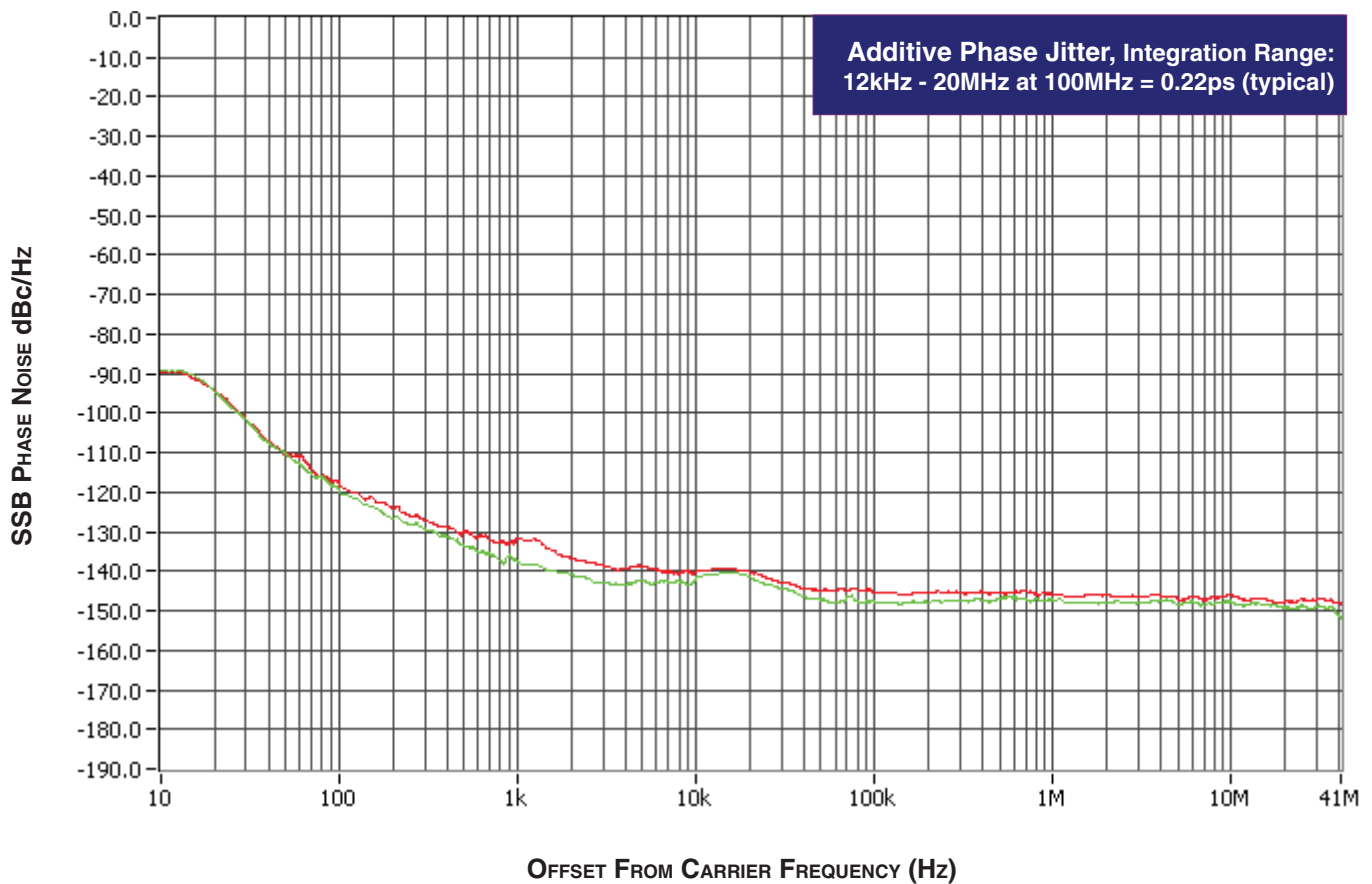
NOTE: 13. T_{STABLE} is the time the differential clock must maintain a minimum $\pm 150\text{mV}$ differential voltage after rising/falling edges before it is allowed to droop back into the $V_{RB} \pm 100\text{mV}$ differential range. See Parameter Measurement Information Section.

NOTE 14: Input duty cycle must be 50%.

ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels

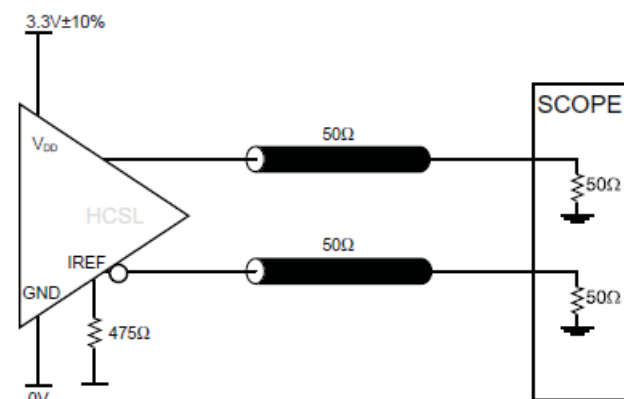
(dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device.

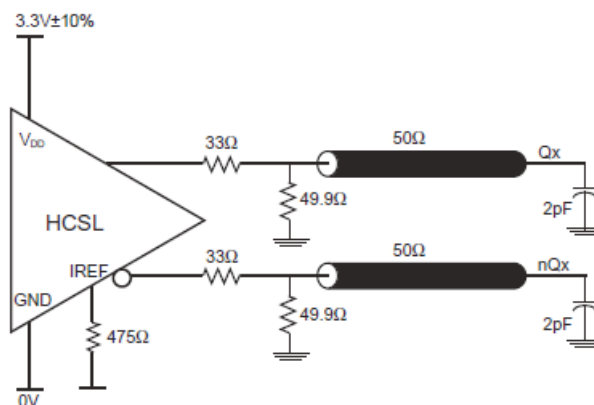
This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

PARAMETER MEASUREMENT INFORMATION

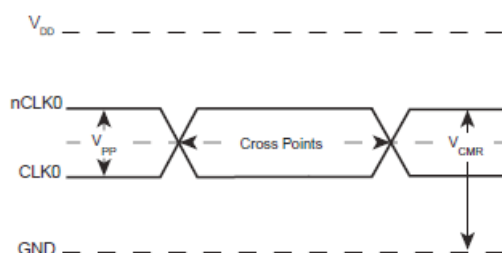


This load condition is used for I_{DD} , $t_{sk}(o)$, t_{pd} , and t_{jit} measurements.

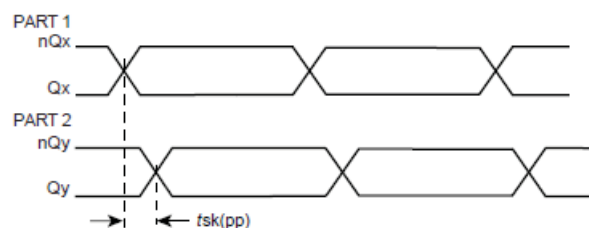
HCSSL OUTPUT LOAD AC TEST CIRCUIT



HCSSL OUTPUT LOAD AC TEST CIRCUIT



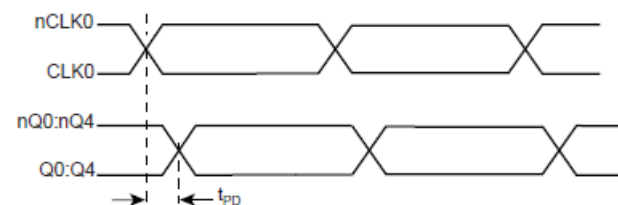
DIFFERENTIAL INPUT LEVELS



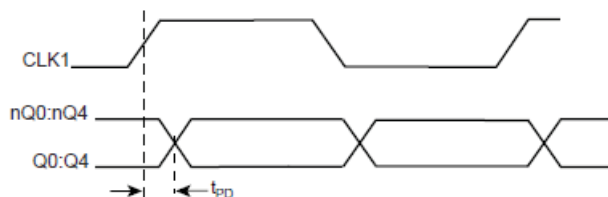
PART-TO-PART SKEW



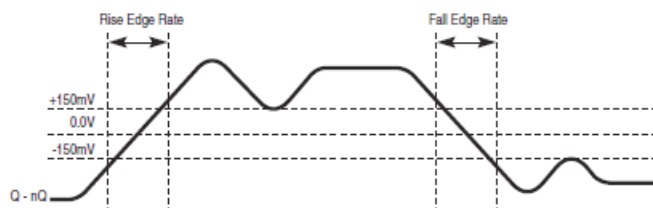
OUTPUT SKEW (DIFFERENTIAL INPUT)



PROPAGATION DELAY (DIFFERENTIAL INPUTS)

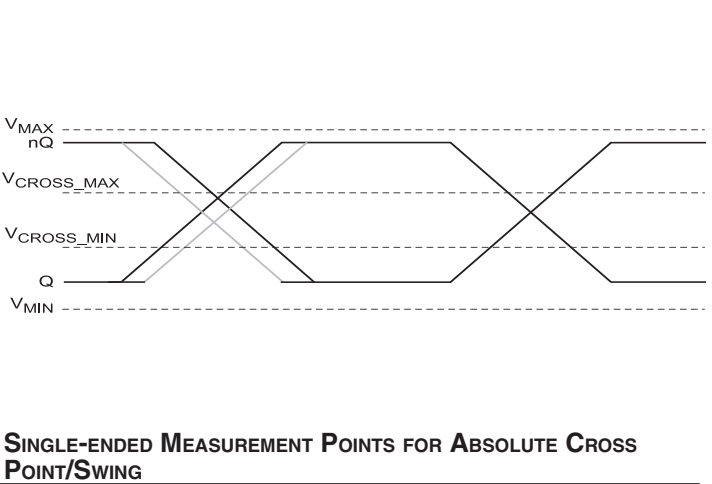
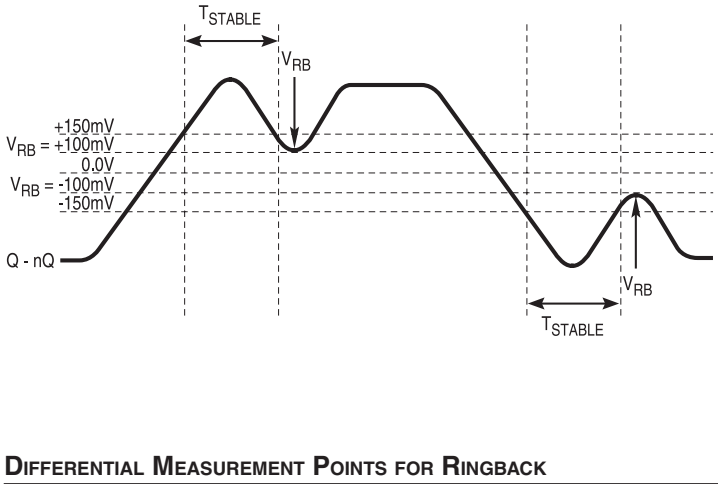
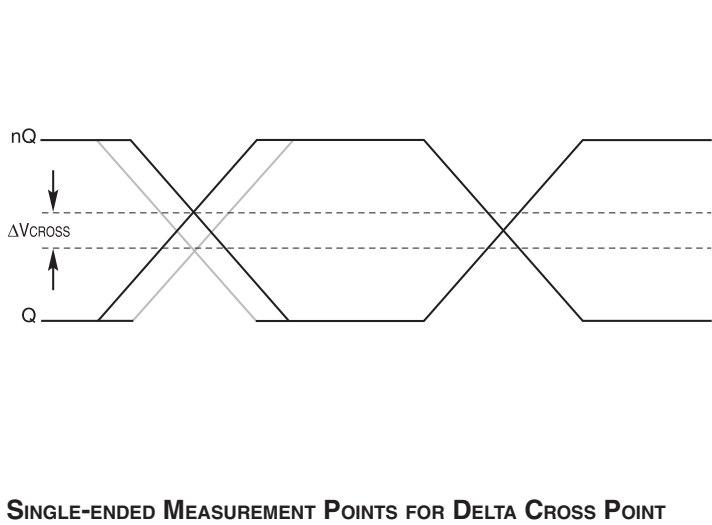
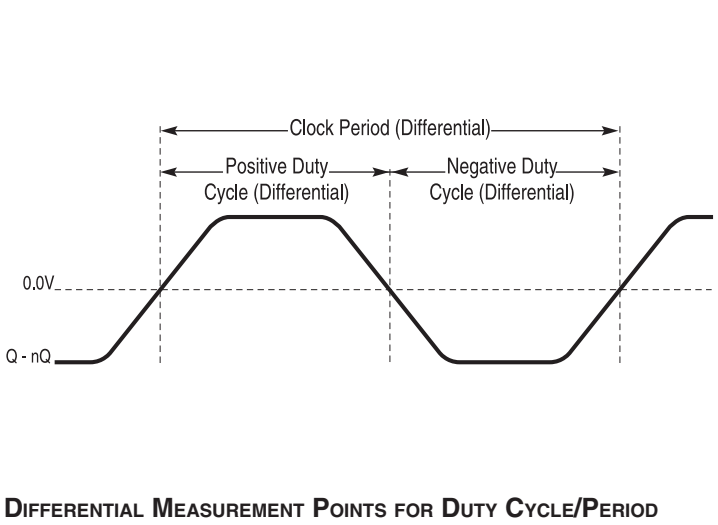


PROPAGATION DELAY (LVCMOS INPUT)



DIFFERENTIAL MEASUREMENT POINTS FOR RISE/FALL TIME

PARAMETER MEASUREMENT INFORMATION, CONTINUED



APPLICATIONS INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK INPUT

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from the CLK input to ground.

CLK/nCLK INPUTS

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from CLK to ground.

LVCN00 CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

OUTPUTS:

DIFFERENTIAL OUTPUTS

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{DD} = 3.3V$, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single-ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the

transmission line impedance. For most 50 applications, R3 and R4 can be 100 Ω . The values of the resistors can be increased to reduce the loading for slower and weaker LVCN00 driver. When using single ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCN00 signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_L cannot be less than -0.3V and V_H cannot be more than $V_{DD} + 0.3V$. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

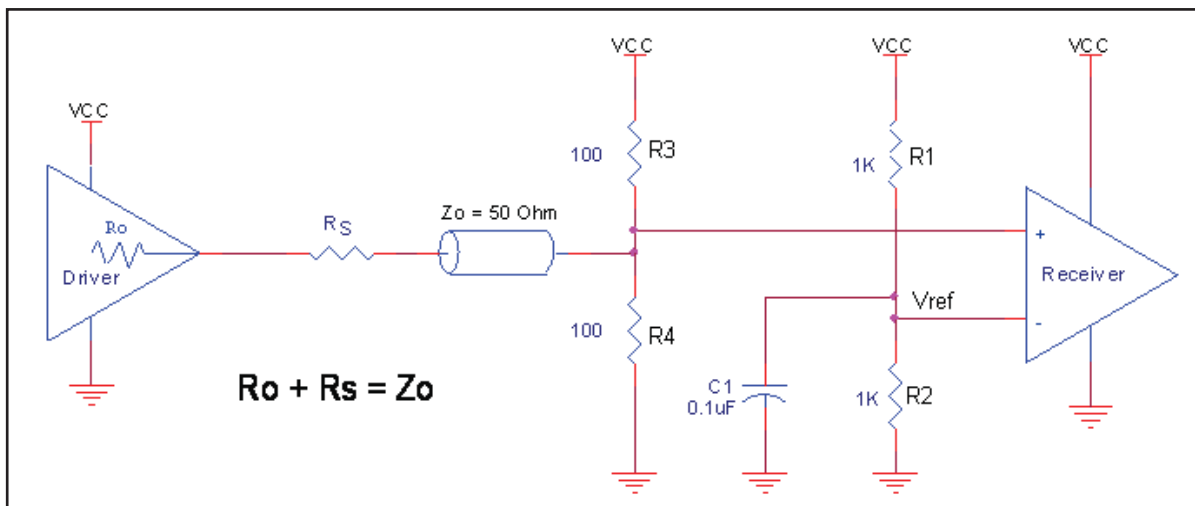


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please

consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination

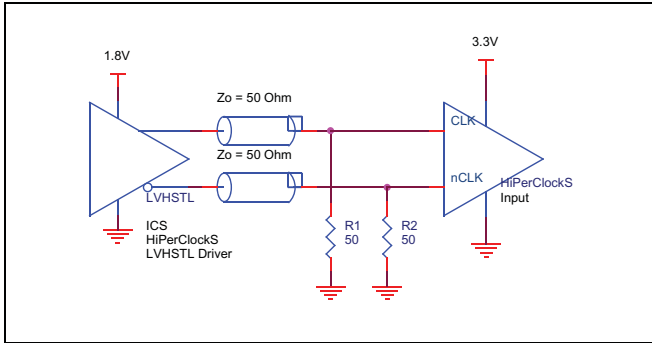


FIGURE 3A. CLK/nCLK INPUT DRIVEN BY AN IDT OPEN EMITTER LVHSTL DRIVER

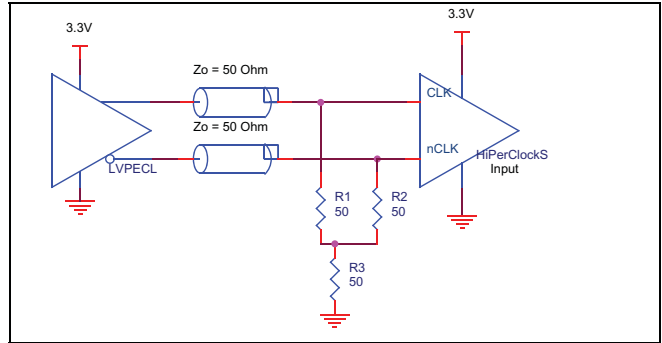


FIGURE 3B. CLK/nCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

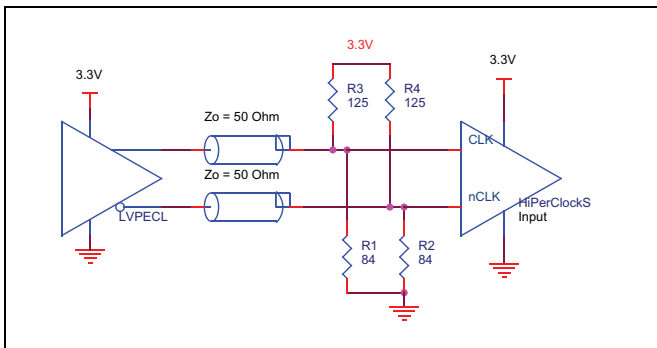


FIGURE 3C. CLK/nCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

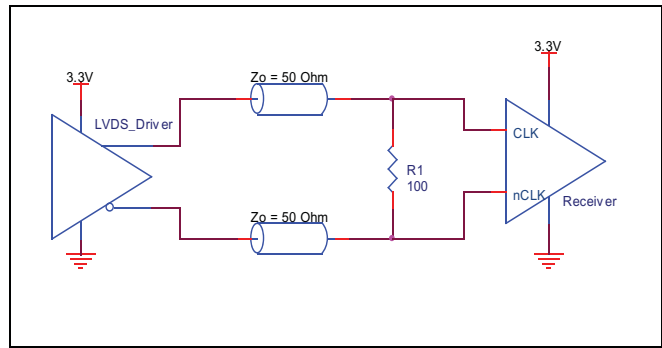


FIGURE 3D. CLK/nCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

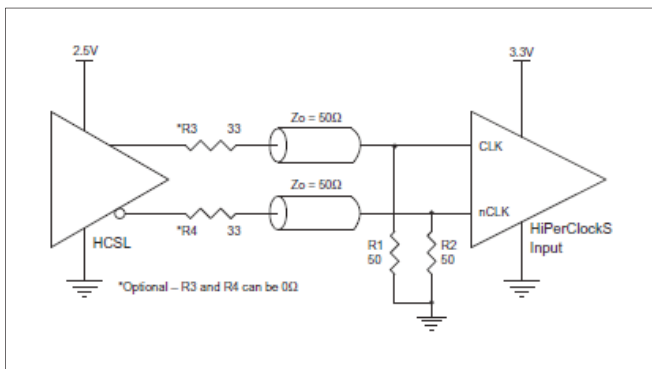


FIGURE 3E. CLK/nCLK INPUT DRIVEN BY A 3.3V HCSL DRIVER

RECOMMENDED TERMINATION

Figure 4A is the recommended source termination for applications where the driver and receiver will be on separate PCBs. This termination is the standard for PCI Express and

HCSL output types. All traces should be 50Ω impedance single ended or 100Ω differential.

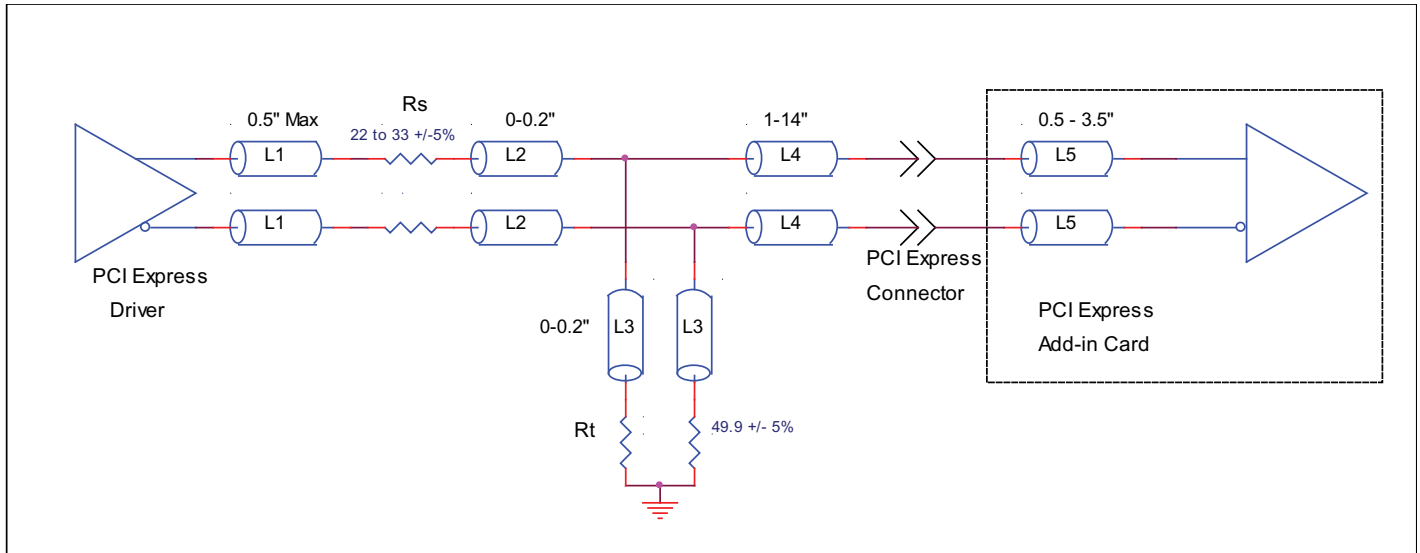


FIGURE 4A. RECOMMENDED TERMINATION

Figure 4B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor

(Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single ended or 100Ω differential.

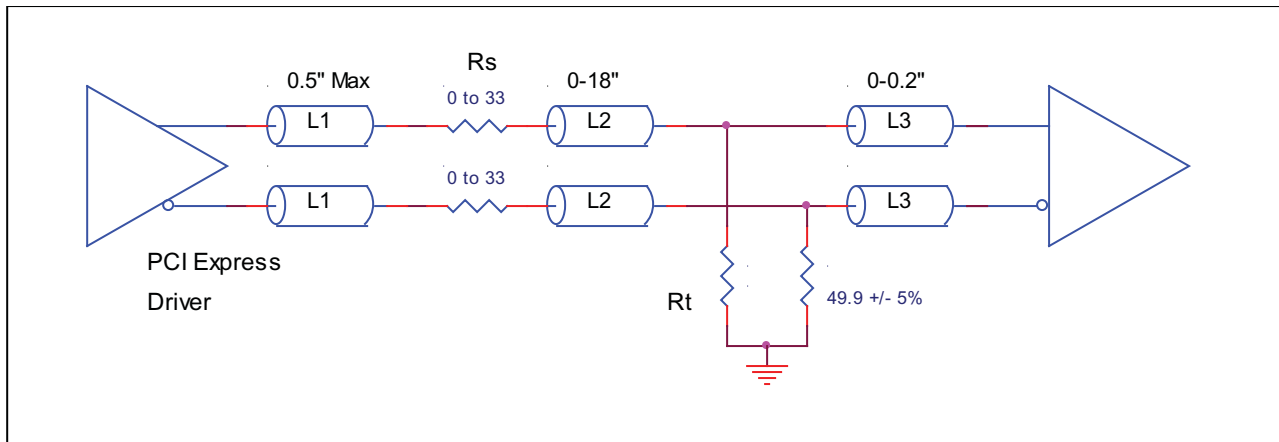


FIGURE 4B. RECOMMENDED TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 85105I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 85105I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 10\% = 3.63V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{DD_MAX} * I_{DD_MAX} = 3.63V * 27mA = 98.01mW$
- Power (outputs)_{MAX} = **47.3mW/Loaded Output pair**
If all outputs are loaded, the total power is $5 * 47.3mW = 236.5mW$

$$\text{Total Power}_{_MAX} \text{ (3.63V, with all outputs switching)} = 98.01mW + 236.5mW = 334.51mW$$

2. Junction Temperature.

Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in Section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 91.1°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:
 $85^\circ C + 0.335W * 91.1^\circ C/W = 115.5^\circ C$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-LEADN TSSOP, FORCED CONVECTION

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 91.1°C/W | 86.7°C/W | 84.6°C/W |

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 5*.

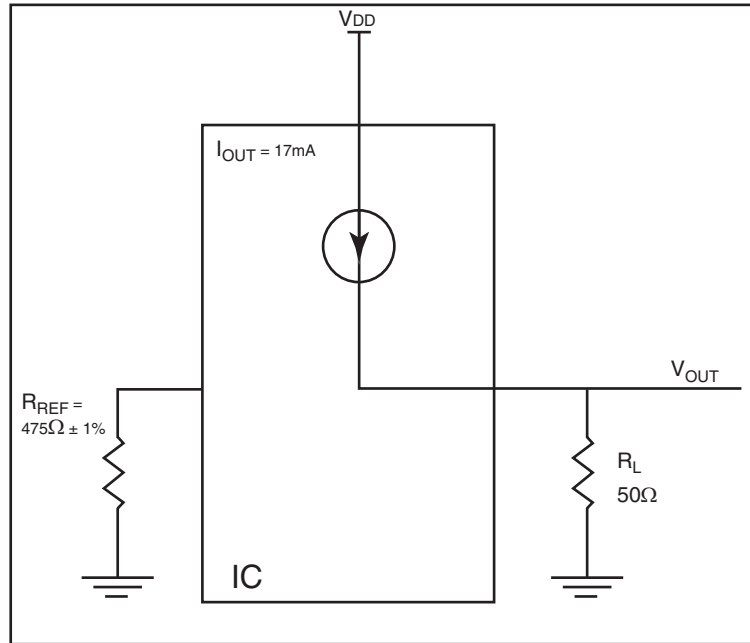


FIGURE 5. HCSL DRIVER CIRCUIT AND TERMINATION

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD} is HIGH.

$$\begin{aligned}
 \text{Power} &= (V_{DD_HIGH} - V_{OUT}) * I_{OUT}, \text{ since } V_{OUT} = I_{OUT} * R_L \\
 &= (V_{DD_HIGH} - I_{OUT} * R_L) * I_{OUT} \\
 &= (3.63V - 17mA * 50\Omega) * 17mA
 \end{aligned}$$

Total Power Dissipation per output pair = **47.3mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} vs. AIR FLOW TABLE FOR 20 LEAD TSSOP

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 91.1°C/W | 86.7°C/W | 84.6°C/W |

TRANSISTOR COUNT
The transistor count for 85105I is: 614

PACKAGE OUTLINE AND DIMENSIONS

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

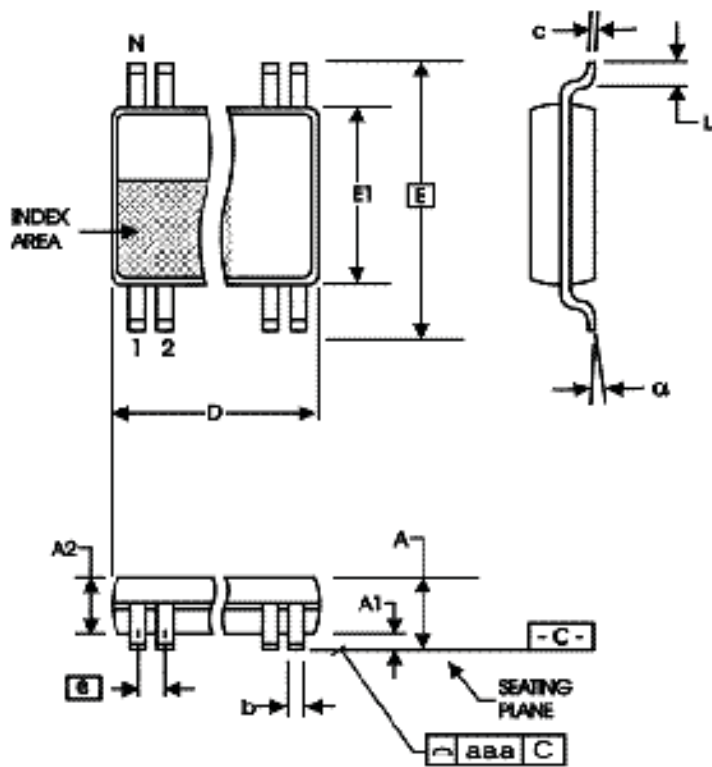


TABLE 8A. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | Minimum | Maximum |
| N | 20 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 6.40 | 6.60 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|--------------|---------------------------|--------------------|----------------|
| 85105AGILF | ICS85105AGIL | 20 lead "Lead Free" TSSOP | Tube | -40°C to +85°C |
| 85105AGILFT | ICS85105AGIL | 20 lead "Lead Free" TSSOP | Tape and Reel | -40°C to +85°C |

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