General Description

The 849S625 is a high frequency clock generator. The 849S625 uses an external 25MHz crystal to synthesize 625MHz, 312.5MHz, 156.25MHz and 125MHz clocks. The 849S625 has excellent cycle-to-cycle and RMS phase jitter performance.

The 849S625 operates at full 3.3V supply mode and is available in a fully RoHS compliant 48-lead TQFP, E-Pad package.

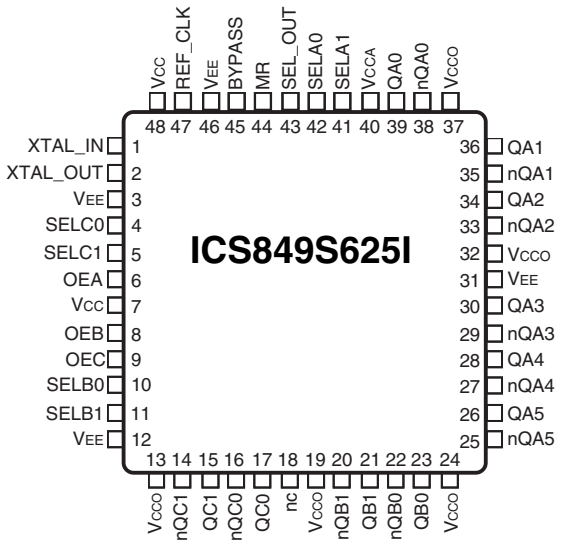
Features

- Ten selectable differential LVPECL or LVDS outputs
- Output frequencies of 625MHz, 312.5MHz, 156.25MHz or 125MHz using a 25MHz crystal.
- Crystal interface designed for a 25MHz, parallel resonant crystal
- Cycle-to-cycle jitter: 25ps (maximum)
- RMS phase jitter at 156.25MHz (1MHz - 20MHz): 0.375ps (typical), LVDS outputs
- Output duty cycle: 53% (maximum)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging

Frequency Table for Bank A, B and C Outputs

Crystal Frequency (MHz)	M Feedback Divider	VCO Frequency (MHz)	Nx Output Divider	Output Frequency (MHz)
25	25	625	1	625
25	25	625	2	312.5
25	25	625	4	156.25
25	25	625	5	125

Pin Assignment



48 Lead TQFP, E-Pad
7mm x 7mm x 1.0mm package body
Y Package
Top View

Block Diagram

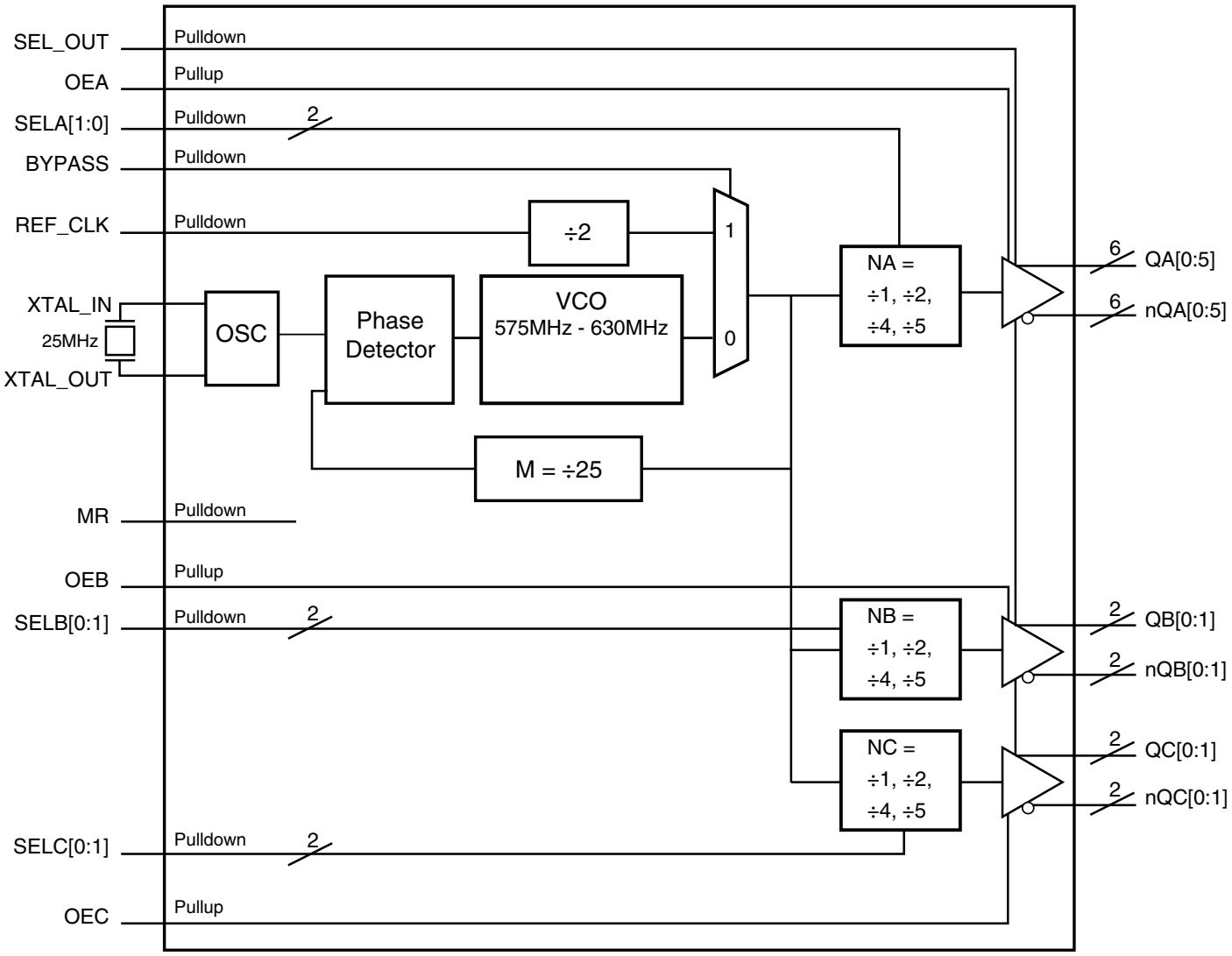


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	XTAL_IN XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
3, 12, 31, 46	V_{EE}	Power		Negative supply pins.
4, 5	SELC0, SELC1	Input	Pulldown	Selects the output divider value. See Table 3D. LVCMOS/LVTTL interface levels.
6	OEA	Input	Pullup	Active high output enable. When logic HIGH, Bank A outputs are enabled and active. When logic LOW, the outputs are disabled and forced to HIGH/LOW. LVCMOS/LVTTL interface levels.
7, 48	V_{CC}	Power		Core supply pins.
8	OEB	Input	Pullup	Active high output enable. When logic HIGH, Bank B outputs are enabled and active. When logic LOW, the outputs are disabled and forced to HIGH/LOW. LVCMOS/LVTTL interface levels.
9	OEC	Input	Pullup	Active high output enable. When logic HIGH, Bank C outputs are enabled and active. When logic LOW, the outputs are disabled and forced to HIGH/LOW. LVCMOS/LVTTL interface levels.
10, 11	SELB0, SELB1	Input	Pulldown	Selects the output divider value. See Table 3C. LVCMOS/LVTTL interface levels.
13, 19, 24, 32, 37	V_{CCO}	Power		Output supply pins.
14, 15	nQC1, QC1	Output		Differential output pair. LVPECL or LVDS interface levels.
16, 17	nQC0, QC0	Output		Differential output pair. LVPECL or LVDS interface levels.
18	nc	Unused		No connect.
20, 21	nQB1, QB1	Output		Differential output pair. LVPECL or LVDS interface levels.
22, 23	nQB0, QB0	Output		Differential output pair. LVPECL or LVDS interface levels.
25, 26	nQA5, QA5	Output		Differential output pair. LVPECL or LVDS interface levels.
27, 28	nQA4, QA4	Output		Differential output pair. LVPECL or LVDS interface levels.
29, 30	nQA3, QA3	Output		Differential output pair. LVPECL or LVDS interface levels.
33, 34	nQA2, QA2	Output		Differential output pair. LVPECL or LVDS interface levels.
35, 36	nQA1, QA1	Output		Differential output pair. LVPECL or LVDS interface levels.
38, 39	nQA0, QA0	Output		Differential output pair. LVPECL or LVDS interface levels.
40	V_{CCA}	Power		Analog supply pin.
41, 42	SELA1, SELA0	Input	Pulldown	Selects the output divider value. See Table 3B. LVCMOS/LVTTL interface levels.
43	SEL_OUT	Input	Pulldown	Selects between either LVDS or LVPECL output levels. See Table 3A. LVCMOS/LVTTL interface levels.
44	MR	Input	Pulldown	Master Reset. LVCMOS/LVTTL interface levels.
45	BYPASS	Input	Pulldown	PLL BYPASS mode select pin. See Table 3F. LVCMOS/LVTTL interface levels.
47	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulludown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. SEL_OUT Function Table

Input	
SEL_OUT	Output Levels
0 (default)	LVDS
1	LVPECL

Table 3E. MR Function Table

Input	
MR	Device Function
0 (default)	Normal
1	Master Reset

Table 3B. SELA Function Table

Inputs		NA
SELA0	SELA1	Bank A Output Divider
0 (default)	0 (default)	÷1
0	1	÷2
1	0	÷4
1	1	÷5

Table 3F. BYPASS Function Table

Input	
BYPASS	Device Function
0 (default)	PLL mode. The output frequency is the VCO frequency divided by the selected output divider.
1	Bypass mode. The output frequency is the REF_CLK frequency divided by two and then divided by the selected output divider.

Table 3C. SELB Function Table

Inputs		NB
SELB0	SELB1	Bank B Output Divider
0 (default)	0 (default)	÷1
0	1	÷2
1	0	÷4
1	1	÷5

Table 3D. SELC Function Table

Inputs		NC
SELC0	SELC1	Bank C Output Divider
0 (default)	0 (default)	÷1
0	1	÷2
1	0	÷4
1	1	÷5

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{CC} -0.5V to V_{CC} + 0.5V
Outputs, LVPECL I_O Continuos Current Surge Current Outputs, LVDS I_O Continuos Current Surge Current	 50mA 100mA 10mA 15mA
Package Thermal Impedance, θ_{JA}	33.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.16	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current				107	mA
I_{CCA}	Analog Supply Current				16	mA
I_{CCO}	Output Supply Current				228	mA

NOTE: Outputs configured as LVDS (SEL_OUT = 0).
NOTE: For the Power Supply Voltage Sequence Information, see Applications Information section.

Table 4B. LVPECL Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.16	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				181	mA
I_{CCA}	Analog Supply Current				16	mA

NOTE: Outputs configured as LVPECL (SEL_OUT = 1).
NOTE: For the Power Supply Voltage Sequence Information, see Applications Information section.

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{CC} = 3.3V$	2.2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{CC} = 3.3V$	-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK, BYPASS, MR, SELA[1:0], SELB[1:0], SELC[1:0], SEL_OUT	$V_{CC} = V_{IN} = 3.465V$			150	µA
		OEA, OEB, OEC	$V_{CC} = V_{IN} = 3.465V$			10	µA
I_{IL}	Input Low Current	REF_CLK, BYPASS, MR, SELA[1:0], SELB[1:0], SELC[1:0], SEL_OUT	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-10			µA
		OEA, OEB, OEC	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage		$V_{CCO} - 1.2$		$V_{CCO} - 0.7$	V
V_{OL}	Output Low Voltage		$V_{CCO} - 2.0$		$V_{CCO} - 1.5$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

Table 4E. LVDS DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		268		475	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 5A. LVPECL AC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Qx = ÷1	575	625	630	MHz
		Qx = ÷2	287.5	312.5	315	MHz
		Qx = ÷4	143.75	156.25	157.5	MHz
		Qx = ÷5	115	125	126	MHz
tjit(Ø)	RMS Phase Jitter (Random); NOTE 1	156.25MHz, Integration Range: (1MHz – 20MHz)		0.373	0.422	ps
		156.25MHz, Integration Range: (12kHz – 20MHz)		0.694	1.04	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 2				25	ps
t_R / t_F	Output Rise/Fall Time	10% to 90%	65	180	350	ps
odc	Output Duty Cycle		47		53	%
t_{LOCK}	PLL Lock Time				130	ms

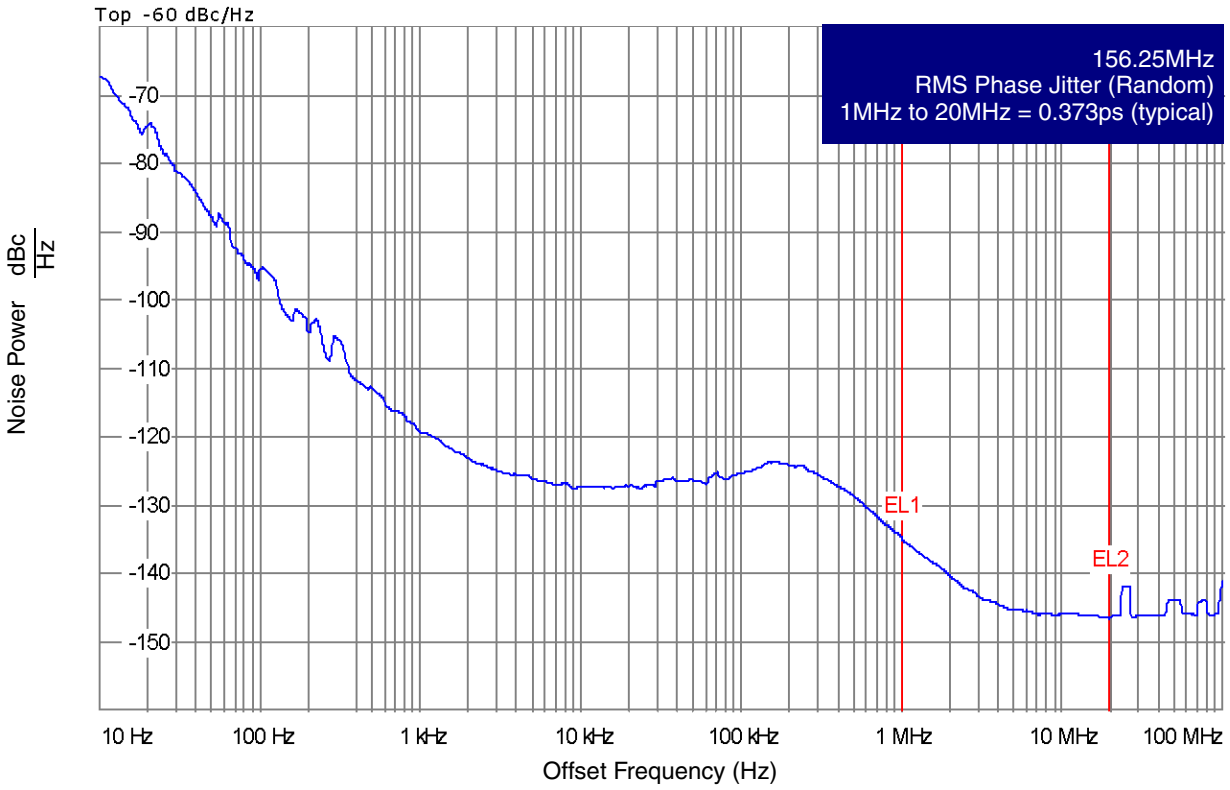
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Outputs configured as LVPECL (SEL_OUT = 1).
NOTE 1: Refer to the Phase Noise Plot.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. LVDS AC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

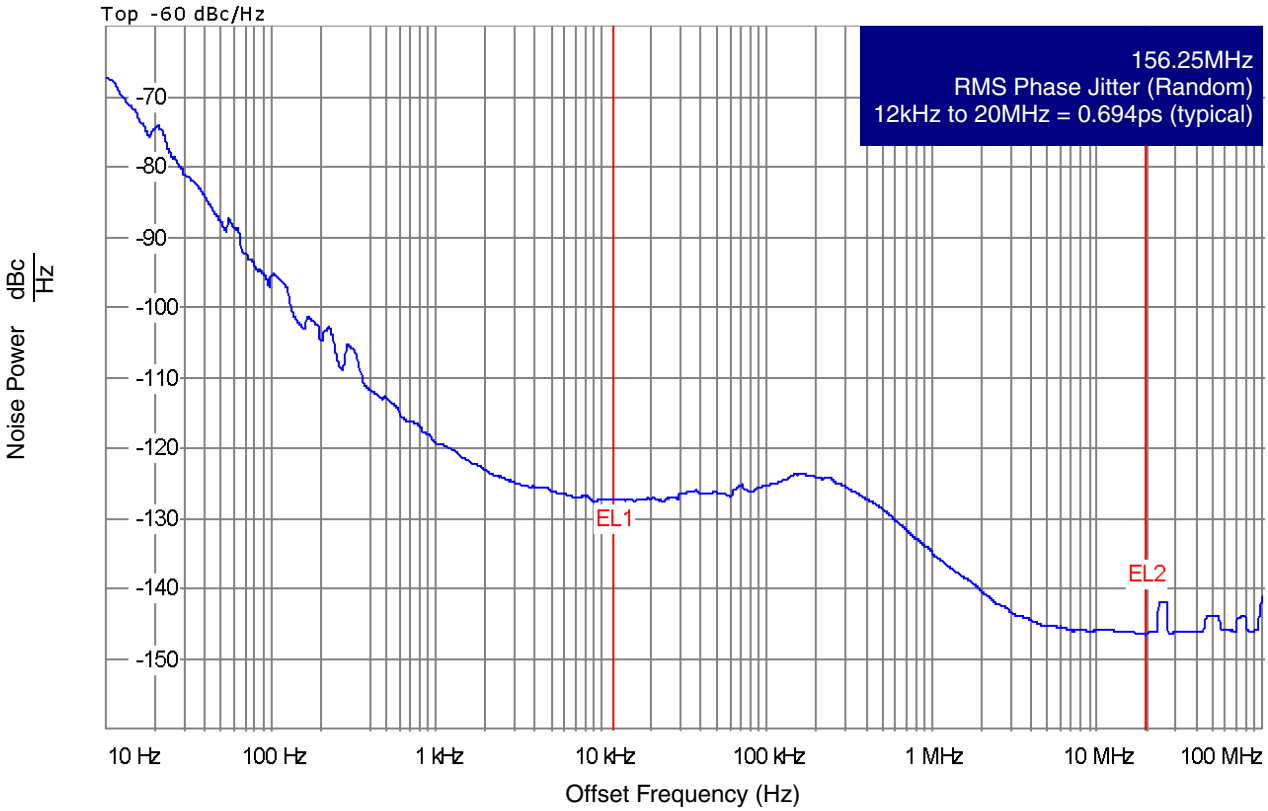
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Qx = ÷1	575	625	630	MHz
		Qx = ÷2	287.5	312.5	315	MHz
		Qx = ÷4	143.75	156.25	157.5	MHz
		Qx = ÷5	115	125	126	MHz
tjit(Ø)	RMS Phase Jitter (Random); NOTE 1	156.25MHz, Integration Range: (1MHz – 20MHz)		0.375	0.413	ps
		156.25MHz, Integration Range: (12kHz – 20MHz)		0.712	1.26	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 2				20	ps
t_R / t_F	Output Rise/Fall Time	10% to 90%	65	190	350	ps
odc	Output Duty Cycle		47		53	%
t_{LOCK}	PLL Lock Time				130	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Outputs configured as LVDS (SEL_OUT = 0).
NOTE 1: Refer to the Phase Noise Plot.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

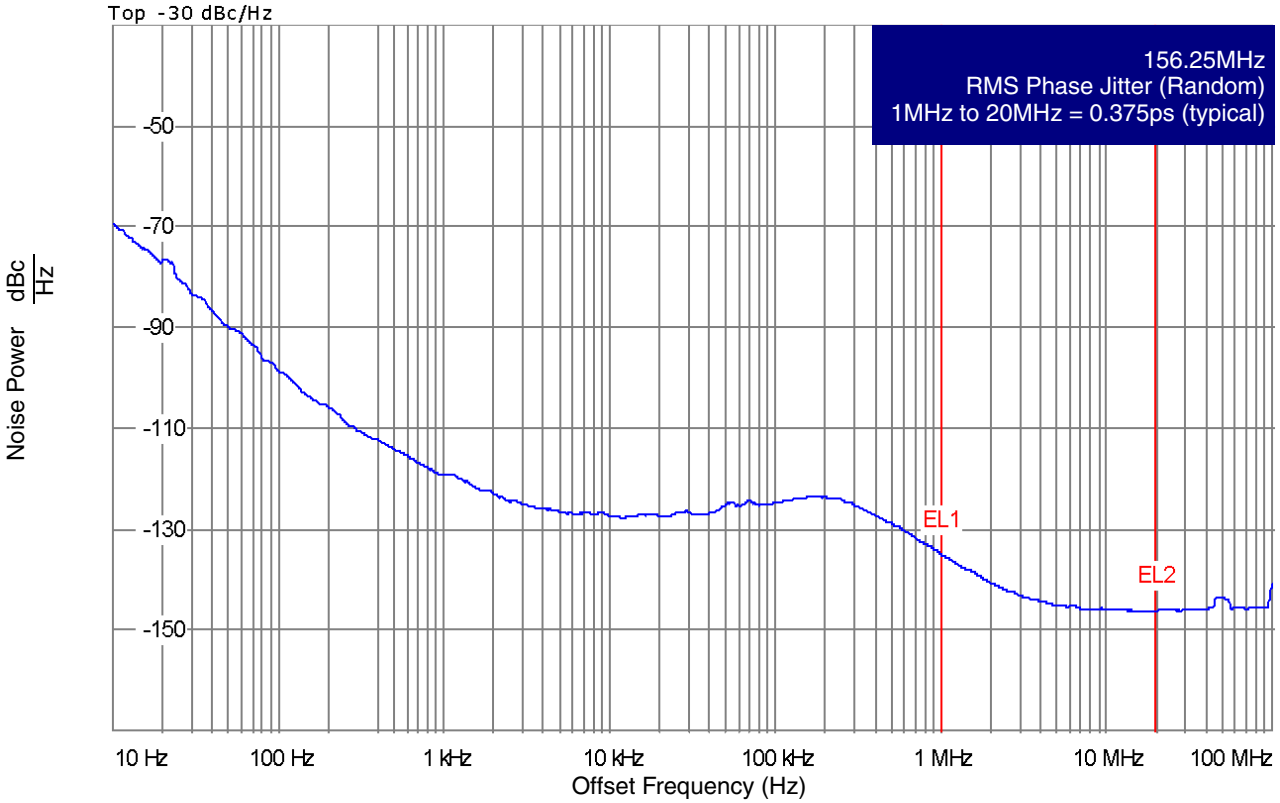
Typical Phase Noise at 156.25MHz (LVPECL)



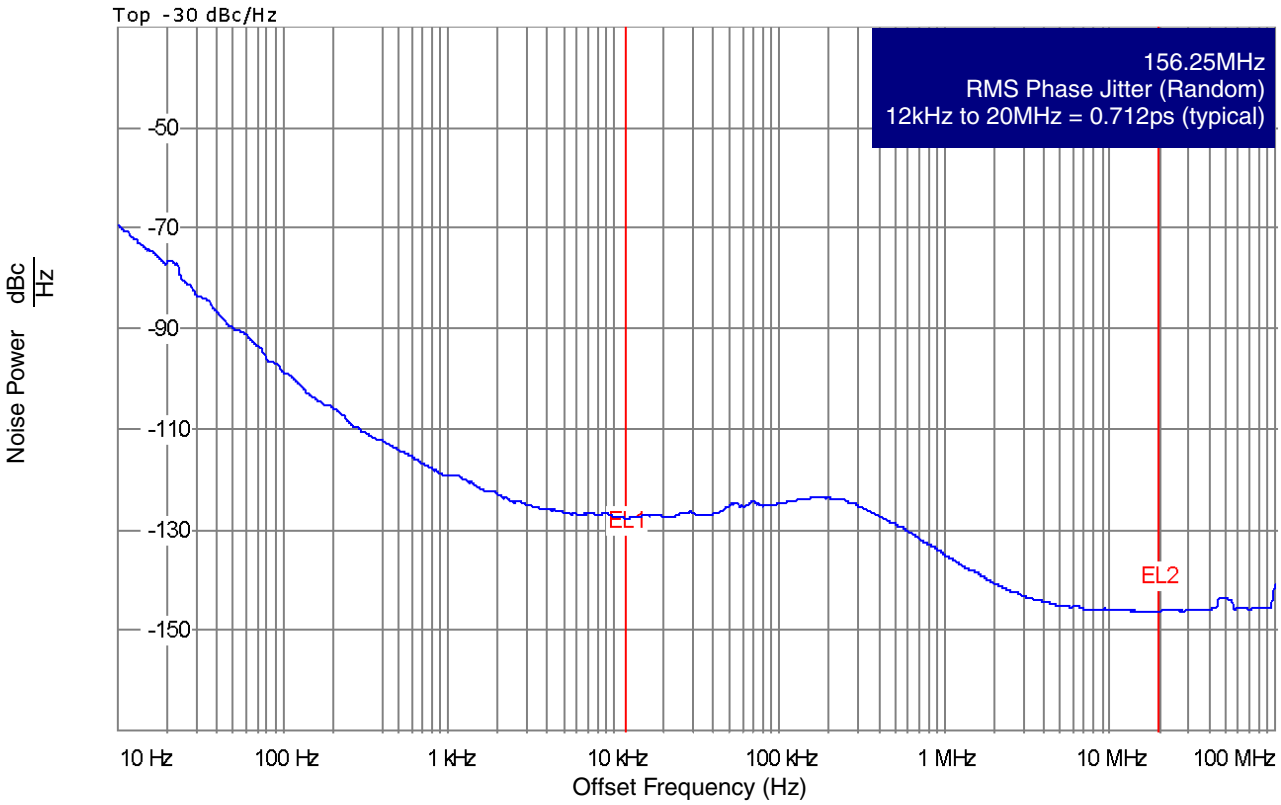
Typical Phase Noise at 156.25MHz (LVPECL)



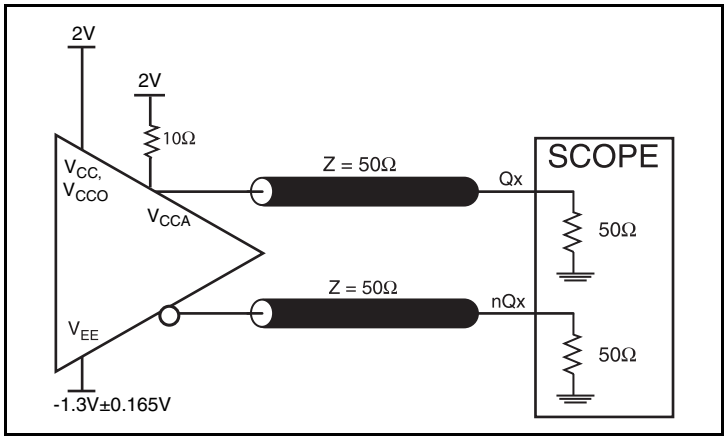
Typical Phase Noise at 156.25MHz (LVDS)



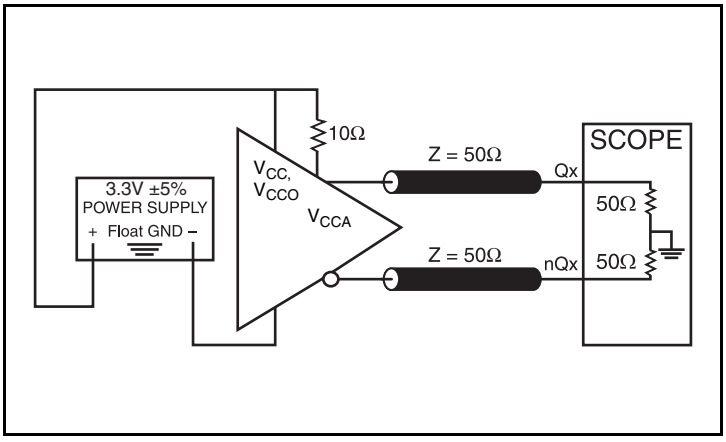
Typical Phase Noise at 156.25MHz (LVDS)



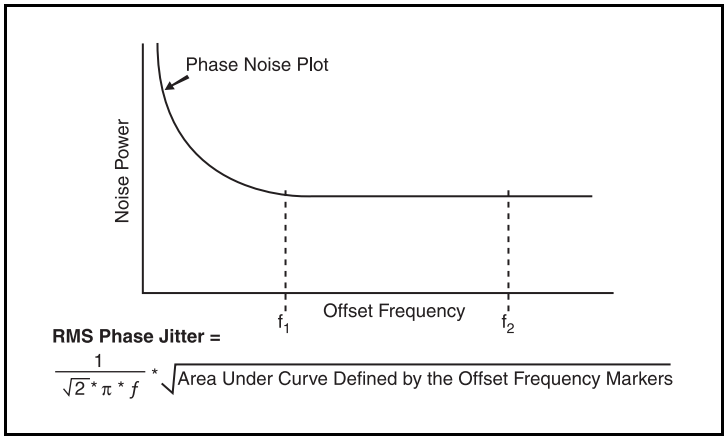
Parameter Measurement Information



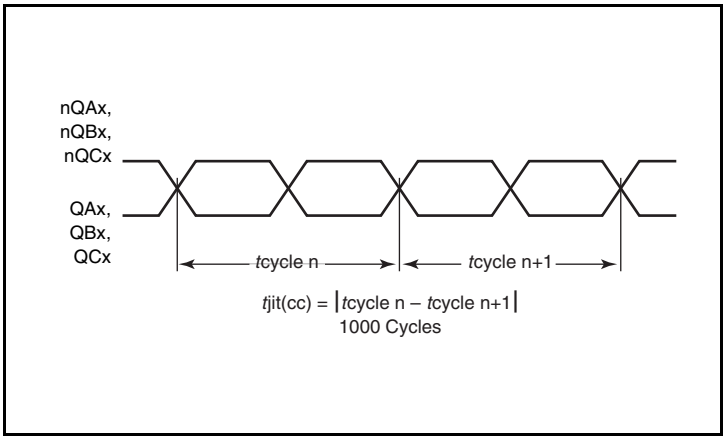
LVPECL Output Load AC Test Circuit



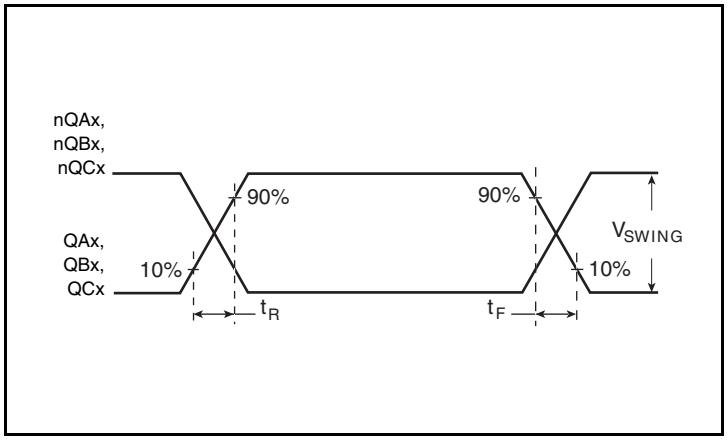
LVDS Output Load AC Test Circuit



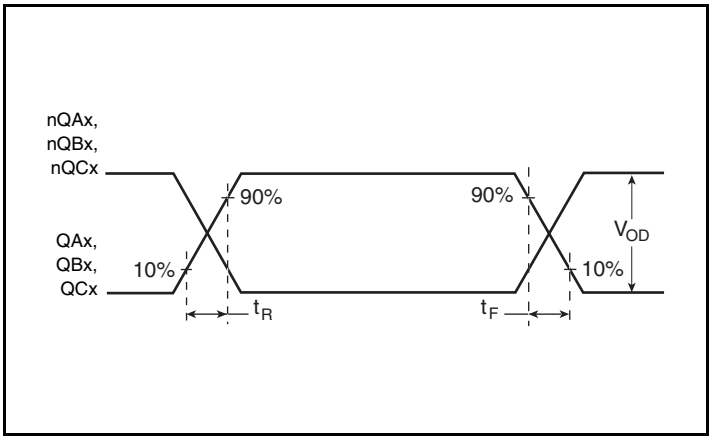
RMS Phase Jitter



Cycle-to-Cycle Jitter

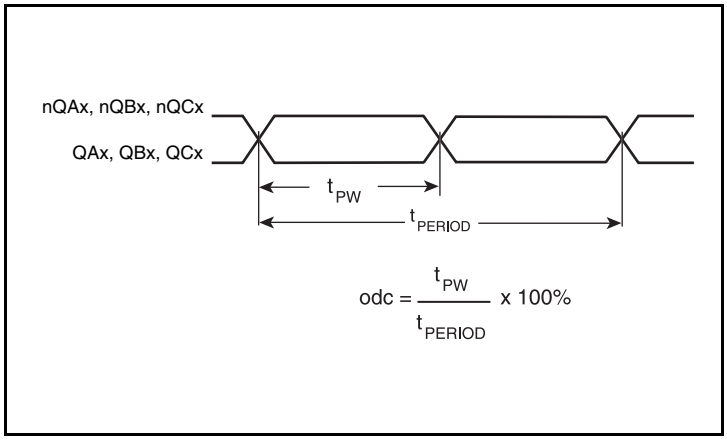


LVPECL Output Rise/Fall Time

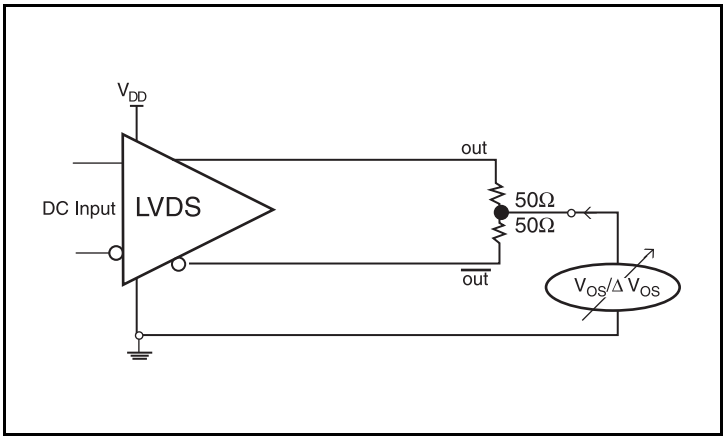


LVDS Output Rise/Fall Time

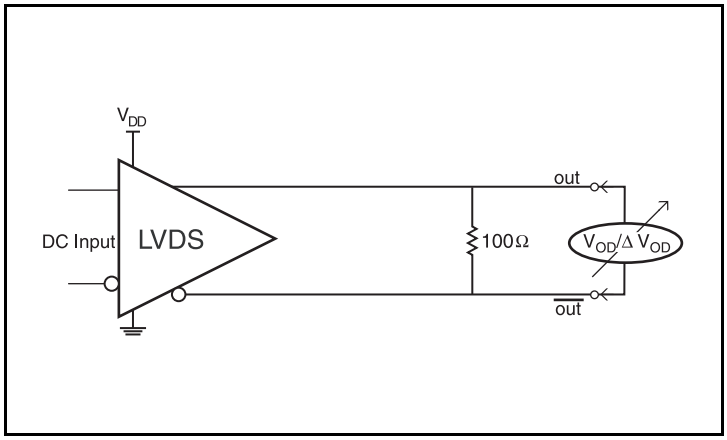
Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period



Offset Voltage Setup



Differential Output Voltage Setup

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Table 6. Recommended Crystal Specifications

Symbol	Parameter	Value
	Crystal Cut	Fundamental at Cut
	Resonance	Parallel Resonance
f_T	Frequency Tolerance	±25ppm at 25^0C
f_S	Frequency Stability	±25ppm over -40^0C to $+85^0$C
C_L	Load Capacitance	18pF
C_O	Shunt Capacitance	5pF - 7pF
ESR	Equivalent Series Resistance	20Ω - 50Ω
	Aging @ 25 ^{0}C	±15ppm/10 Years Maximum

NOTE: External tuning capacitors must be used for proper operation.

Power Supply Voltage Sequence Information

No power sequence restrictions apply if V_{CC} and V_{CCA} are supplied by the same power plane and the recommended V_{CCA} filter is used (see Figure 6). V_{CCO} may be applied at any time before or after V_{CC} and V_{CCA} are applied. If V_{CC} and V_{CCA} are not supplied by the same power plane, V_{CCA} must be powered on before or at the same time V_{CC} is applied. The V_{CCO} supply voltage may be applied at any time.

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 1A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

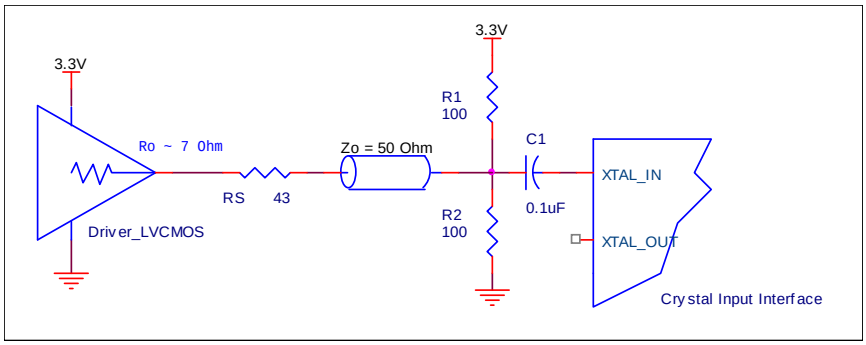


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

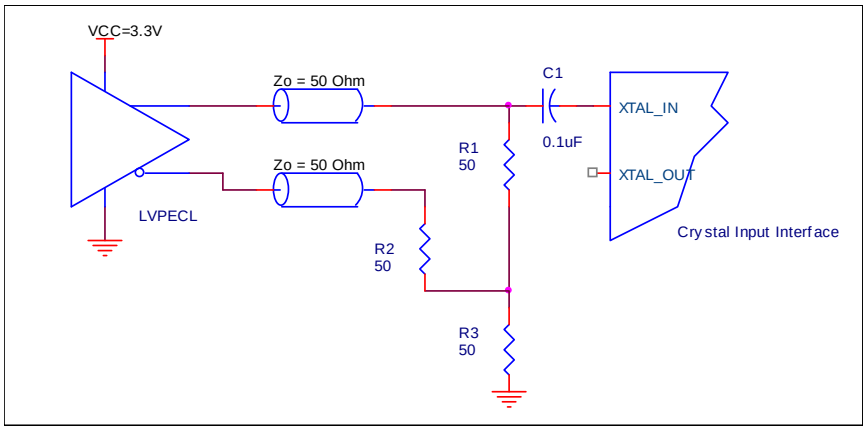


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

LVDS Driver Termination

A general LVDS interface is shown in *Figure 2.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 2 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the input receivers amplitude and common mode input range should be verified for compatibility with the output.

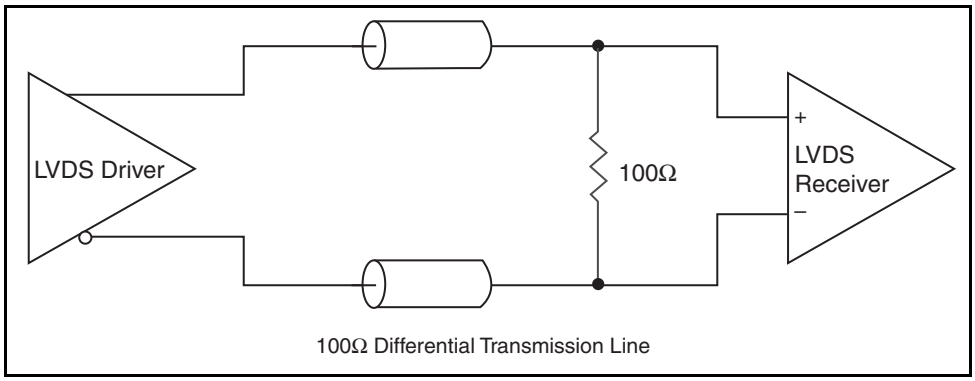


Figure 2. Typical LVDS Driver Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

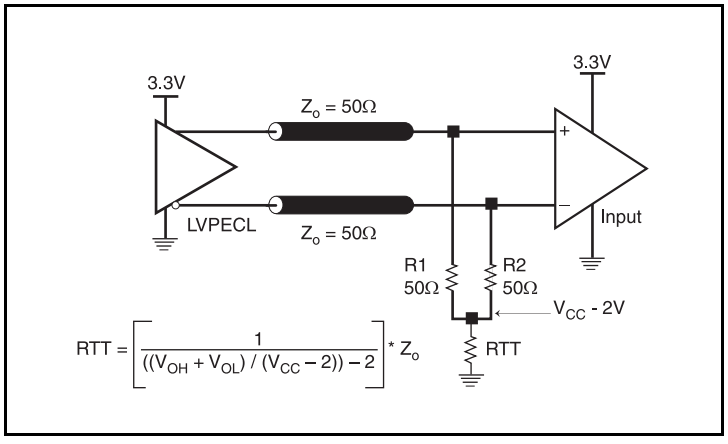


Figure 3A. 3.3V LVPECL Output Termination

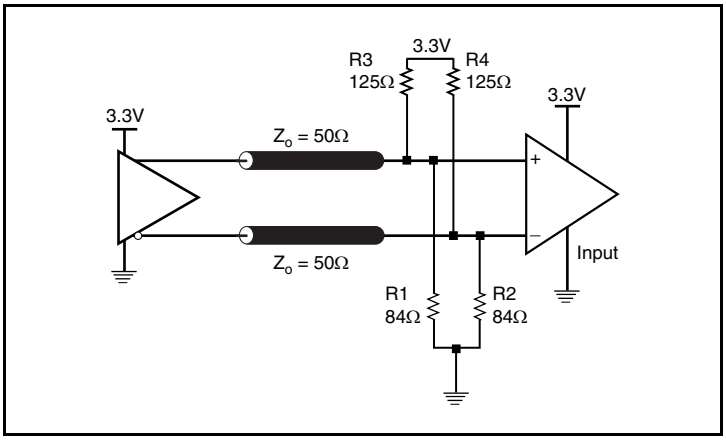


Figure 3B. 3.3V LVPECL Output Termination

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

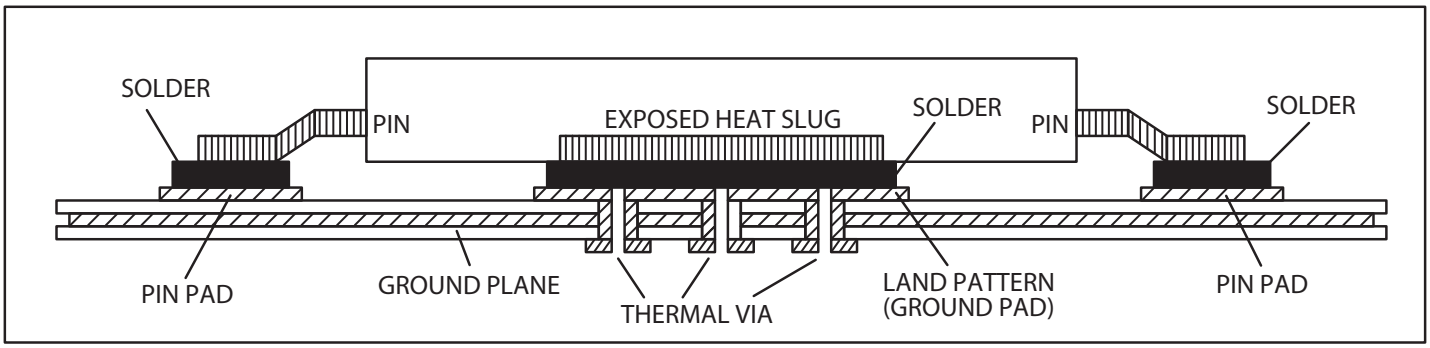


Figure 4. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Application Schematic Example

Figure 5 shows an example of 849S625 application schematic. In this example, the device is operated at V_{CC} = V_{CCA} = V_{CCO} = 3.3V. An 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. Depending on the parasitics of the printed circuit board layout, these values might required slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The 849S625 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

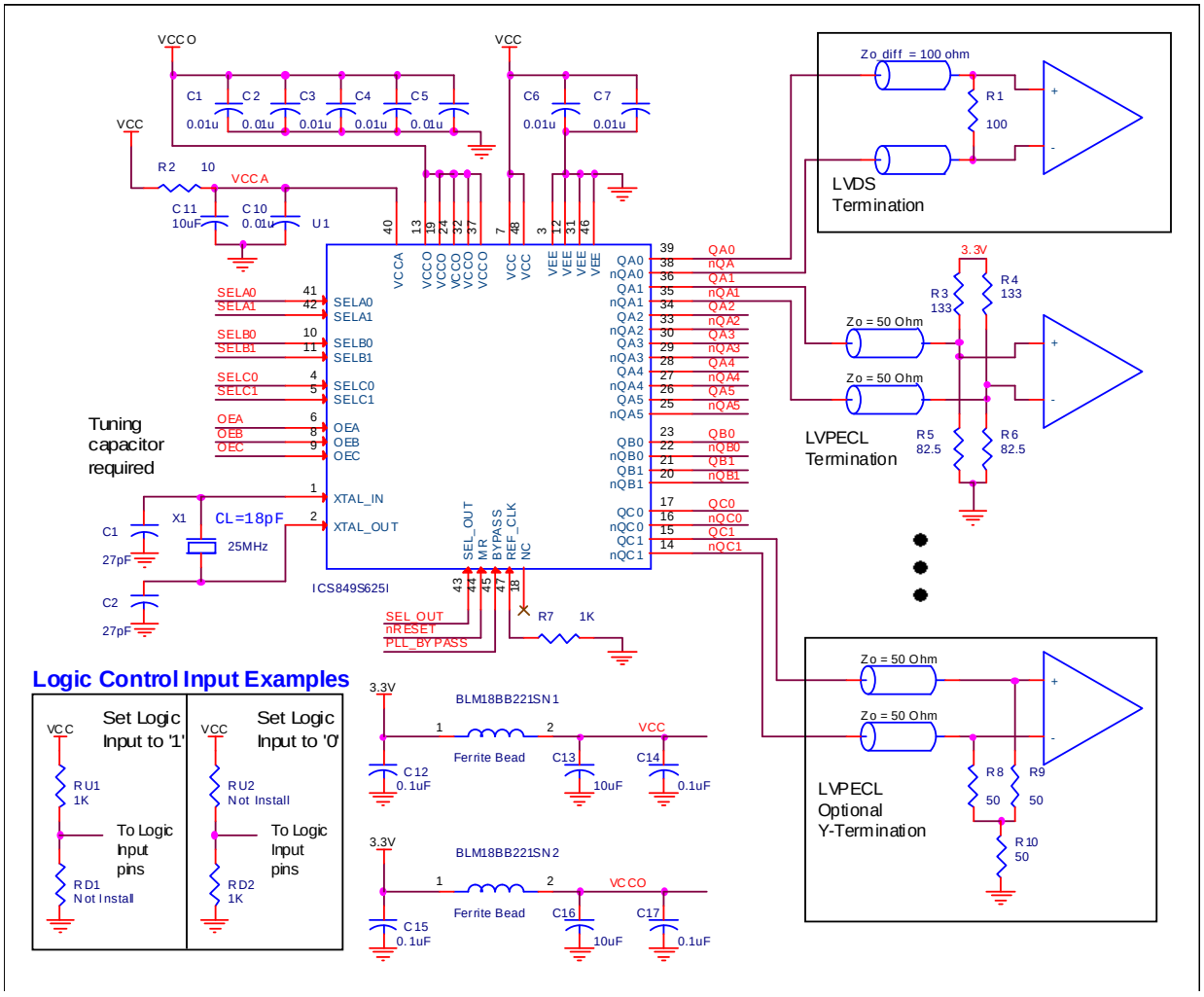


Figure 5. 849S625 Application Schematic

LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the 849S625.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 849S625 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

The maximum current at 85°C is as follows:
I_{EE_MAX} = 170mA

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 170mA = **589.05mW**
- Power $(outputs)_{MAX}$ = **33.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 10 * 33.2mW = **332mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 589.05mW + 332mW = **921.05mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.921W * 33.1°C/W = 115.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 48 Lead TQFP, E-Pad, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	27.2°C/W	25.7°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 6.*

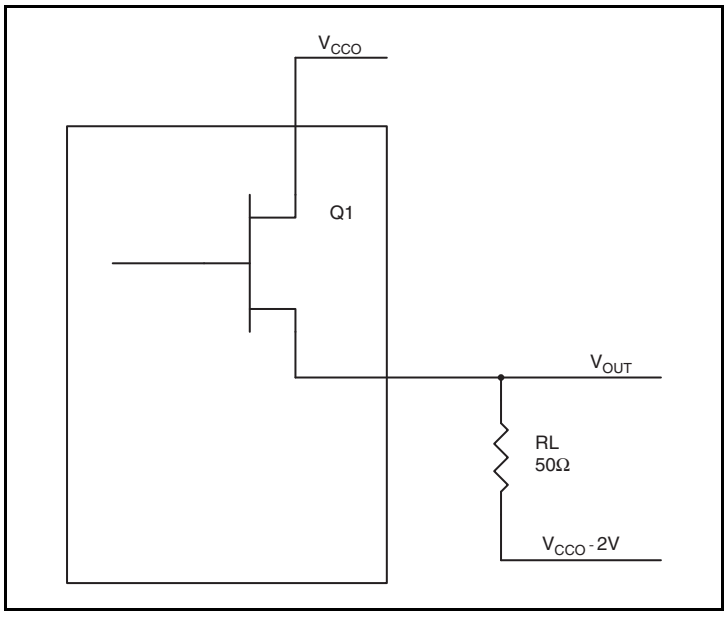


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.7V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.7V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.5V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.5V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.7V)/50\Omega] * 0.7V =$ **18.2mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.5V)/50\Omega] * 1.5V =$ **15mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **33.2mW**

LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the 849S625.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 849S625 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

The maximum current at 85°C is as follows:
I_{CC_MAX} = 100mA
I_{CCA_MAX} = 15mA
I_{CCO_MAX} = 212mA

- Power (core)$_{MAX}$ = V_{CC_MAX} * (I_{CC_MAX} + I_{CCA_MAX}) = 3.465V * (100mA + 15mA) = **398.475mW**
- Power (outputs)$_{MAX}$ = V_{CCO_MAX} * I_{CCO_MAX} = 3.465V * 212mA = **734.58mW**

Total Power$_{\_MAX}$ = 398.475mW + 734.58mW = **1133.1mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.133W * 33.1°C/W = 122.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8. Thermal Resistance θ_{JA} for 48 Lead TQFP, E-Pad, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	27.2°C/W	25.7°C/W

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for a 48 Lead TQFP, E-Pad

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	27.2°C/W	25.7°C/W

Transistor Count

The transistor count for 849S625 is: 3696

Package Outline and Package Dimensions

Package Outline - Y Suffix for 48 Lead TQFP, E-Pad

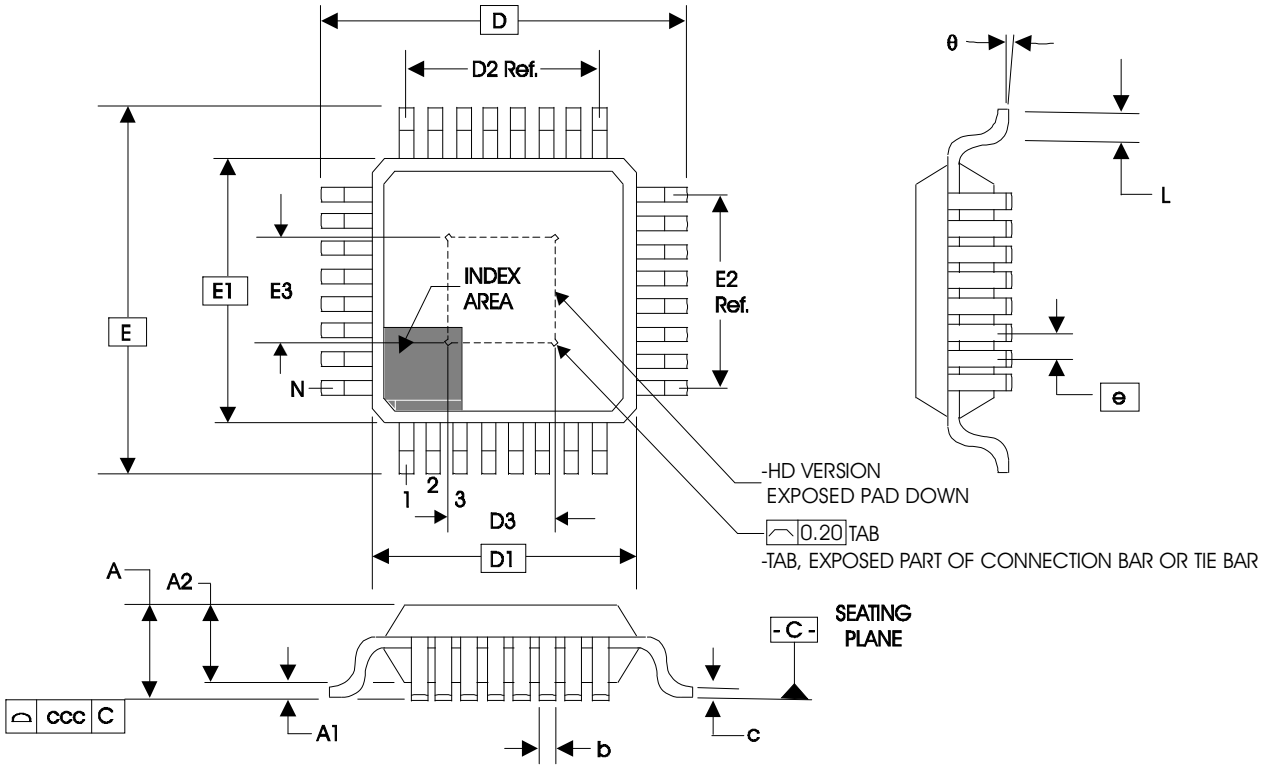


Table 10. Package Dimensions for 48 Lead TQFP, E-Pad

JEDEC Variation: BBC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		48	
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.50 Ref.	
D3 & E3		3.5	
e		0.5 Basic	
L	0.45	0.60	0.75
θ	0°		7°

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
849S625BYILF	ICS49S625BIL	“Lead-Free” 48 Lead TQFP, E-Pad	Tray	-40°C to 85°C
849S625BYILFT	ICS49S625BIL	“Lead-Free” 48 Lead TQFP, E-Pad	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T4E	6	VOD: changed units from V to mV	10/1/12
	T11	22	Deleted quantity from Tape &Rreel. Deleted Lead-Free note.	

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