RENESAS

FemtoClock® Crystal-to-LVDS Clock Generator

ICS844201I-45

DATASHEET

General Description

The ICS844201I-45 is a PCI Express™ Clock Generator. The ICS844201I-45 can synthesize 100MHz or 125MHz reference clock frequencies with a 25MHz crystal. The ICS844201I-45 has excellent phase jitter performance and is packaged in a small 16-pin VFQFN, making it ideal for use in systems with limited board space.

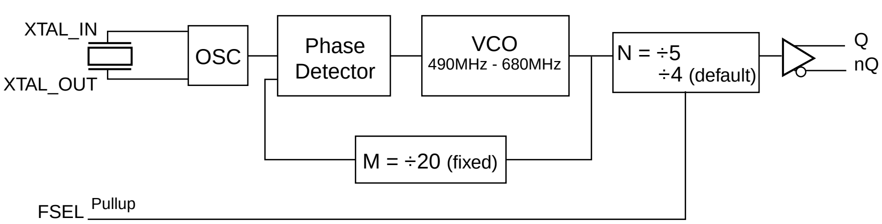
Features

- One differential LVDS output pair
- Crystal oscillator interface designed for 18pF, 25MHz parallel resonant crystal
- VCO range: 490MHz – 680MHz
- RMS phase jitter at 100MHz (12kHz – 20MHz): 0.792ps (typical)
- RMS phase jitter at 125MHz (12kHz – 20MHz): 0.773ps (typical)
- Full 3.3V output supply mode
- PCI Express (2.5Gb/s) and Gen 2 (5Gb/S) jitter compliant
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

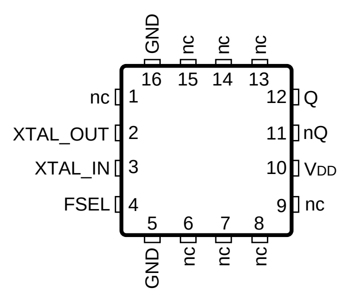
Frequency Table

Inputs					Output Frequency Range (MHz)
Crystal Frequency (MHz)	M	FSEL	N	Multiplication Value M/N	
25	20	1	4	5	125 (default)
25	20	0	5	4	100

Block Diagram



Pin Assignment



ICS844201I-45

16-Lead VFQFN
Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 6, 7, 8, 9, 13, 14, 15	nc	Unused		No connect.
2, 3	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4	FSEL	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
5, 16	GND	Power		Power supply ground.
10	V_{DD}	Power		Power supply pin.
11, 12	nQ, Q	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	74.9°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.97	3.3	3.63	V
I_{DD}	Power Supply Current				95	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.63V			5	µA
I_{IL}	Input Low Current	V_{DD} = 3.63V, V_{IN} = 0V	-150			µA

Table 3C. LVDS DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{DIFF_OUT}	Peak-to-Peak Differential Output Voltage		494		908	mV
V_{OS}	Offset Voltage		1.3		1.63	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		24.5	25	34	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

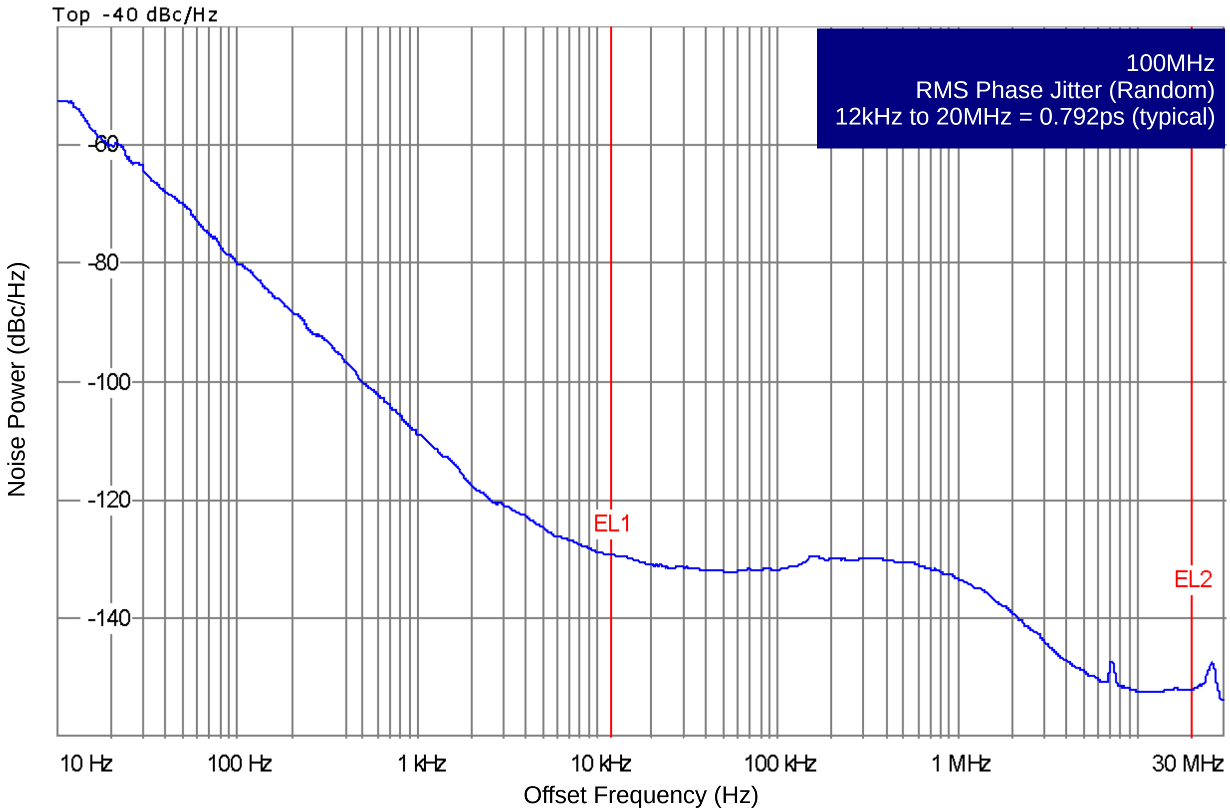
AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

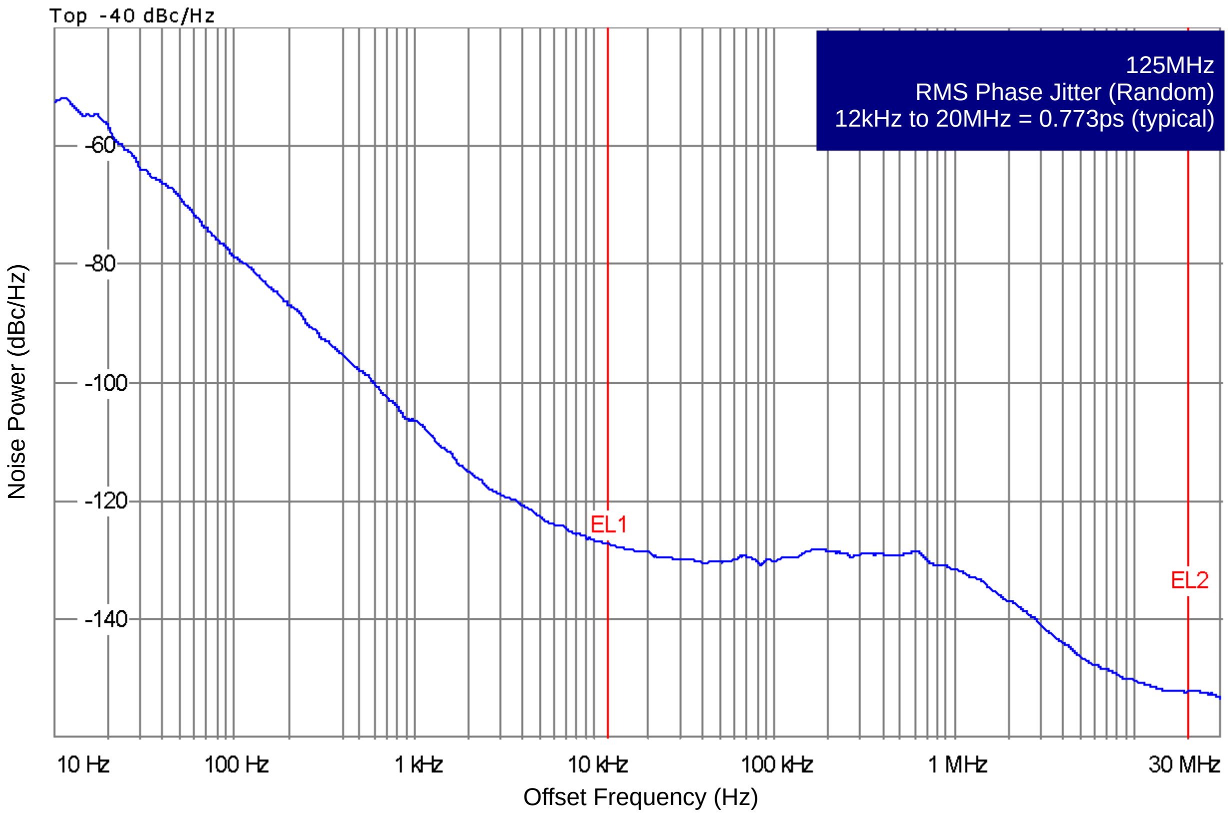
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			125		MHz
				100		MHz
tjit(Ø)	RMS Phase Jitter, Random; NOTE 1	125MHz, Integration Range: 12kHz – 20MHz		0.773		ps
		100MHz, Integration Range: 12kHz – 20MHz		0.792		ps
t_j	Phase Jitter Peak-to-Peak; NOTE 2	125MHz, (1.2MHz – 21.9MHz) 25MHz crystal input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		12.51		ps
		100MHz, (1.2MHz – 21.9MHz) 25MHz crystal input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		13.48		ps
$t_{REFCLK\_HF\_RMS}$	Phase Jitter RMS; NOTE 3	125MHz, (1.2MHz – 21.9MHz) 25MHz crystal input High Band: 1.5MHz - Nyquist (clock frequency/2)		1.13		ps
		100MHz, (1.2MHz – 21.9MHz) 25MHz crystal input High Band: 1.5MHz - Nyquist (clock frequency/2)		1.25		ps
$t_{REFCLK\_LF\_RMS}$	Phase Jitter RMS; NOTE 3	125MHz, (1.2MHz – 21.9MHz) 25MHz crystal input Low Band: 10kHz - 1.5MHz		0.32		ps
		100MHz, (1.2MHz – 21.9MHz) 25MHz crystal input Low Band: 10kHz - 1.5MHz		0.33		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		450	ps
odc	Output Duty Cycle	f_{OUT} = 125MHz	48		52	%
		f_{OUT} = 100MHz	46		54	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 25MHz crystal.
NOTE 1: Refer to Phase Noise Plots.
NOTE 2: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods. See IDT Application Note *PCI Express Reference Clock Requirements* and also the PCI Express Application section of this datasheet which show each individual transfer function and the overall composite transfer function.
NOTE 3: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps rms for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0 ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band). See IDT Application Note *PCI Express Reference Clock Requirements* and also the PCI Express Application section of this datasheet which show each individual transfer function and the overall composite transfer function.

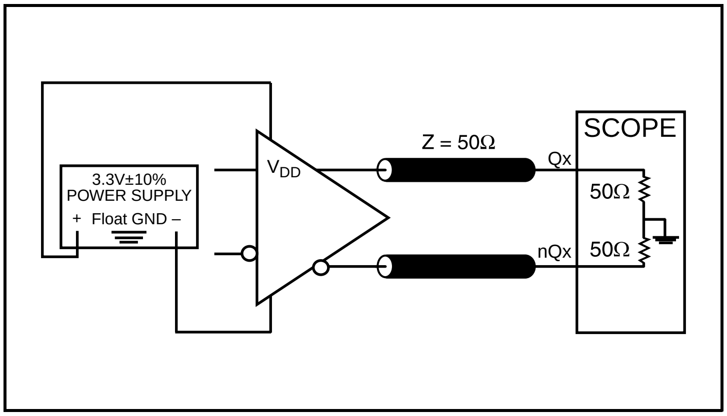
Typical Phase Noise at 100MHz



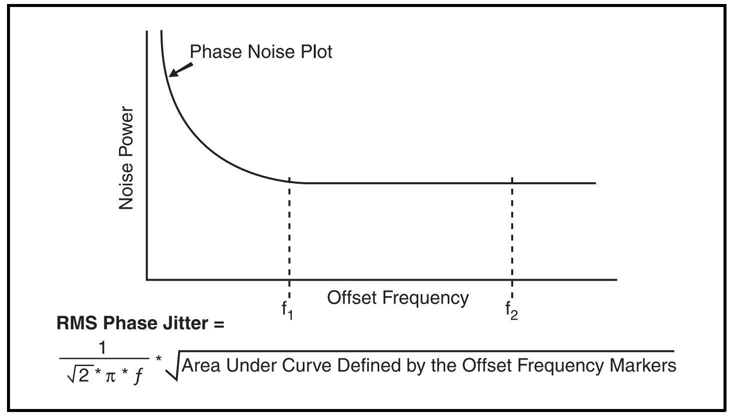
Typical Phase Noise at 125MHz



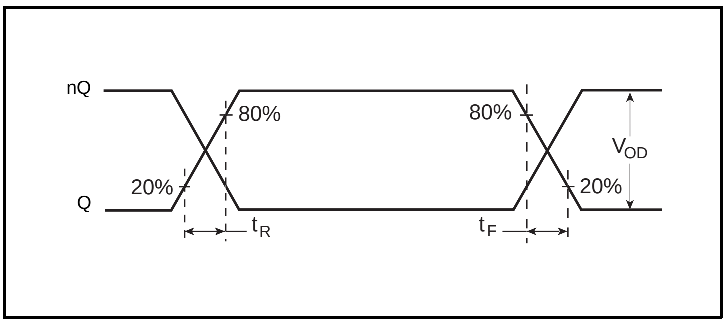
Parameter Measurement Information



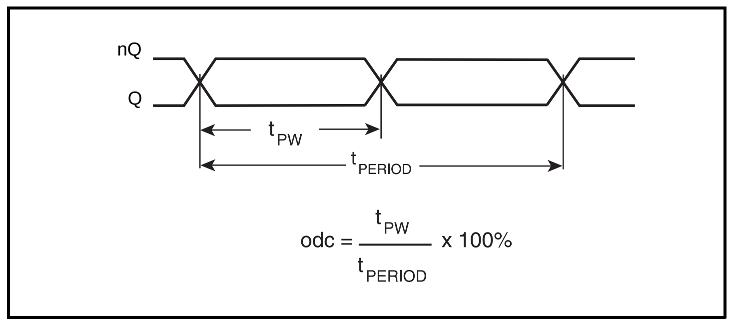
3.3V LVDS Output Load AC Test Circuit



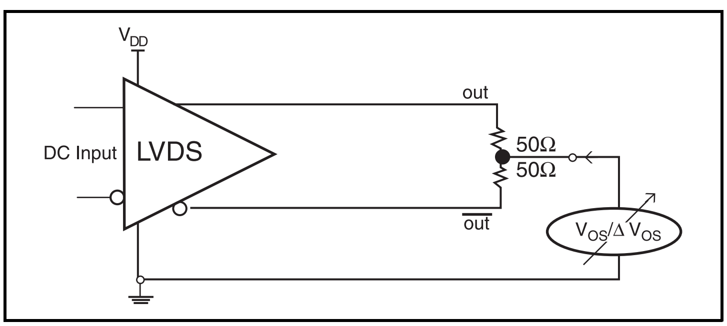
RMS Phase Jitter



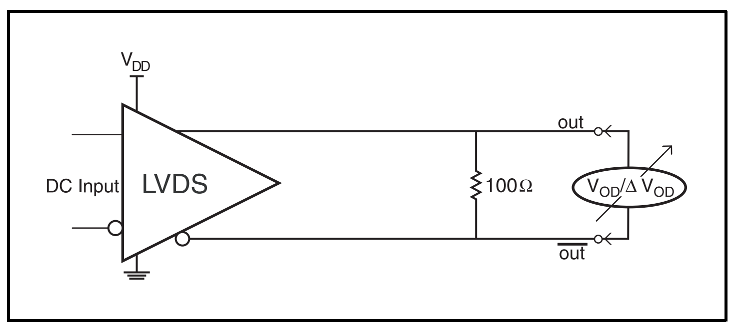
Output Rise/Fall Time



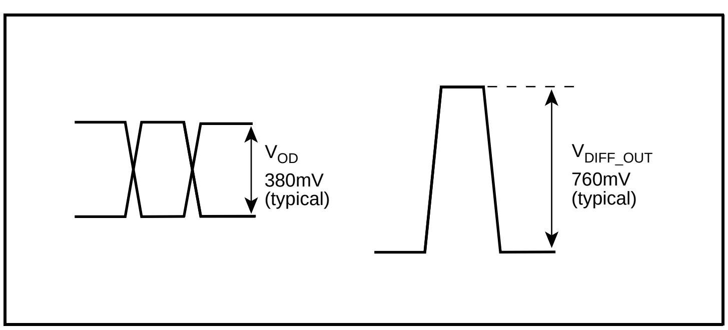
Output Duty Cycle/Pulse Width/Period



Offset Voltage Setup



Differential Output Voltage Setup



Differential Output Voltage

Application Information

Crystal Input Interface

The ICS844201I-45 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

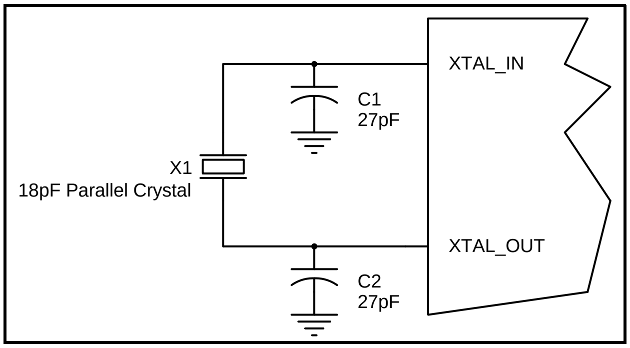


Figure 1. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

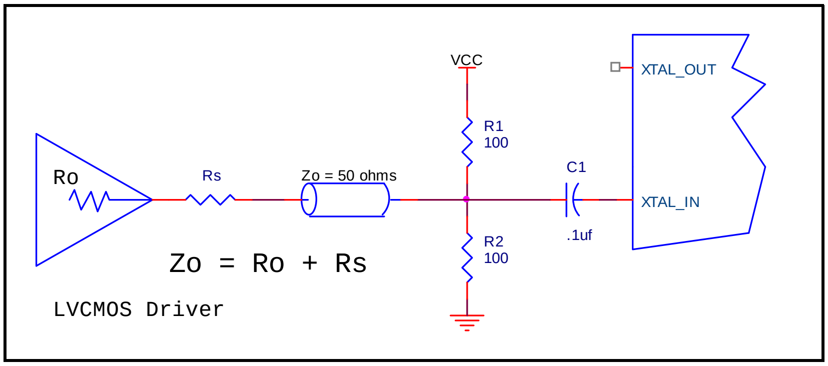


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

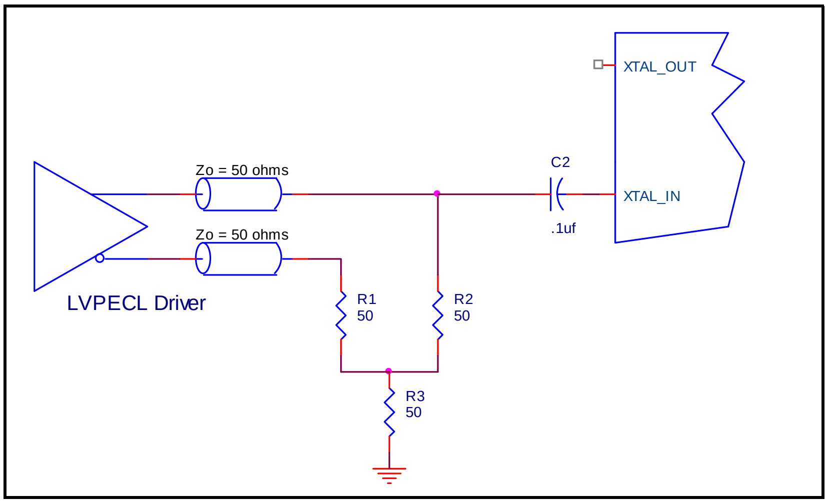
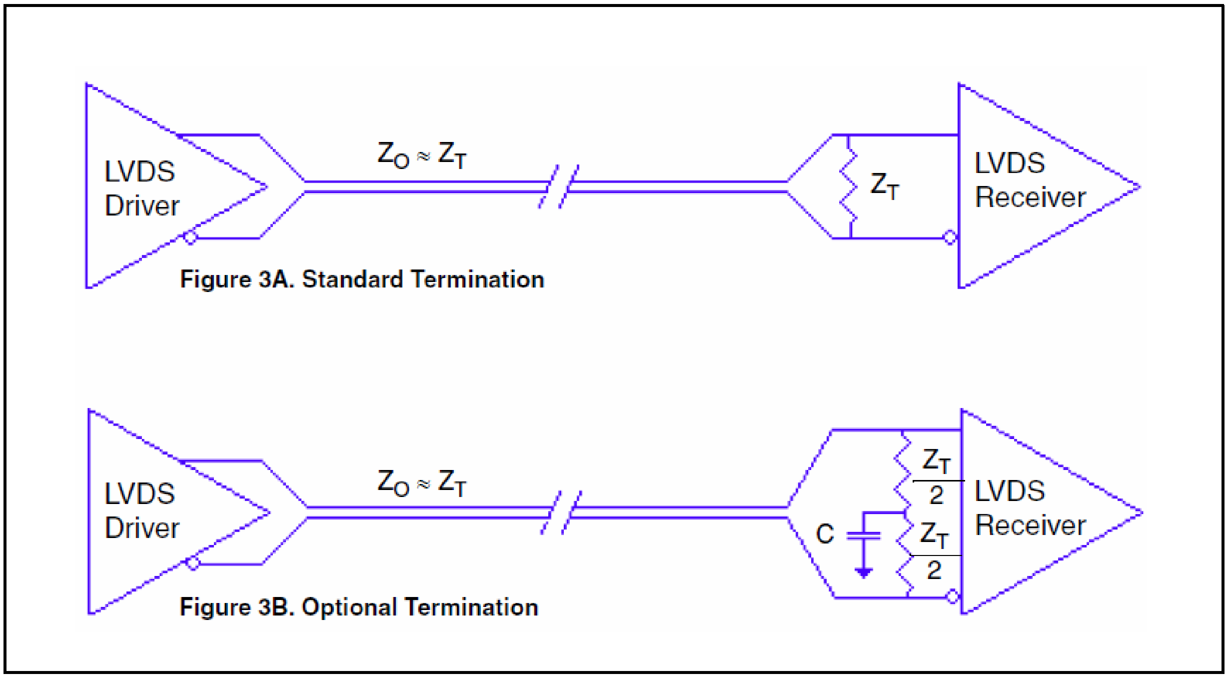


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



LVDS Termination

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

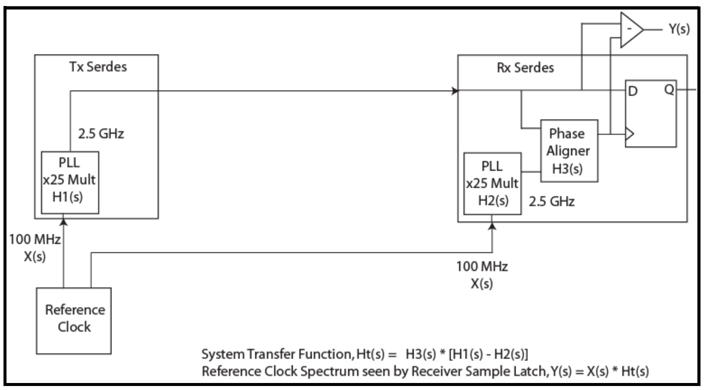
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

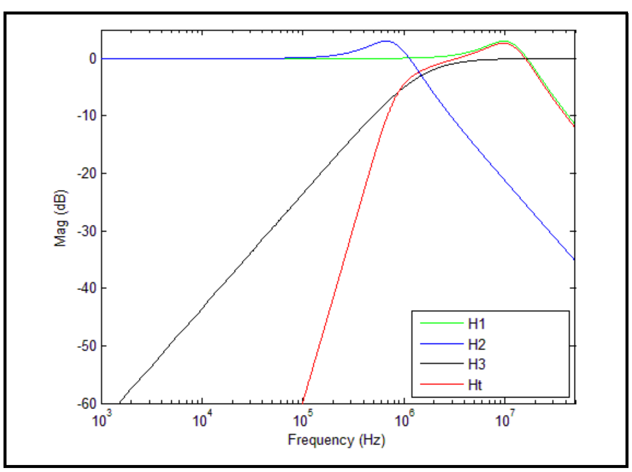
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



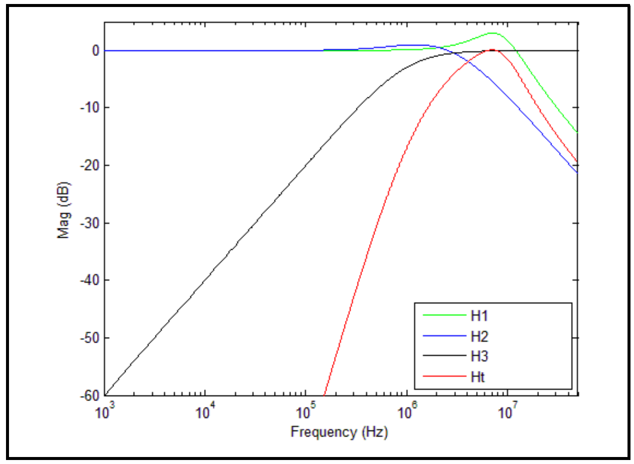
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

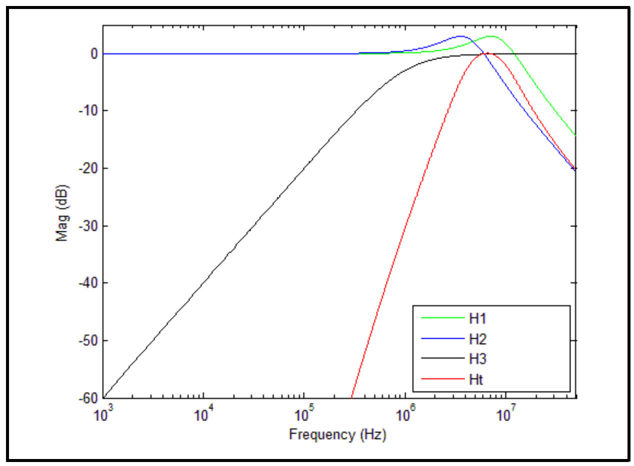


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

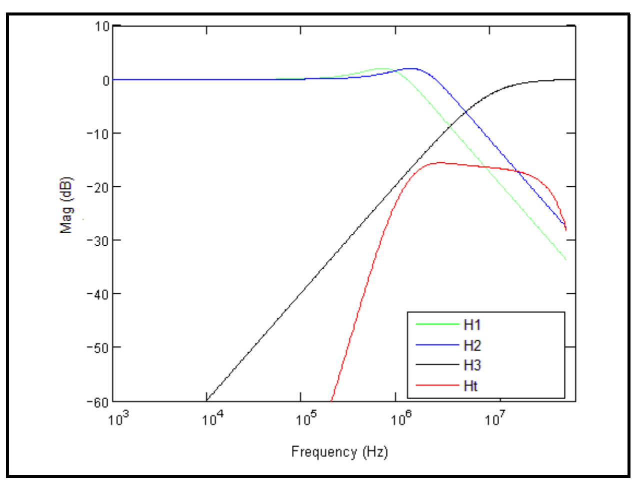


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

Schematic Example

Figure 4 shows an example of ICS844201I-45 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVDS for receiver without built-in termination are shown in this schematic.

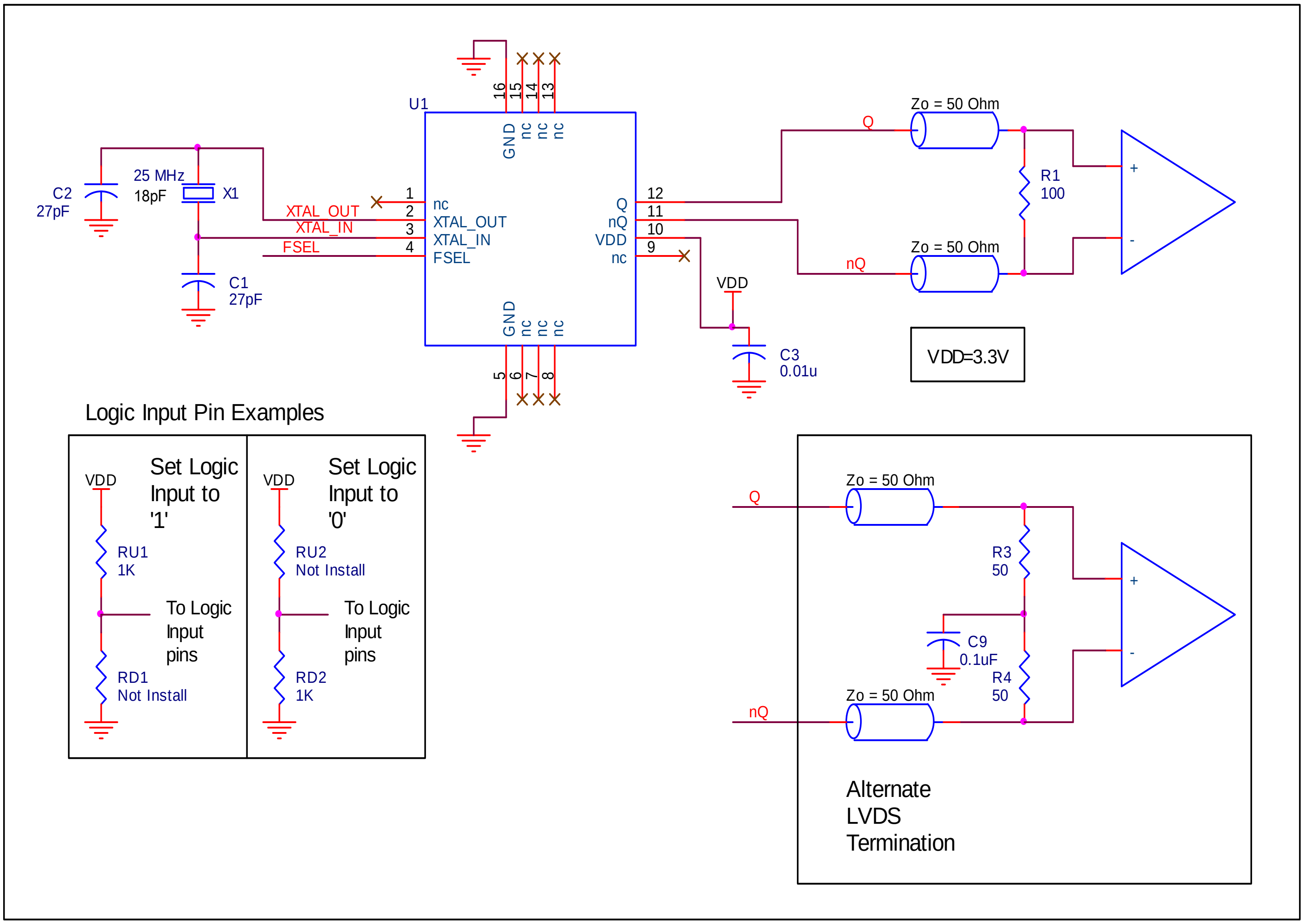


Figure 4. ICS844201I-45 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844201I-45.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844201I-45 is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 10% = 3.63V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.63V * 95mA = **344.85mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.9°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.345W * 74.9°C/W = 110.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.9°C/W	65.5°C/W	58.8°C/W

Reliability Information

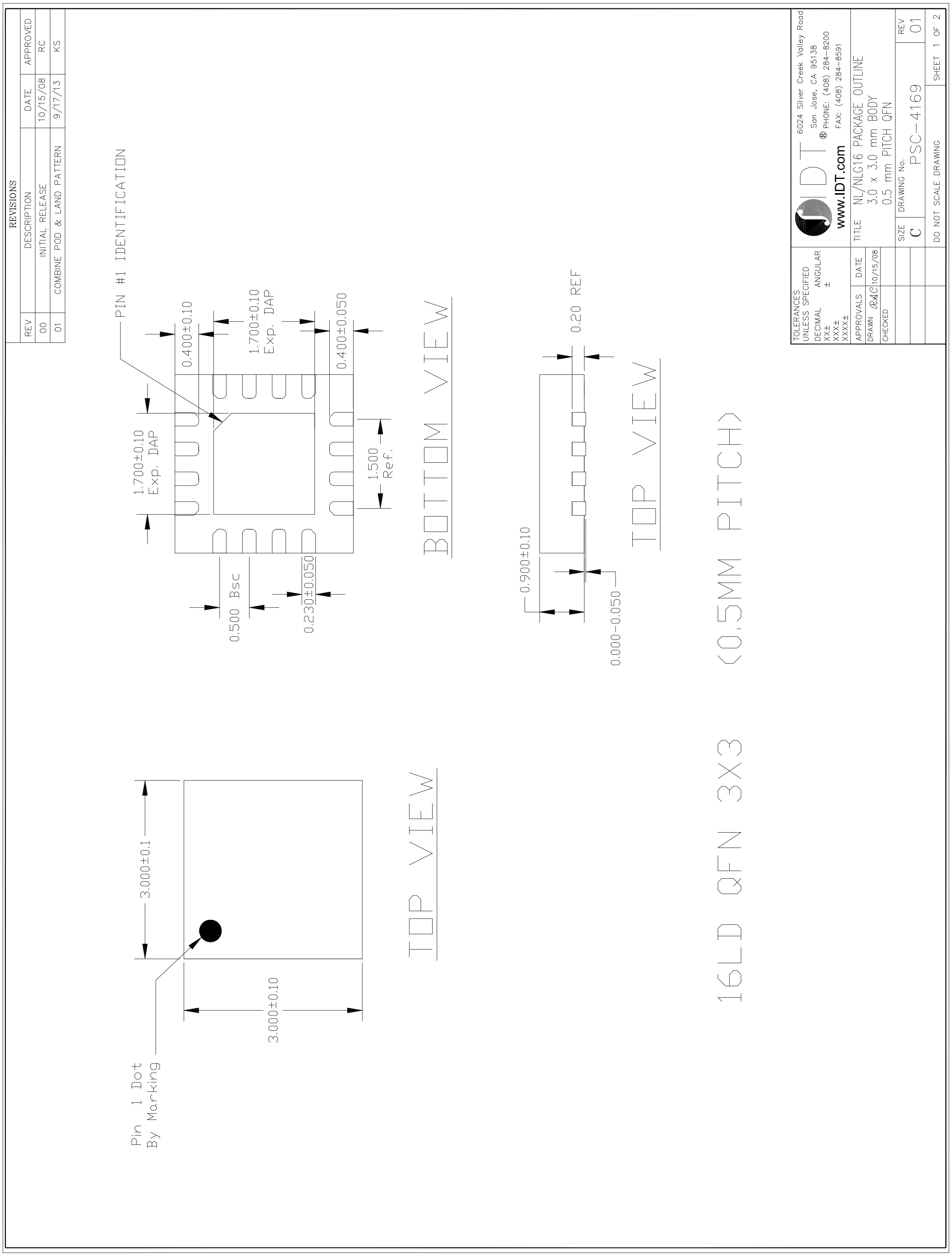
Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.9°C/W	65.5°C/W	58.8°C/W

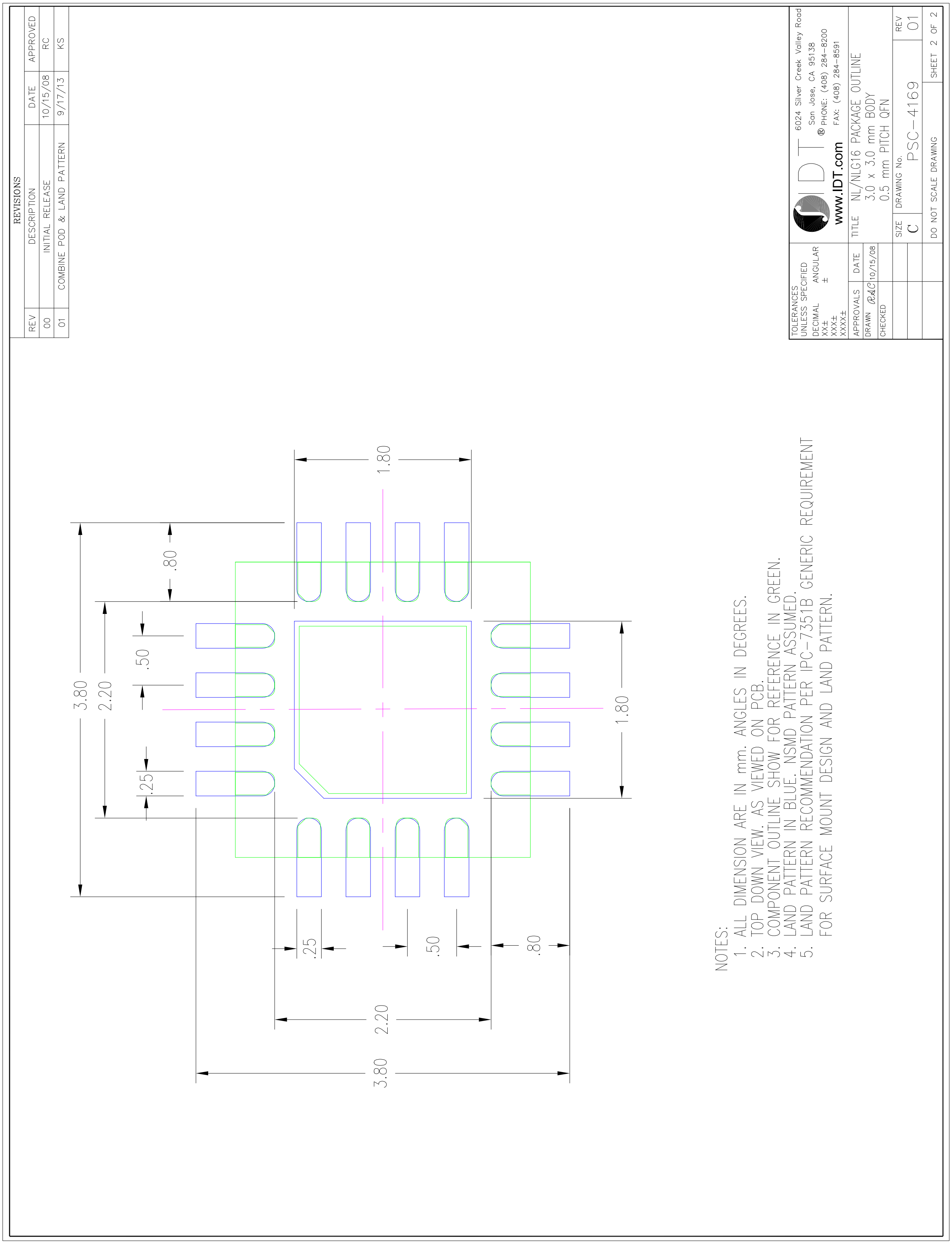
Transistor Count

The transistor count for ICS844201I-45 is: 1986

Package Outline Drawings (Sheet 1)



Package Outline Drawings (Sheet 2)



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844201BKI-45LF	B15L	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
844201BKI-45LFT	B15L	“Lead-Free” 16 Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	-	-	Initial release.	10/07/2013
B	-	11/12	Updated the package outline drawings.	5/27/2017

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Contact Information

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