

General Description

The 843S1333D is a high frequency clock generator. The 843S1333D uses an external 20MHz crystal to synthesize 1333.33MHz. The 843S1333D has excellent cycle-to-cycle and RMS period jitter performance.

The 843S1333D operates at 3.3V operating supply and is available in a fully RoHS compliant 8-lead TSSOP package.

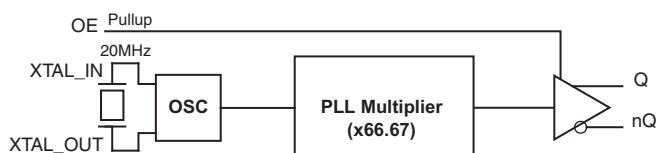
Features

- One differential LVPECL output
- Crystal oscillator interface designed for 18pF, 20MHz parallel resonant crystal
- Cycle-to-Cycle Jitter: 14ps (maximum)
- Period Jitter, RMS: 2.6ps (maximum)
- Output Duty Cycle: 48 – 52%
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

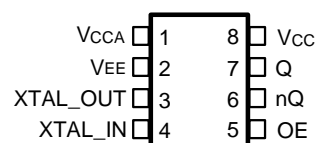
Table 1. Frequency Table

Crystal Frequency (MHz)	Multiplier Value	Output Frequency (MHz)
20	66.67	1333.33

Block Diagram



Pin Assignment



843S1333D

8 Lead TSSOP

4.40mm x 3.0mm x 0.925mm package body

G Package

Top View

Table 2. Pin Descriptions

Number	Name	Type		Description
1	V _{CCA}	Power		Analog supply pin.
2	V _{EE}	Power		Negative supply pin.
3, 4	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. External tuning capacitor must be used for proper operation.
5	OE	Input	Pullup	Synchronous output enable. When logic HIGH, the outputs are enabled and active. When logic LOW, Q output is forced LOW and nQ output is forced HIGH. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential output pair. LVPECL interface levels.
8	V _{CC}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 3. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			2		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I XTAL_IN Other Inputs	0V to V_{CC} -0.5V to $V_{CC} + 0.5V$
Outputs, I_O Continuous Current Surge Current	50mA 100mA
Package Thermal Impedance, θ_{JA}	115.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		$V_{CC} - 0.23$	3.3	V_{CC}	V
I_{EE}	Power Supply Current				80	mA
I_{CCA}	Analog Supply Current				23	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	$V_{CC} = V_{IN} = 3.465V$			10	μA
I_{IL}	Input Low Current	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			μA

Table 4C. LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} - 1.3$		$V_{CC} - 0.8$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.6$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to $V_{CC} - 2V$.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			20		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 6. AC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

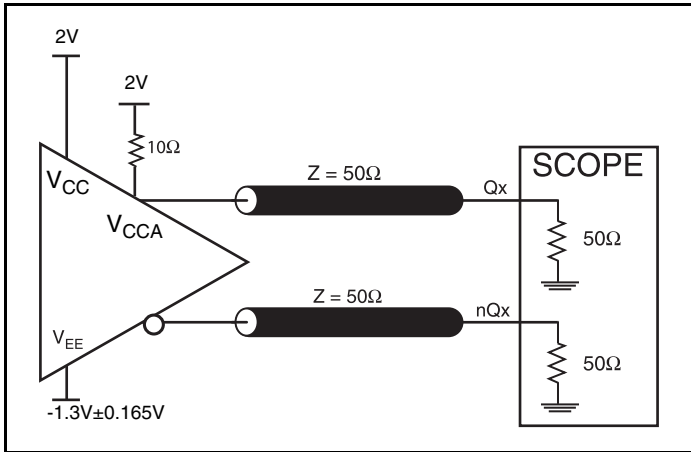
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			1333.33		MHz
$\dot{f}_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1				14	ps
$\dot{f}_{jit(per)}$	Period Jitter, RMS; NOTE 1				2.6	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	80		200	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

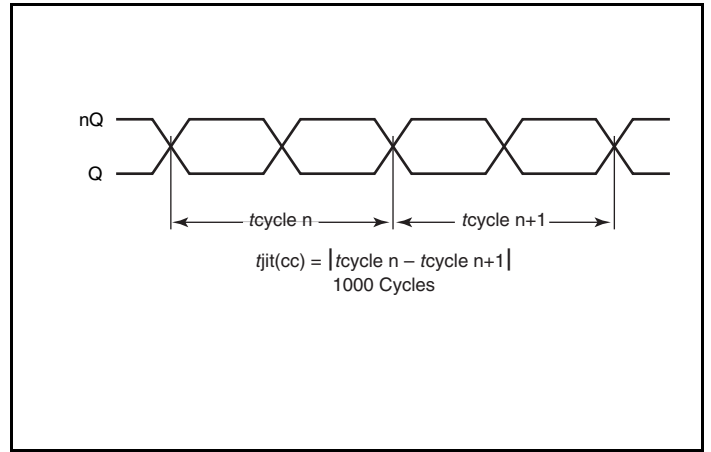
NOTE: External tuning capacitor must be used for proper operation.

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

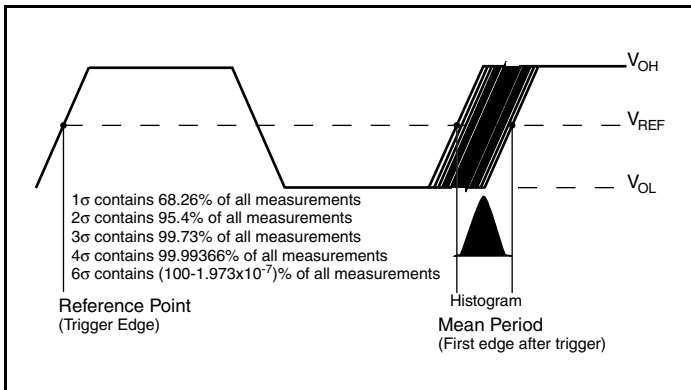
Parameter Measurement Information



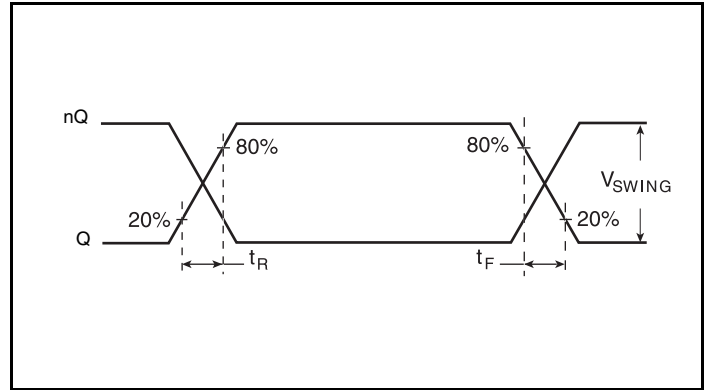
3.3V LVPECL Output Load AC Test Circuit



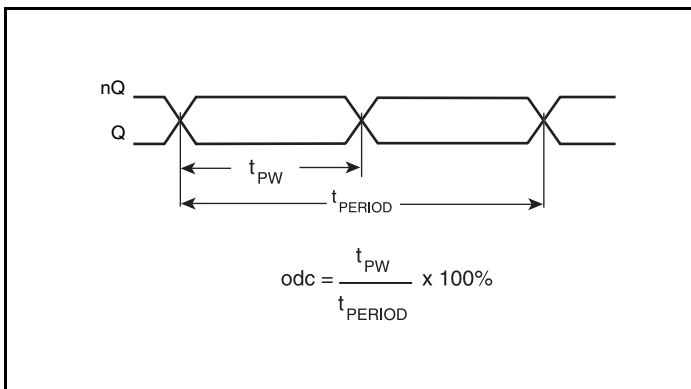
Cycle-to-Cycle Jitter



RMS Period Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843S1333D provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{CCA} pin.

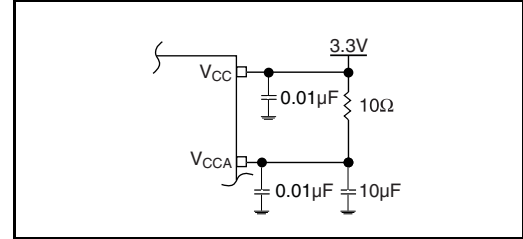


Figure 1. Power Supply Filtering

Crystal Input Interface

The 843S1333D has been characterized with 18pF parallel resonant crystals. The capacitor values, $C1$ and $C2$, shown in *Figure 2* below were determined using a 20MHz , 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum $C1$ and $C2$ values can be slightly adjusted for different board layouts. External tuning capacitor must be used for proper operation.

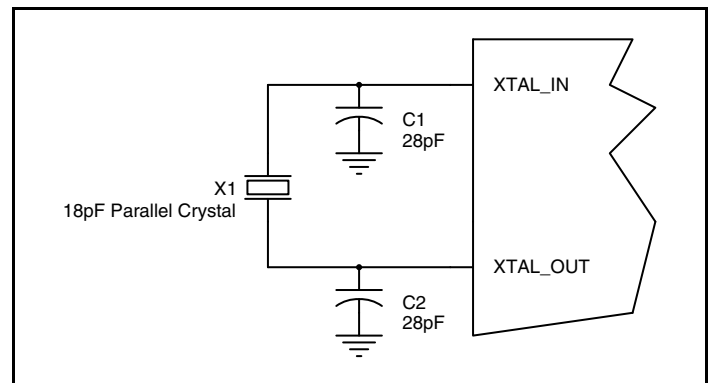


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω. This can also be accomplished by removing R_1 and making R_2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

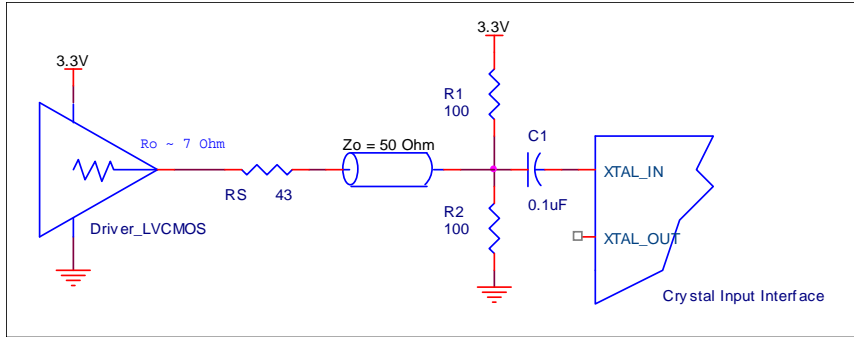


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

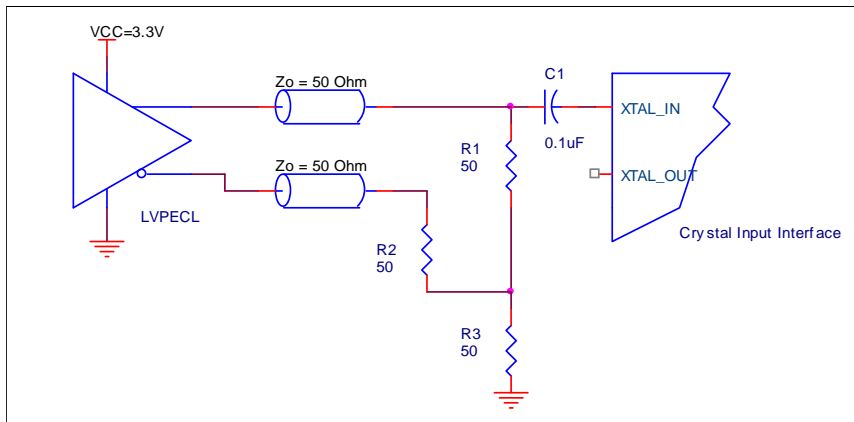


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 4A and 4B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

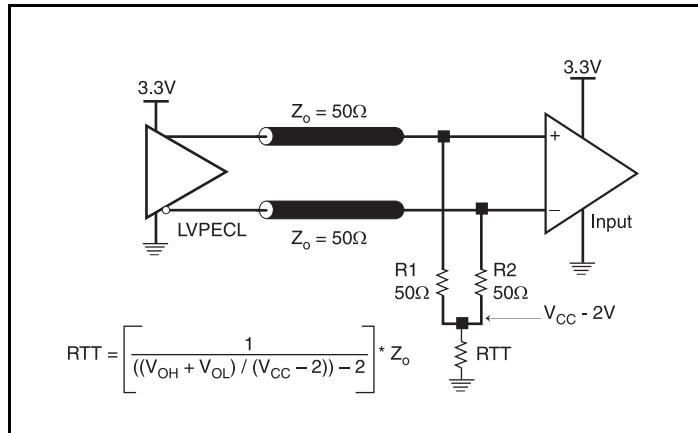


Figure 4A. 3.3V LVPECL Output Termination

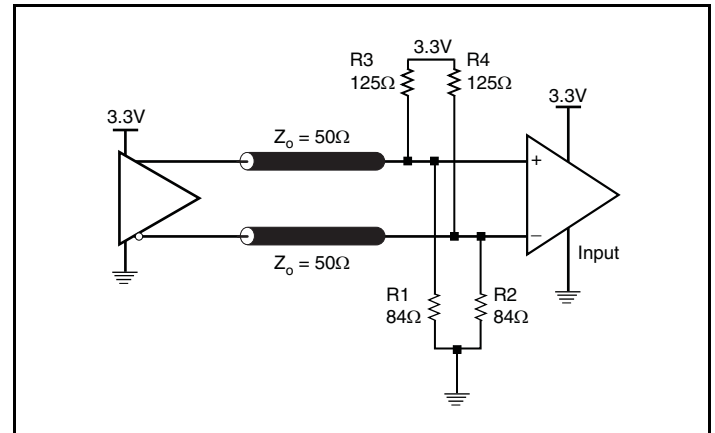


Figure 4B. 3.3V LVPECL Output Termination

Schematic Example

Figure 5 shows an example of the ICS843S133D application schematic. In this example, the device is operated at $V_{CC} = 3.3V$. The 18pF parallel resonant 20MHz crystal is used. The C1 and C2 = 28pF are recommended for frequency accuracy. For different board layout,

the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL termination are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

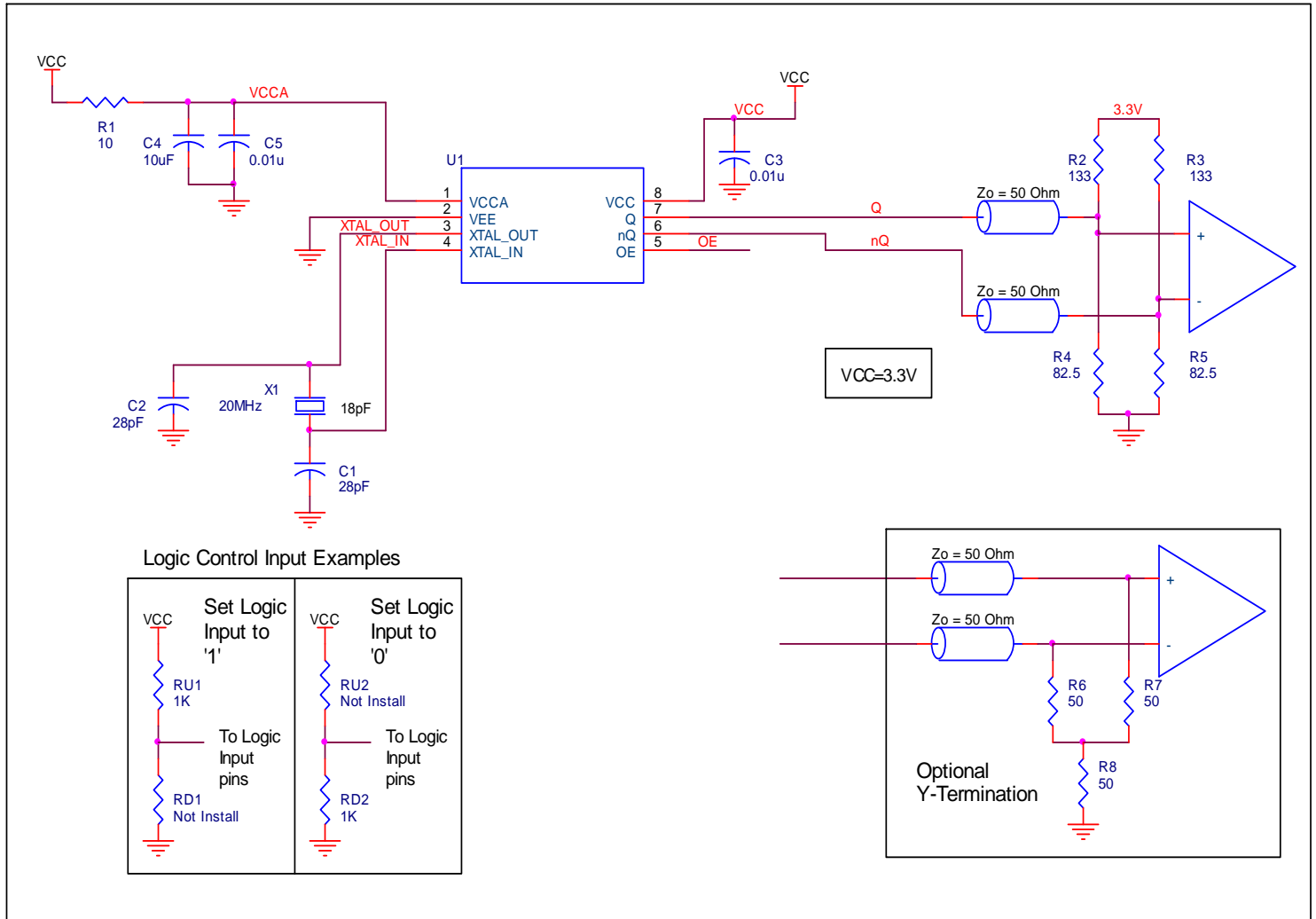


Figure 5. 843S133D Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 843S1333D. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843S1333D is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

The maximum current at 70°C is as follows: $I_{DD_MAX} = 77.68mA$

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 77.68mA = 269.16mW$
- Power (outputs)_{MAX} = **32mW/Loaded Output pair**

Total Power_{MAX} (3.3V, with all outputs switching) = $269.16mW + 32mW = 301.16mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 115.2°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.301W * 115.2^\circ C/W = 104.7^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	115.2°C/W	110.9°C/W	108.8°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 6*.

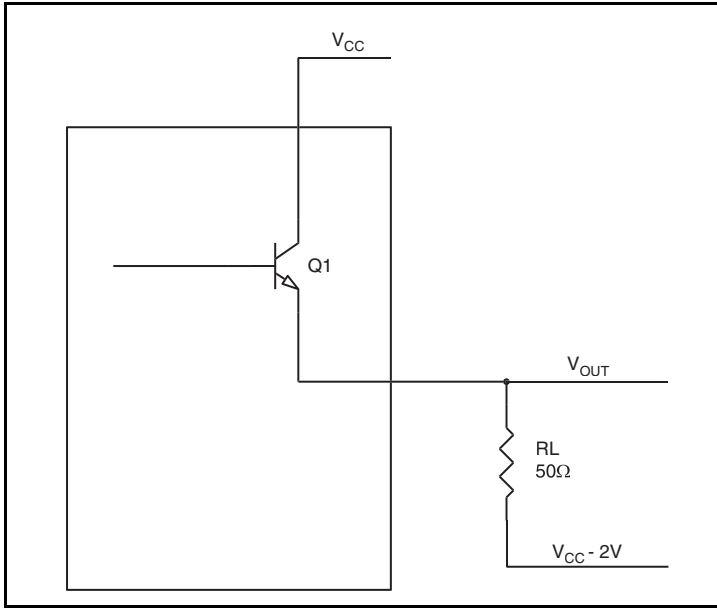


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.8V$
($V_{CC_MAX} - V_{OH_MAX}$) = **0.8V**
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.6V$
($V_{CC_MAX} - V_{OL_MAX}$) = **1.6V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.8V)/50\Omega] * 0.8V = \mathbf{19.2mW}$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.6V)/50\Omega] * 1.6V = \mathbf{12.8mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{32mW}$$

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	115.2°C/W	110.9°C/W	108.8°C/W

Transistor Count

The transistor count for 843S1333D is: 1023

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

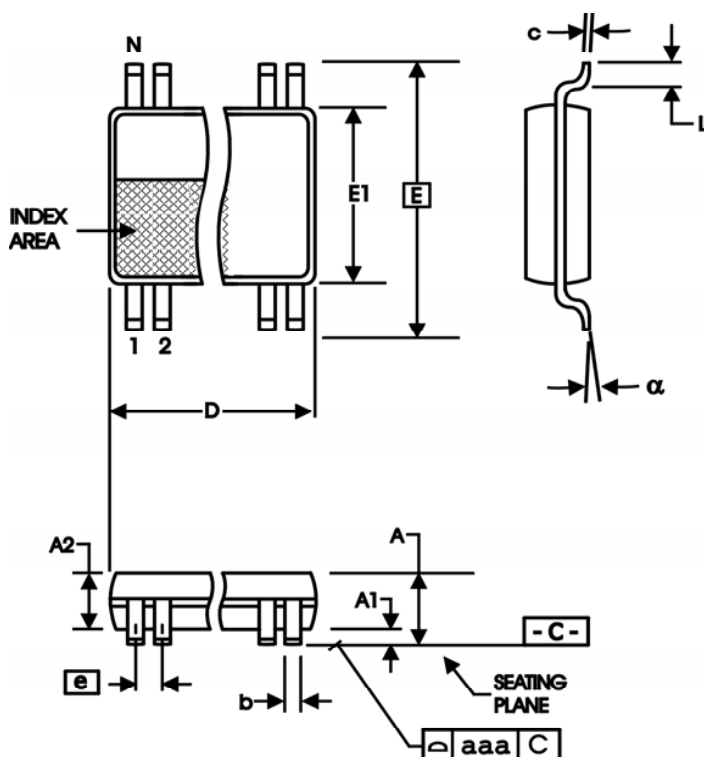


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843S1333DGLF	33DL	"Lead-Free" 8 Lead TSSOP	Tube	0°C to 70°C
843S1333DGLFT	33DL	"Lead-Free" 8 Lead TSSOP	Tape & Reel	0°C to 70°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A			Updated data sheet format.	12/2/15

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.