General Description

The ICS843252-04 is a 10Gb/12Gb Ethernet Clock Generator. The ICS843252-04 can synthesize 10 Gigabit Ethernet and 12 Gigabit Ethernet with a 25MHz crystal. It can also generate SATA and 10Gb Fibre Channel reference clock frequencies with the appropriate choice of crystals. The ICS843252-04 has excellent phase jitter performance and is packaged in a small 16-pin TSSOP, making it ideal for use in systems with limited board space.

Features

- Two differential 3.3V LVPECL output pairs
- Crystal input frequency range: 20MHz – 30MHz
- Output frequency range: 150MHz – 187.5MHz
- VCO frequency: 600MHz – 750MHz
- RMS Phase Jitter @ 156.25MHz, (1.875MHz – 20MHz): 0.31ps (typical)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Lead-free (RoHS 6) packaging

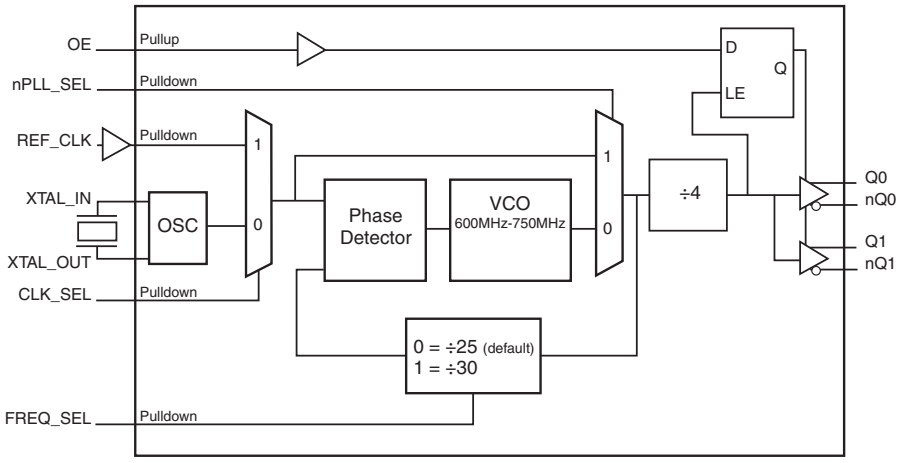
Configuration Table with 25MHz Crystal

Inputs				Output Frequency (MHz)	Application
Crystal Frequency (MHz)	Feedback Divide	VCO Frequency (MHz)	N Output Divide		
25	30	750	4	187.5	12 Gigabit Ethernet
25	25	625	4	156.25	10 Gigabit Ethernet

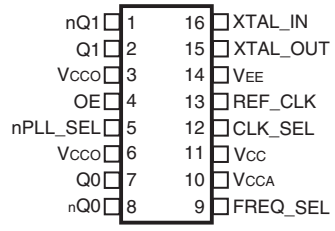
Configuration Table with Selectable Crystals

Inputs				Output Frequency (MHz)	Application
Crystal Frequency (MHz)	Feedback Divide	VCO Frequency (MHz)	N Output Divide		
20	30	600	4	150	SATA
21.25	30	637.5	4	159.375	10 Gigabit Ethernet
24	25	600	4	150	SATA
25.5	25	637.5	4	159.375	10 Gigabit Ethernet
30	25	750	4	187.5	12 Gigabit Ethernet

Block Diagram



Pin Assignment



ICS843252-04

16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm
package body
G Package
Top View

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Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential clock output pair. LVPECL interface levels.
3, 6	V_{CCO}	Power		Output supply pins.
4	OE	Input	Pullup	Output enable. When HIGH, clock outputs follow clock input. When LOW, Qx outputs are forced low, nQx outputs are forced high. LVCMOS/LVTTL interface levels.
5	nPLL_SEL	Input	Pulldown	PLL select pin. When LOW, selects the PLL. When HIGH, bypasses the PLL. LVCMOS/LVTTL interface levels.
7, 8	Q0, nQ0	Output		Differential clock output pair. LVPECL interface levels.
9	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
10	V_{CCA}	Power		Analog supply pin.
11	V_{CC}	Power		Power supply pin.
12	CLK_SEL	Input	Pulldown	Clock select input. When LOW, selects the crystal inputs. When HIGH, selects REF_CLK. LVCMOS/LVTTL interface levels.
13	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
14	V_{EE}	Power		Negative supply pin.
15, 16	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface XTAL_IN is the input, XTAL_OUT is the output.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	REF_CLK			4		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I, XTAL_IN Other Inputs	 0V to V_{CC} -0.5V to V_{CC} + 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	81.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$; $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.16	3.3	V_{CC}	V
V_{CCO}	Power Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current				76	mA
I_{CCA}	Analog Supply Current				16	mA
I_{EE}	Power Supply Current				113	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$; $T_A = 0°C$ to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK, CLK_SEL, nPLL_SEL, FREQ_SEL	$V_{CC} = V_{IN} = 3.465V$			150	µA
		OE	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	REF_CLK, CLK_SEL, nPLL_SEL, FREQ_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		OE	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA

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Table 3C. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$; $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.55		1.0	V

NOTE 1: Output termination with 50Ω to $V_{CCO} - 2V$.

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		20		30	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Capacitive Loading (C_L)			12	18	pF

AC Electrical Characteristics

Table 5. AC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$; $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		150		187.5	MHz
$t$jit(Ø)	RMS Phase Jitter (Random); NOTE 1	156.25MHz, Integration Range: 1.875MHz – 20MHz		0.31	0.40	ps
		159.375MHz, Integration Range: 1.875MHz – 20MHz		0.31	0.35	ps
		187.5MHz, Integration Range: 1.875MHz – 20MHz		0.33	0.40	ps
$t$sk(o)	Output skew; NOTE 2, 3			5	15	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		600	ps
odc	Output Duty Cycle	nPLL_SEL = 0	48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using crystal with $C_L = 18pF$.
NOTE 1: Please refer to the Phase Noise plots.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.

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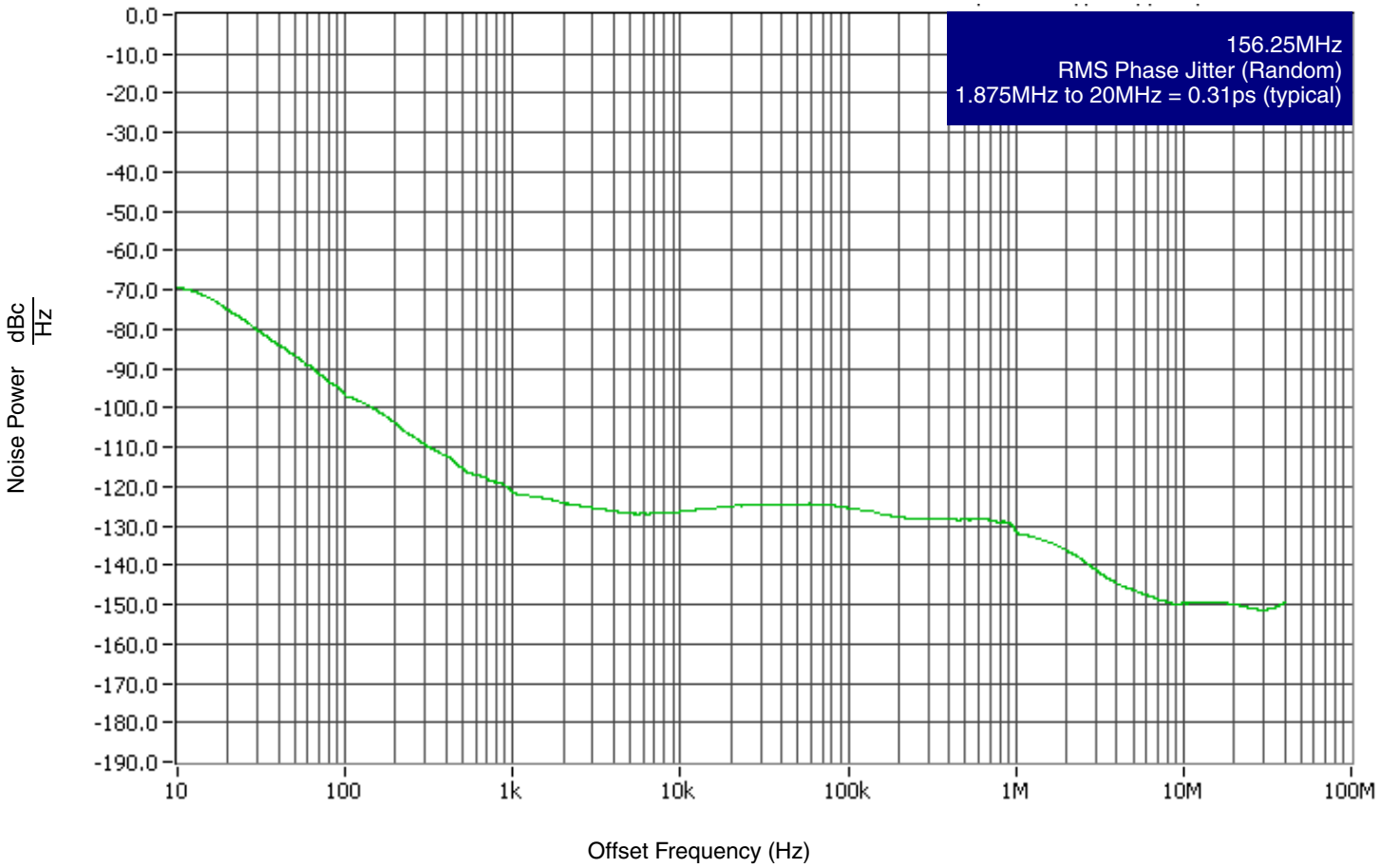
Typical Phase Noise at 156.25MHz



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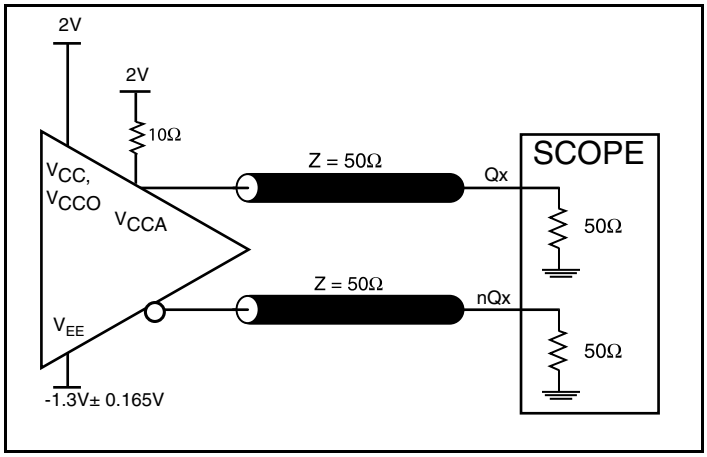
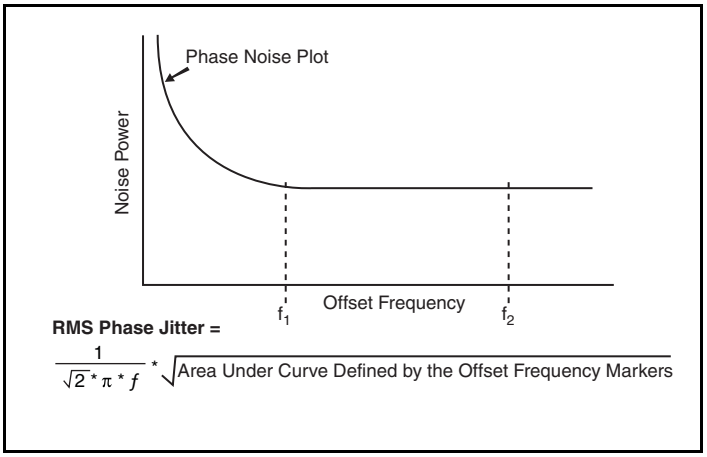
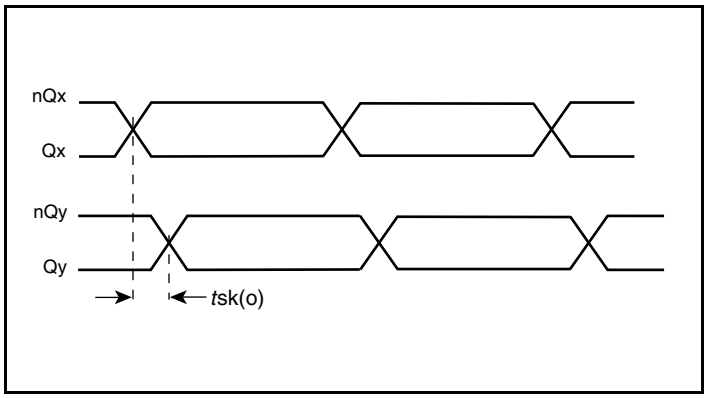
Parameter Measurement Information



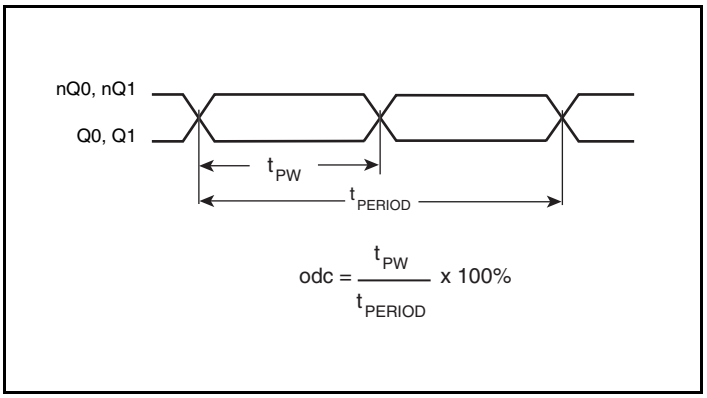
3.3V LVPECL Output Load Test Circuit



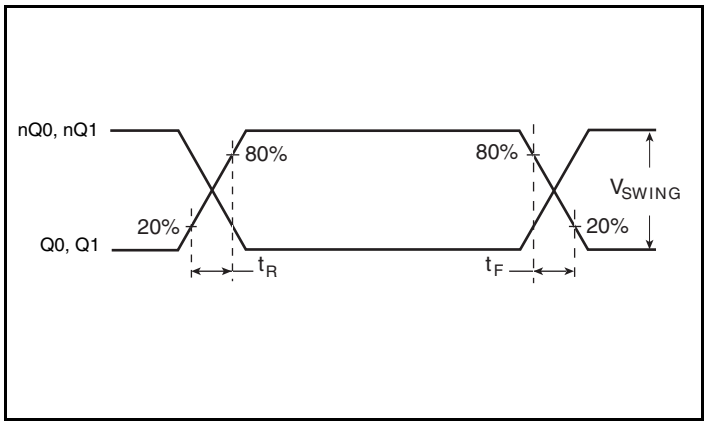
RMS Phase Jitter



Output Skew



LVPECL Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

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Applications Information

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

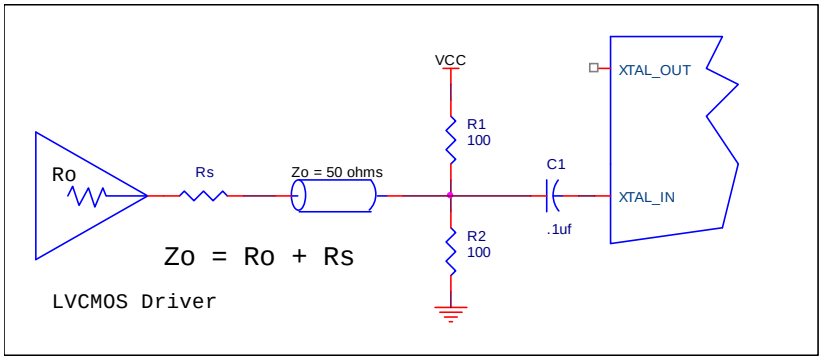

Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

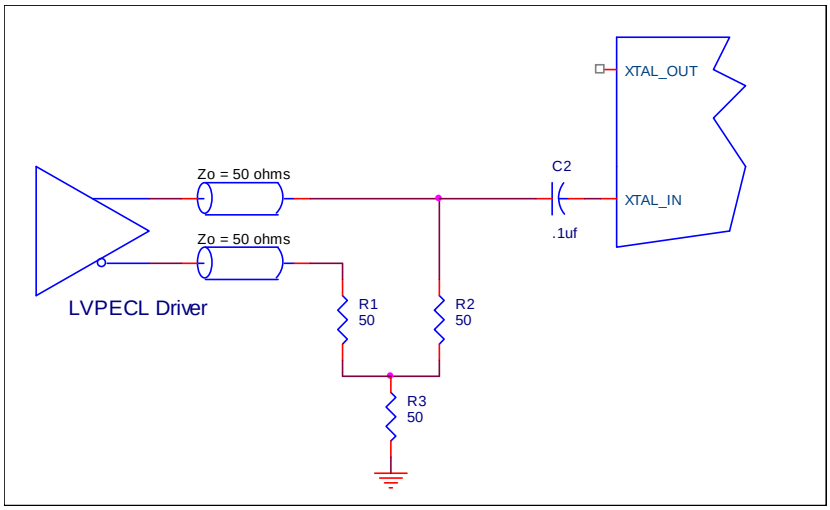

Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

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Recommendations for Unused Input Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS Control Pins

All control pins have internal pullup and pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

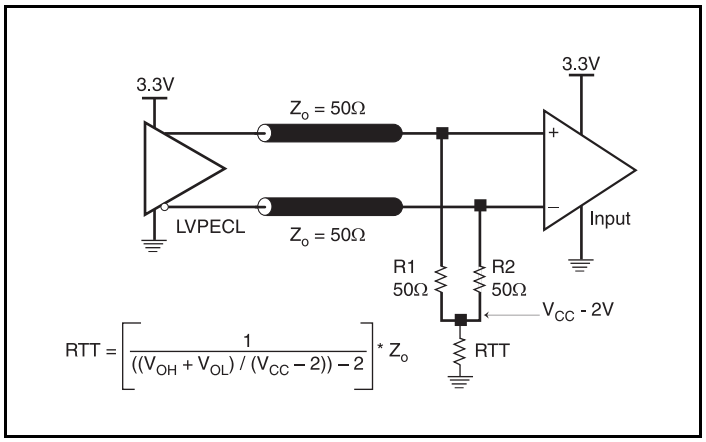

Figure 2A. 3.3V LVPECL Output Termination

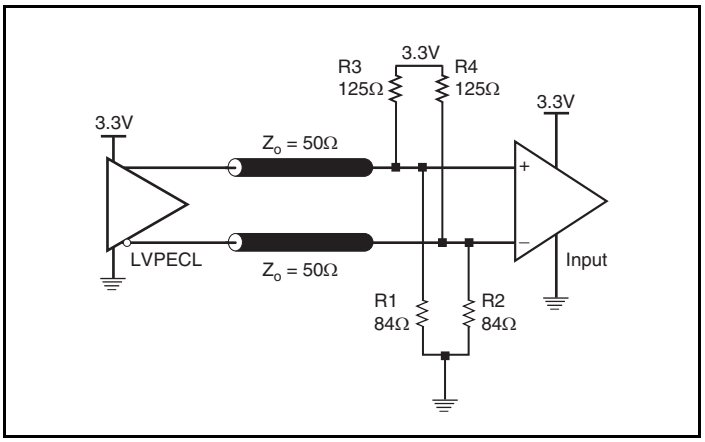

Figure 2B. 3.3V LVPECL Output Termination

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Schematic Example

Figure 3 (next page) shows an example of ICS843252-04 application schematic. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

In this example, the device is operated $V_{CC} = V_{CCA} = V_{CCO} = 3.3V$. The 12pF parallel resonant 25MHz crystal is used. The load capacitance C1 = C2 = 10pF are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. For this device, the crystal load capacitors are required for proper operation. Crystals with other load capacitance specifications can be used, but will require different values for C1 and C2.

Two LVPECL terminations are shown for the outputs, one is a standard DC termination and the other is an example of an AC termination, typically used when connecting a 3.3V LVPECL driver to a receiver operating at a lower supply voltage. For alternative terminations see the IDT application note “Termination – LVPECL”.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843252-04 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequency. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component with high amplitude interference is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally general design practice for power plane voltage stability suggests adding bulk capacitances in the general area of all devices.

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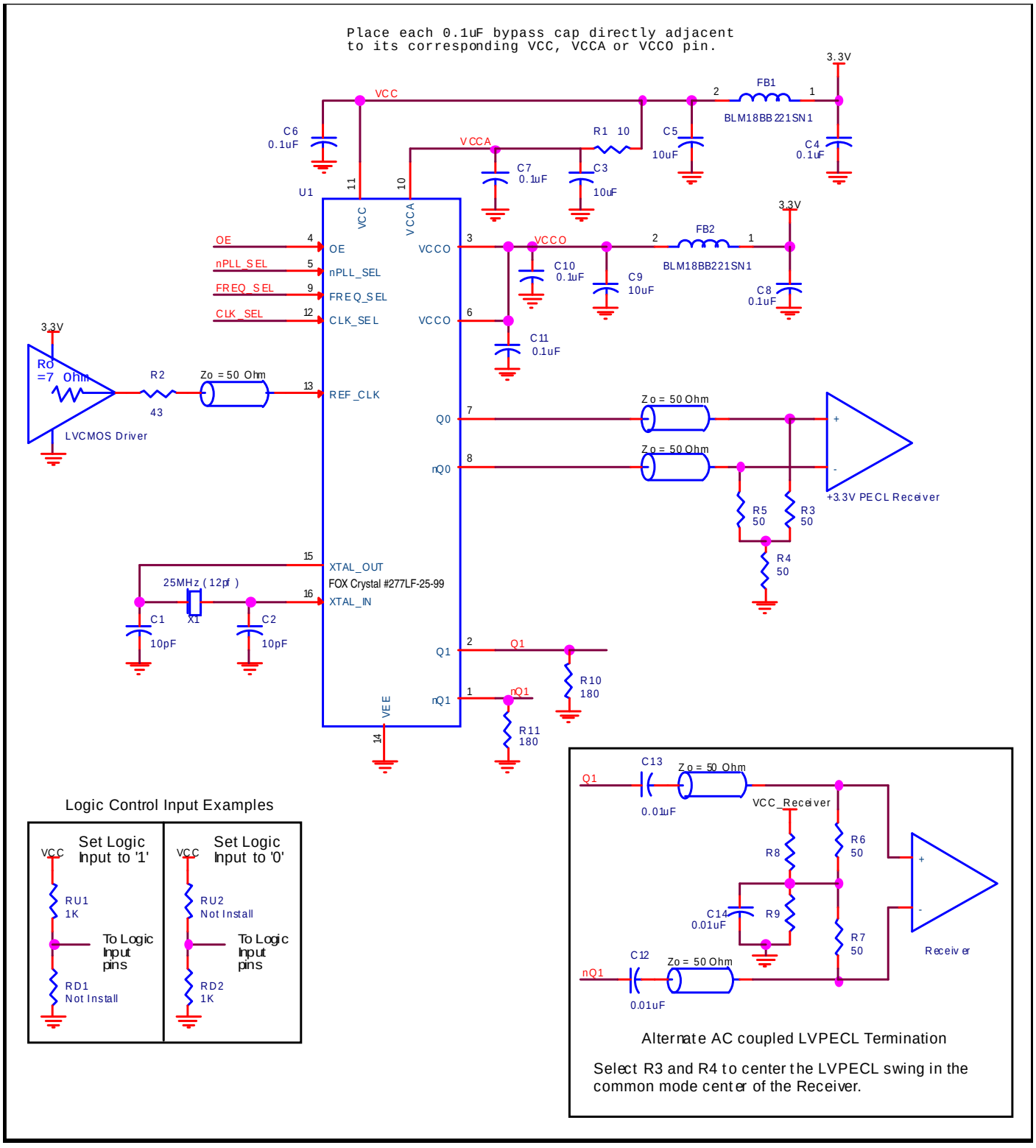

Figure 3. ICS843252-04 Schematic Layout

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Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843252-04.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843252-04 is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power $(core)_{MAX} = V_{CCO\_MAX} * I_{EE\_MAX}$ = 3.465V * 113mA = **391.5mW**

Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 391.5mW + 60mW = **451.5mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 81.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.452W * 81.2°C/W = 106.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.2°C/W	73.9°C/W	70.2°C/W

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3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

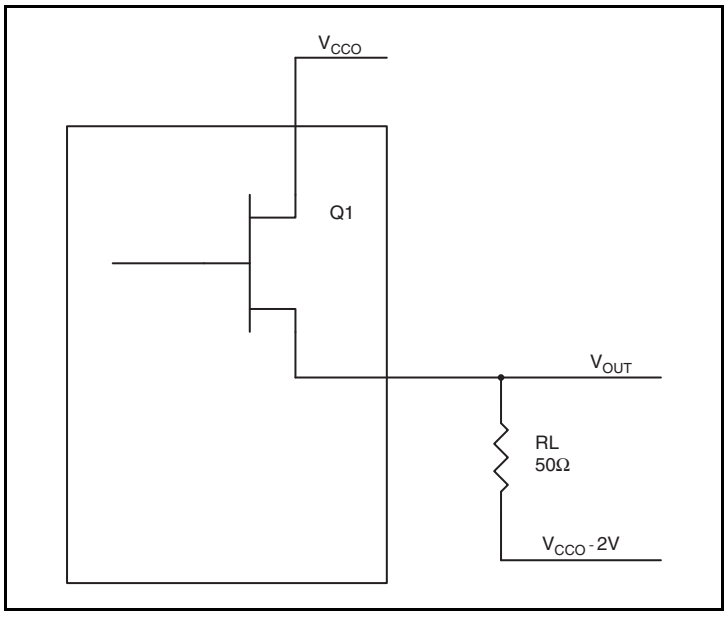

Figure 4. LVPECL Driver Circuit and Termination

To calculate power dissipation due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CCO_MAX} – 0.9V**
  ($V_{CCO\_MAX} - V_{OH\_MAX}$) = **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CCO_MAX} – 1.7V**
  ($V_{CCO\_MAX} - V_{OL\_MAX}$) = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_{L]} * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.2°C/W	73.9°C/W	70.2°C/W

Transistor Count

The transistor count for ICS843252-04 is: 2210

Package Outline and Package Dimensions

Package Outline - G Suffix for 16-Lead TSSOP

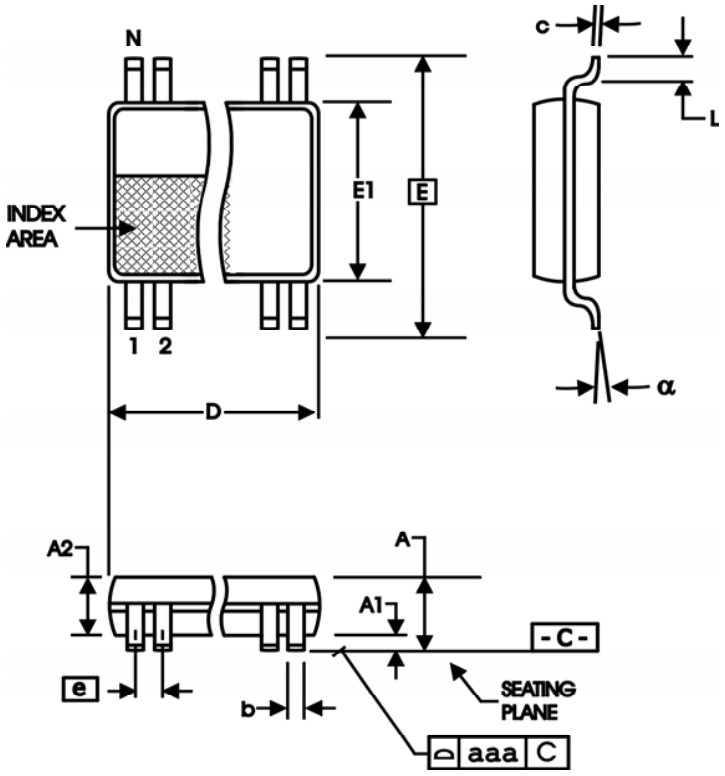

Table 8. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

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Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843252AG-04LF	3252A04L	“Lead-Free” Lead-Free, 16 Lead TSSOP	Tube	0°C to 70°C
843252AG-04LFT	3252A04L	“Lead-Free” Lead-Free, 16 Lead TSSOP	Tape & Reel	0°C to 70°C

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