## General Description

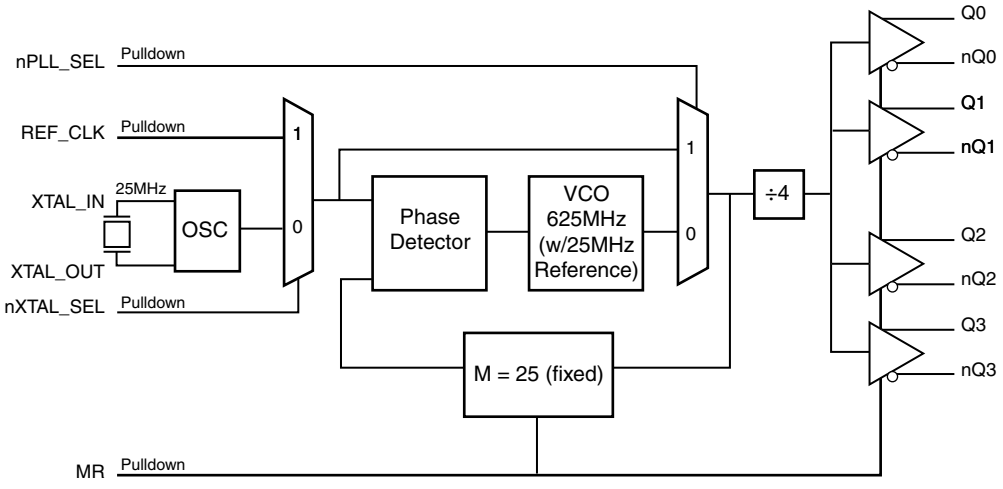
The ICS843004I-156 is a four output LVPECL synthesizer optimized to generate Ethernet reference clock frequencies. Using a 25MHz 18pF parallel resonant crystal, the ICS843004I-156 can generate 156.25MHz.

The ICS843004I-156 uses IDT's 3RD generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS843004I-156 is packaged in a small 24-pin TSSOP E-Pad package.

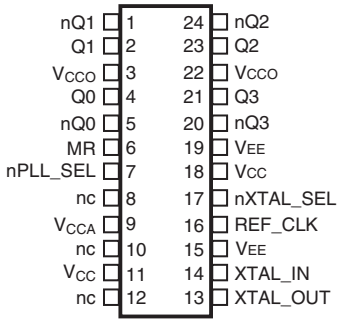
## Features

- Four 3.3V differential LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended clock input
- 156.25MHz output frequency
- VCO range: 560MHz – 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.49ps (typical)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram




## Pin Assignment




**ICS843004I-156**

**24-Lead TSSOP, E-Pad**
**4.4mm x 7.8mm x 0.925mm**
**package body**
**G Package**
**Top View**

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 2 | nQ1, Q1 | Output | | Differential output pair. LVPECL interface levels. |
| 3, 22 | $V_{CCO}$ | Power | | Output supply pins. |
| 4, 5 | Q0, nQ0 | Output | | Differential output pair. LVPECL interface levels. |
| 6 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 7 | nPLL_SEL | Input | Pulldown | Selects either the PLL or the active input reference to be routed to the output dividers. When LOW, selects PLL (PLL Enable). When HIGH, selects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels. |
| 8, 10,12 | nc | Unused | | No connect. |
| 9 | $V_{CCA}$ | Power | | Analog supply pin. |
| 11, 18 | $V_{CC}$ | Power | | Core supply pins. |
| 13, 14 | XTAL_OUT, XTAL_IN | Input | | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. |
| 15, 19 | $V_{EE}$ | Power | | Negative supply pins. |
| 16 | REF_CLK | Input | Pulldown | Single-ended reference clock input. LVCMOS/LVTTL interface levels. |
| 17 | nXTAL_SEL | Input | Pulldown | Selects between the single-ended REF_CLK or crystal interface as the PLL reference source. When HIGH, selects REF_CLK. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels. |
| 20, 21 | nQ3, Q3 | Output | | Differential output pair. LVPECL interface levels. |
| 23, 24 | Q2, nQ2 | Output | | Differential output pair. LVPECL interface levels. |

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$<br>XTAL_IN<br>Other Inputs | <br>0V to $V_{DD}$<br>-0.5V to $V_{DD}$ + 0.5V |
| Outputs, $I_O$ (LVPECL)<br>Continuous Current<br>Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 32.1°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,** $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | $V_{CC}$ – 0.13 | 3.3 | $V_{CC}$ | V |
| $V_{CCO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | | | | 120 | mA |
| $I_{CCA}$ | Analog Supply Current | Included in $I_{EE}$ | | | 13 | mA |

**Table 3B. Power Supply DC Characteristics,** $V_{CC} = V_{CCO} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{CCA}$ | Analog Supply Voltage | | $V_{CC}$ – 0.12 | 2.5 | $V_{CC}$ | V |
| $V_{CCO}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{EE}$ | Power Supply Current | | | | 110 | mA |
| $I_{CCA}$ | Analog Supply Current | Included in $I_{EE}$ | | | 12 | mA |

**Table 3C. LVCMOS/LVTTL DC Characteristics,** $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | $V_{CC} = 3.3V \pm 5\%$ | 2 | | $V_{CC} + 0.3$ | V |
| | | | $V_{CC} = 2.5V \pm 5\%$ | 1.7 | | $V_{CC} + 0.3$ | V |
| $V_{IL}$ | Input Low Voltage | | $V_{CC} = 3.3V \pm 5\%$ | -0.3 | | 0.8 | V |
| | | | $V_{CC} = 2.5V \pm 5\%$ | -0.3 | | 0.7 | V |
| $I_{IH}$ | Input High Current | REF_CLK, MR, nPLL_SEL, nXTAL_SEL | $V_{CC} = V_{IN} = 3.465V$ | | | 150 | µA |
| $I_{IL}$ | Input Low Current | REF_CLK, MR, nPLL_SEL, nXTAL_SEL | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -5 | | | µA |

**Table 3D. LVPECL DC Characteristics,** $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO} - 1.4$ | | $V_{CCO} - 0.9$ | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CCO} - 2.0$ | | $V_{CCO} - 1.7$ | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs termination with 50Ω to $V_{CCO} - 2V$.

**Table 3E. LVPECL DC Characteristics,** $V_{CC} = V_{CCO} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO} - 1.4$ | | $V_{CCO} - 0.9$ | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CCO} - 2.0$ | | $V_{CCO} - 1.5$ | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.4 | | 1.0 | V |

NOTE 1: Outputs termination with 50Ω to $V_{CCO} - 2V$.

**Table 4. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | | Fundamental | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: Characterized using an 18pF parallel resonant crystal.

# AC Electrical Characteristics

**Table 5A. AC Characteristics,** $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency Range | | | 156.25 | | MHz |
| *t*sk(o) | Output Skew; NOTE 1, 2 | | | | 50 | ps |
| *t*jit(Ø) | RMS Phase Jitter, (Random); NOTE 3 | 156.25MHz, (1.875MHz – 20MHz) | | 0.49 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 300 | | 600 | ps |
| odc | Output Duty Cycle | | 48 | | 52 | % |

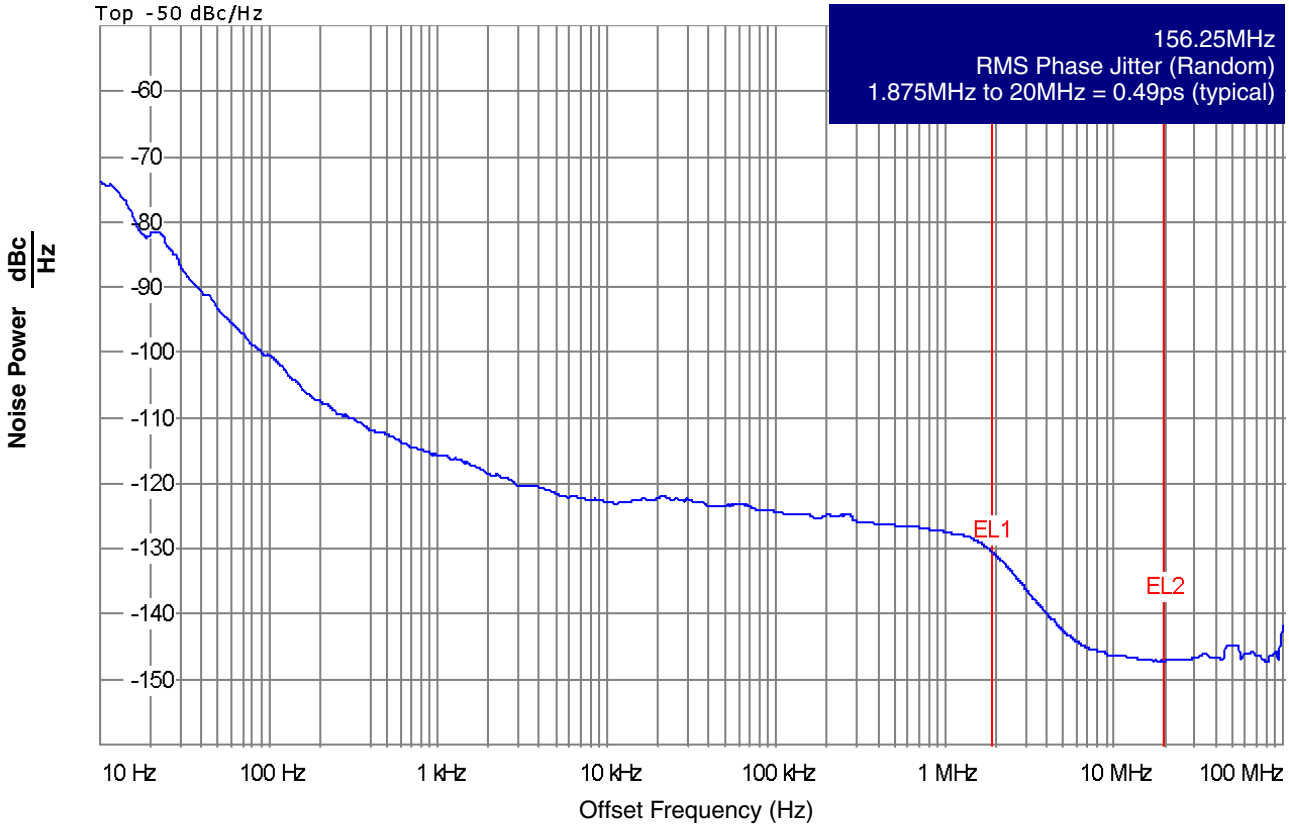
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

**Table 5B. AC Characteristics,** $V_{CC} = V_{CCO} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

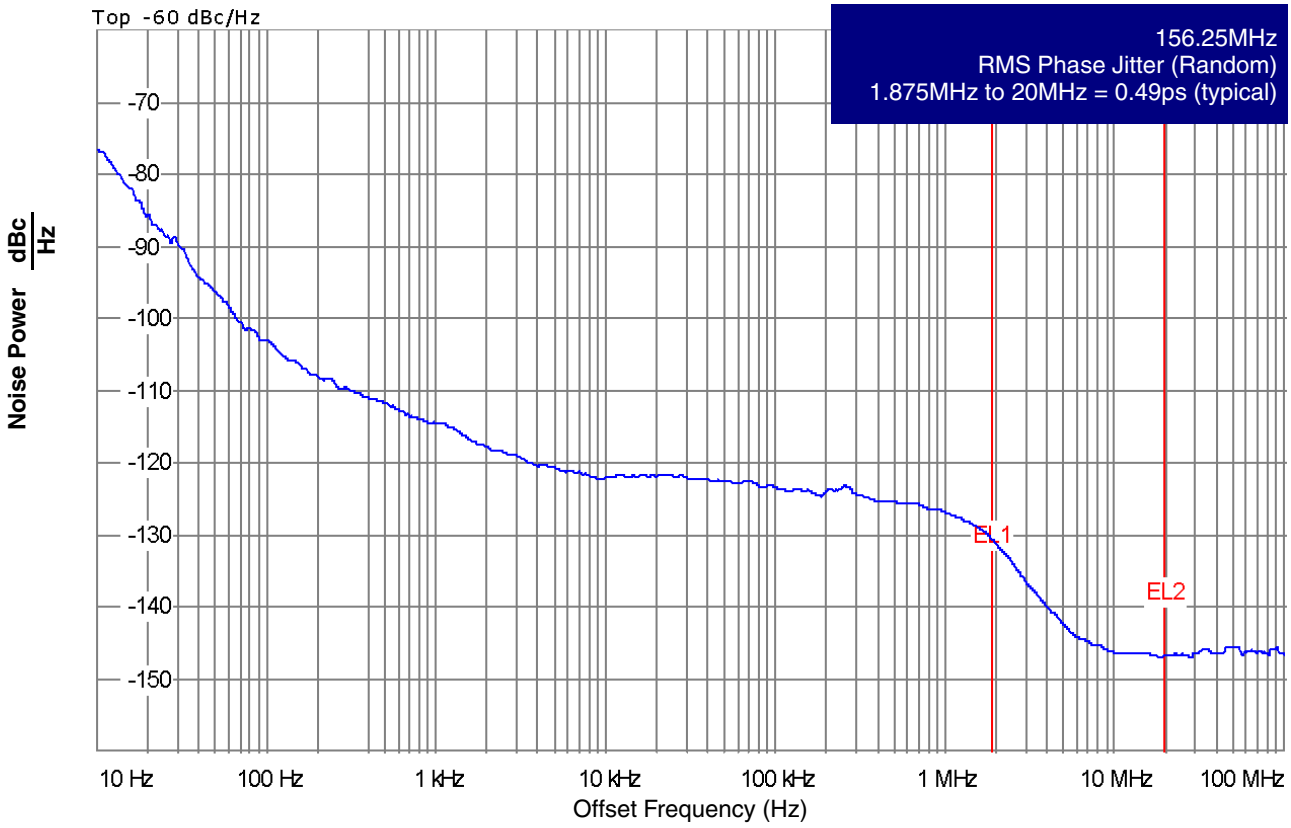
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency Range | | | 156.25 | | MHz |
| *t*sk(o) | Output Skew; NOTE 1, 2 | | | | 50 | ps |
| *t*jit(Ø) | RMS Phase Jitter, (Random); NOTE 3 | 156.25MHz, (1.875MHz – 20MHz) | | 0.49 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 300 | | 600 | ps |
| odc | Output Duty Cycle | | 48 | | 52 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

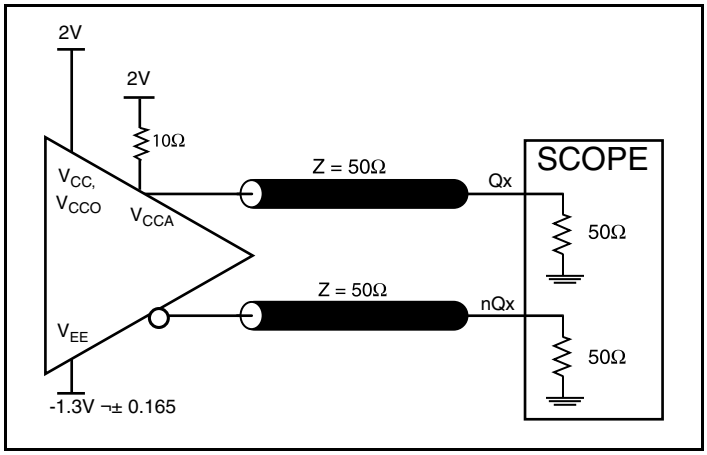
## Typical Phase Noise at 156.25MHz (3.3V)



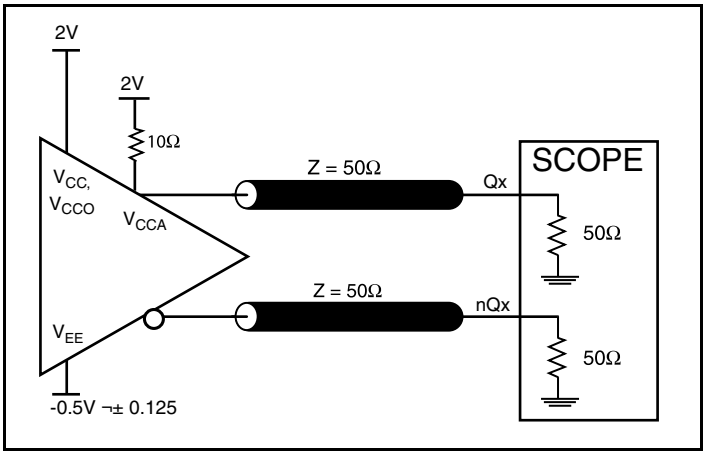

## Typical Phase Noise at 156.25MHz (2.5V)



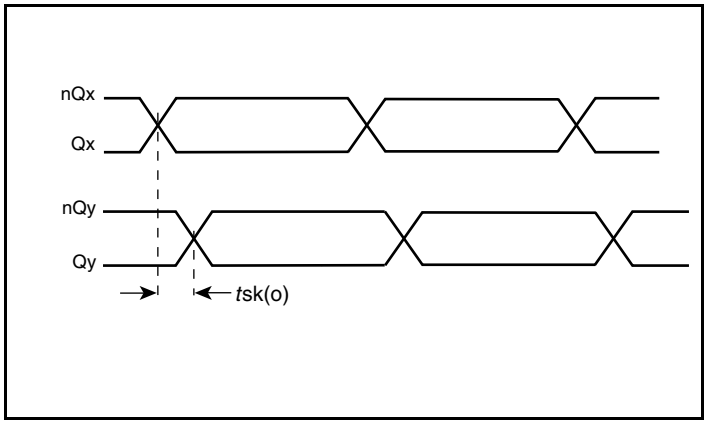
# Parameter Measurement Information



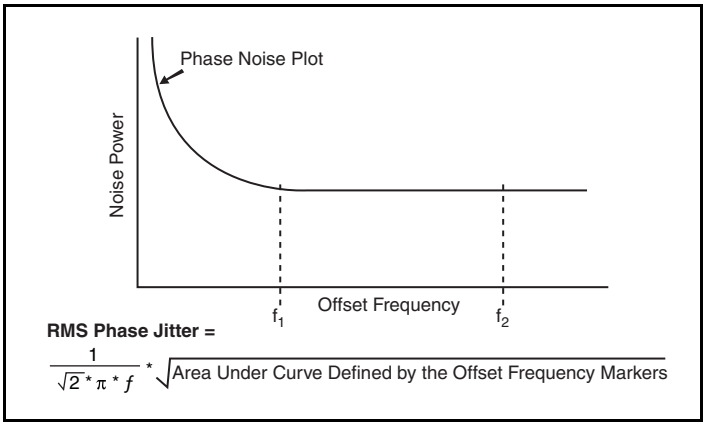

**3.3V LVPECL Output Load AC Test Circuit**



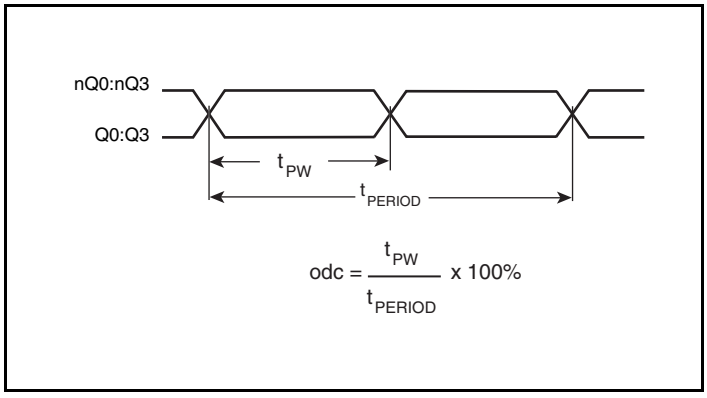

**2.5V LVPECL Output Load AC Test Circuit**



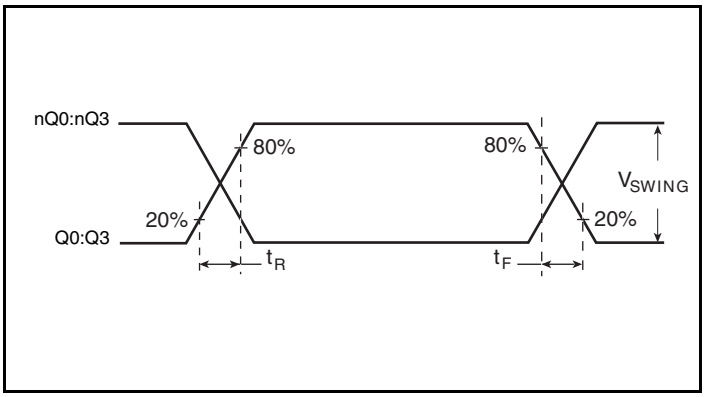

**Output Skew**




**RMS Phase Jitter**




**Output Duty Cycle/Pulse Width/Period**




**Output Rise/Fall Time**

# Applications Information

## Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

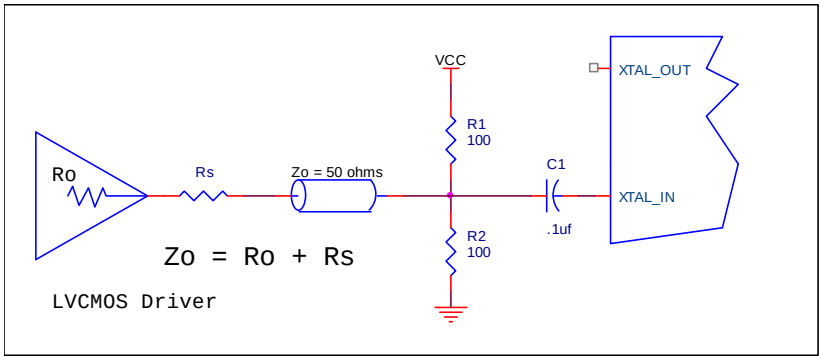



**Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface**

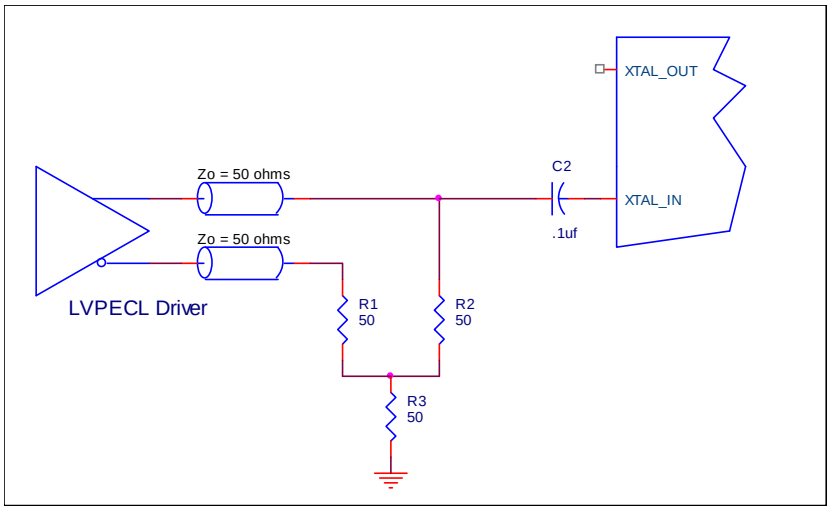



**Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

#### REF_CLK Input

For applications not requiring the use of a reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

#### LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

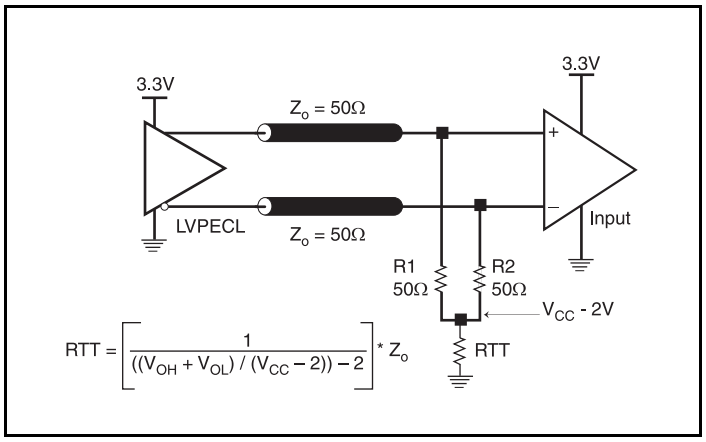



**Figure 2A. 3.3V LVPECL Output Termination**

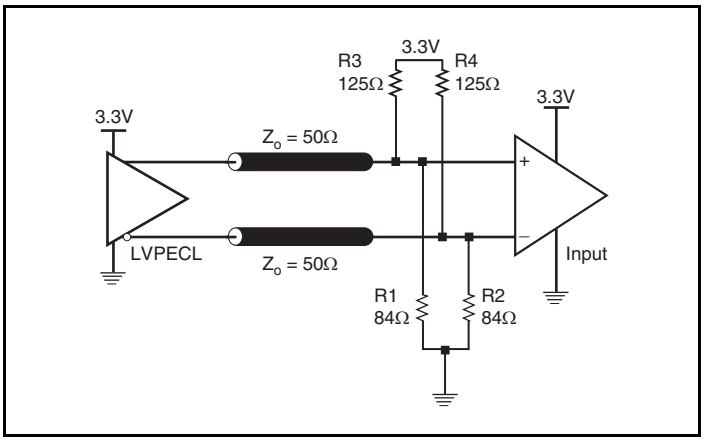



**Figure 2B. 3.3V LVPECL Output Termination**

## Termination for 2.5V LVPECL Outputs

*Figure 3A* and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CCO}$ – 2V. For $V_{CCO}$ = 2.5V, the $V_{CCO}$ – 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

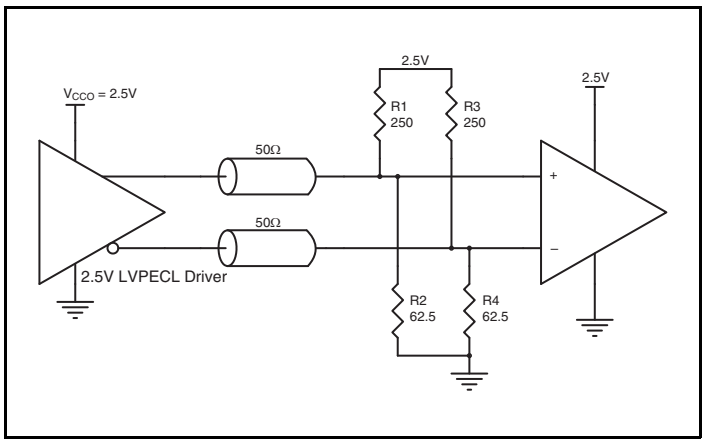



**Figure 3A. 2.5V LVPECL Driver Termination Example**

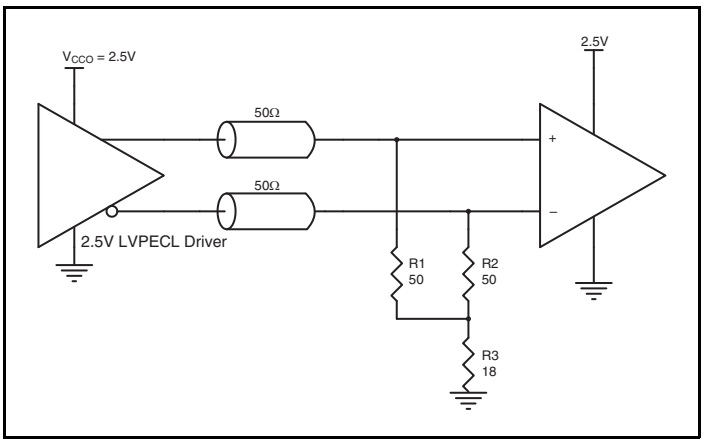



**Figure 3B. 2.5V LVPECL Driver Termination Example**

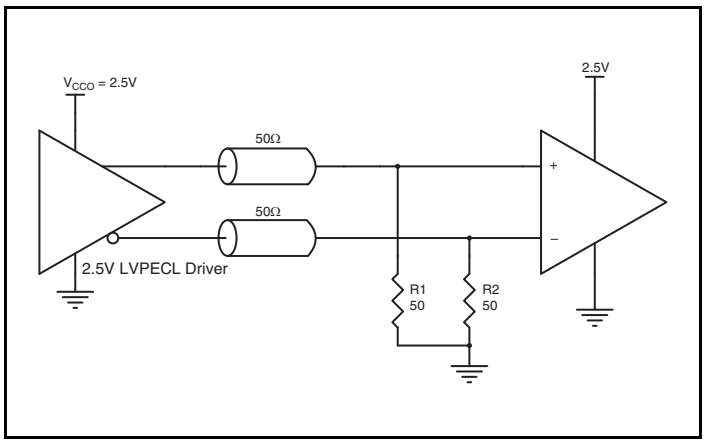



**Figure 3C. 2.5V LVPECL Driver Termination Example**

## EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

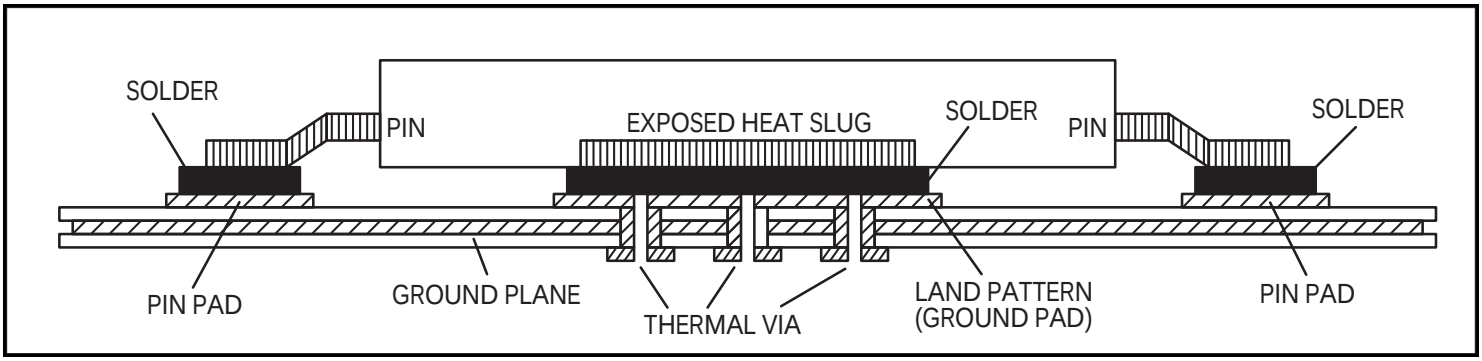



**Figure 4. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)**

## Schematic Example

*Figure 5* (next page) shows an example of ICS843004I-156 application schematic in which the device is operated at $V_{CC}$ = +3.3V. The schematic example focuses on functional connections and is intended as an example only and may not represent the exact user configuration. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. For example MR, nPLL_SEL and nXTAL_SEL can be configured from an FPGA instead of pull up and pull down resistors as shown.

There are three PECL termination options shown as examples of valid LVPECL terminations.

1. The simple three resistor termination of R5, R6 and R7 is easiest to layout and lowest power.

2. The standard four resistor LVPECL termination that explicitly realizes the $V_{CC}$ - 2V VTT termination voltage as a Thevinin equivalent. It is however higher power than the three resistor termination.

3. An AC termination, used when coupling the ICS843004I-156 LVPECL output stage to a different logic family receiver.

Note that in the AC termination the pull down resistors R8 and R9 that bias the LVPECL output stage are to be placed on the ICS843004I-156 side of the PCB directly adjacent to pins 21 and 20 for best signal integrity.

This device package has an ePAD that is connected to ground internally. The ePAD is to be connected to VEE/GND through vias in order to improve heat dissipation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise, so to achieve optimum jitter performance isolation of the $V_{CC}$ pin from power supply is required. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor on the $V_{CC}$ pin must be placed on the device side with direct return to the ground plane though vias. The remaining filter components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

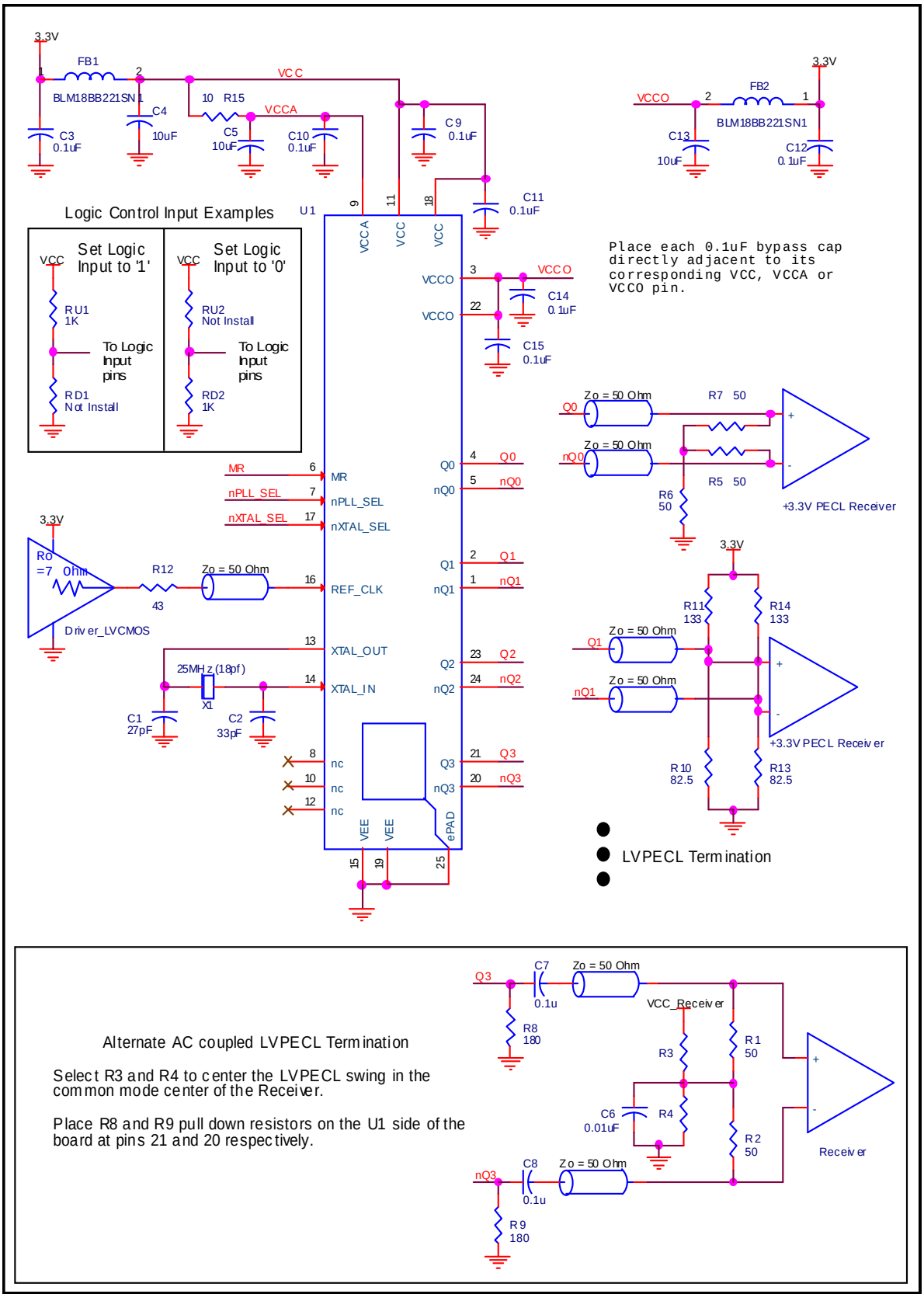



**Figure 5. ICS843004I-156 Application Schematic**

# Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843004I-156.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS843004I-156 is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 120mA = **415.8mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

**Total Power**$_{\_MAX}$ (3.465V, with all outputs switching) = 415.8mW + 120mW = **535.8mW**

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.536W * 32.1°C/W = 102.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance $\theta_{JA}$ for 24 Lead TSSOP, E-Pad, Forced Convection**

| $\theta_{JA}$ **vs. Air Flow** | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 32.1°C/W | 25.5°C/W | 24.0°C/W |

**3. Calculations and Equations.**

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 6.*

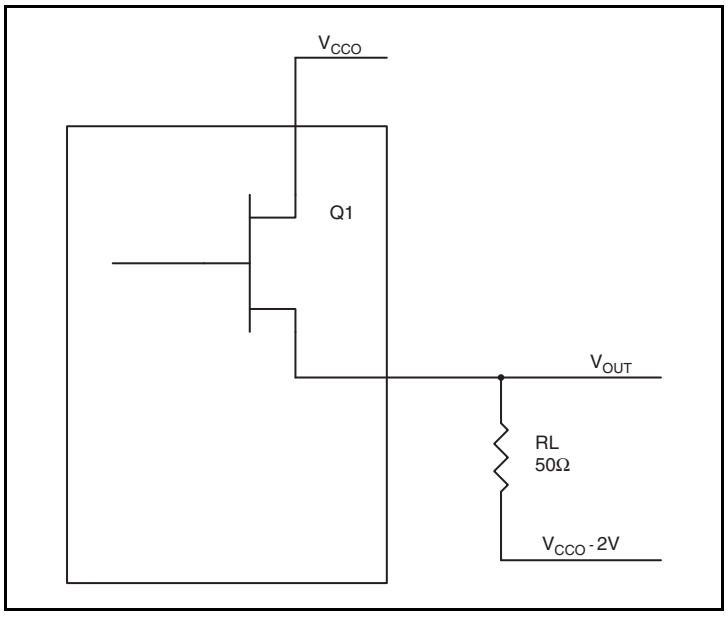



**Figure 6. LVPECL Driver Circuit and Termination**

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – 1.7V)/50Ω] * 1.7V =$ **10.20mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

# Reliability Information

**Table 7. $\theta_{JA}$ vs. Air Flow Table for a 24 Lead TSSOP, E-Pad**

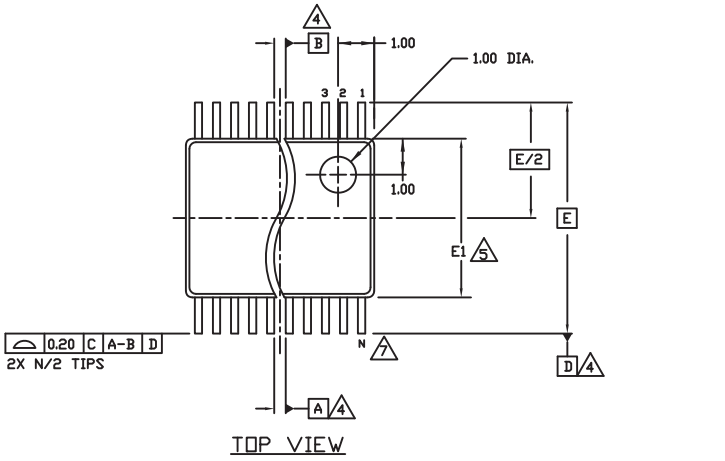
| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 32.1°C/W | 25.5°C/W | 24.0°C/W |

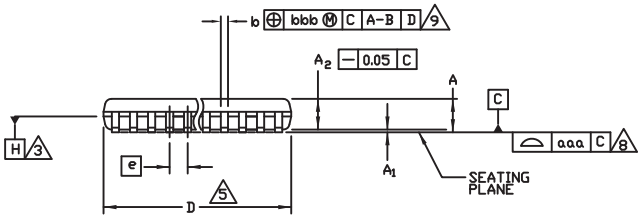
## Transistor Count

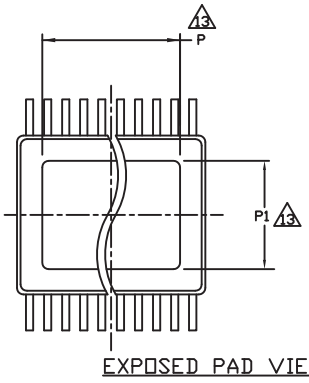
The transistor count for ICS843004I-156 is: 2906

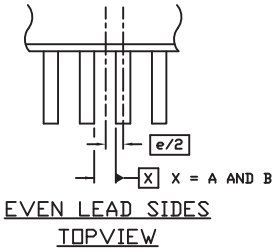
# Package Outline and Package Dimensions

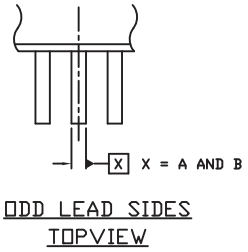
## Package Outline - G Suffix for 24 Lead TSSOP, E-Pad

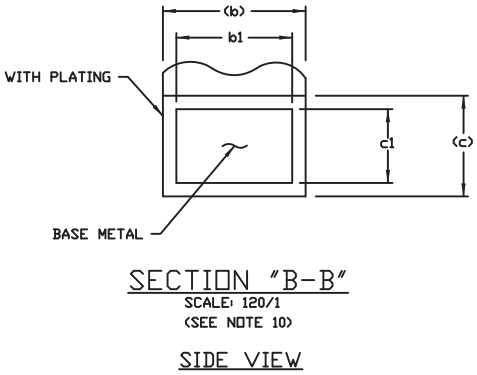


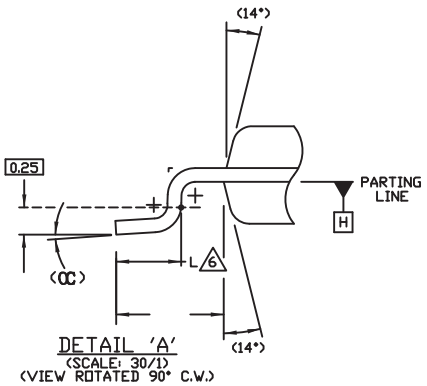



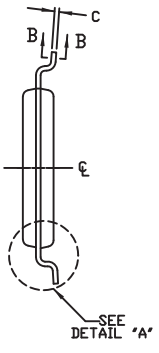




## Table 8. Package Dimensions

| All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 24 | |
| **A** | | 1.10 |
| **A1** | 0.05 | 0.15 |
| **A2** | 0.85 | 0.95 |
| **b** | 0.19 | 0.30 |
| **b1** | 0.19 | 0.25 |
| **c** | 0.09 | 0.20 |
| **c1** | 0.09 | 0.16 |
| **D** | 7.70 | 7.90 |
| **E** | 6.40 Basic | |
| **E1** | 4.30 | 4.50 |
| **e** | 0.65 Basic | |
| **L** | 0.50 | 0.70 |
| **P** | 5.0 | 5.5 |
| **P1** | 3.0 | 3.2 |
| α | 0° | 8° |
| **aaa** | 0.076 | |
| **bbb** | 0.10 | |

Reference Document: JEDEC Publication 95, MO-153

# Ordering Information

**Table 9. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 843004AGI-156LF | ICS3004AI56L | “Lead-Free” 24 Lead TSSOP, E-Pad | Tube | -40°C to 85°C |
| 843004AGI-156LFT | ICS3004AI56L | “Lead-Free” 24 Lead TSSOP, E-Pad | Tape & Reel | -40°C to 85°C |

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