

## GENERAL DESCRIPTION

The 843004-125 is a 4 output LVPECL Synthesizer optimized to generate Ethernet reference clock frequencies and is a member of the family of high performance clock solutions from IDT. The 843004-125 uses IDT's 3<sup>rd</sup> generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The 843004-125 is packaged in a small 24-pin TSSOP package.

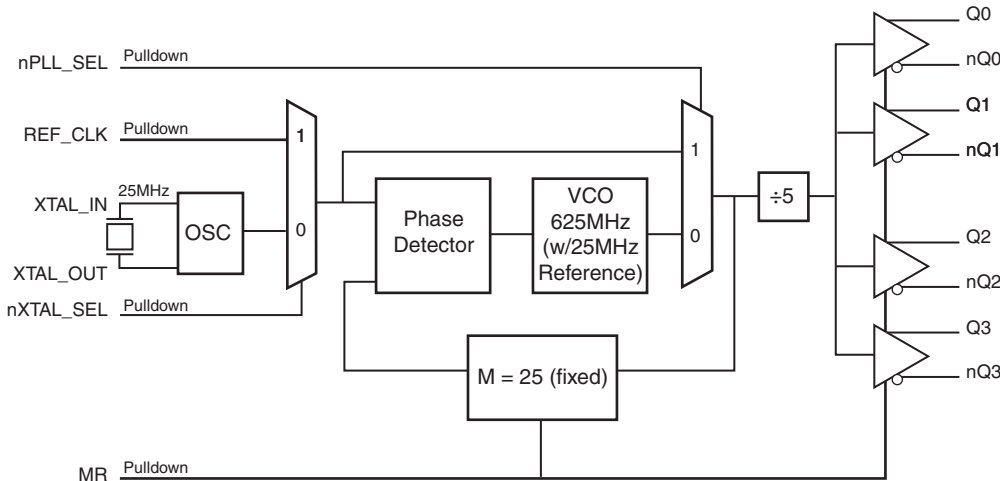
## FEATURES

- Four 3.3V LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Crystal oscillator designed for 25MHz, 18pF parallel resonant crystal
- Supports the following output frequency: 125MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.58ps (typical)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

FREQUENCY SELECT FUNCTION TABLE

Inputs			Output Frequency (MHz) (25MHz Ref.)
M Divider Value	N Divider Value	M/N Divider Value	
25	5	5	125

## BLOCK DIAGRAM



## PIN ASSIGNMENT

nQ1	1	24	nQ2
Q1	2	23	Q2
Vcco	3	22	Vcco
Q0	4	21	Q3
nQ0	5	20	nQ3
MR	6	19	VEE
nPLL_SEL	7	18	Vcc
nc	8	17	nXTAL_SEL
VCCA	9	16	REF_CLK
nc	10	15	VEE
Vcc	11	14	XTAL_IN
nc	12	13	XTAL_OUT

**843004-125**  
**24-Lead TSSOP**

4.40mm x 7.8mm x 0.925mm  
package body  
**G Package**  
Top View

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
3, 22	V <sub>CCO</sub>	Power		Output supply pins.
4, 5	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	Selects between the PLL and REF_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
8, 10, 12	nc	Unused		No connect.
9	V <sub>CCA</sub>	Power		Analog supply pin.
11, 18	V <sub>CC</sub>	Power		Core supply pins.
13, 14	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
15, 19	V <sub>EE</sub>	Power		Negative supply pins.
16	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
17	nXTAL_SEL	Input	Pulldown	Selects between crystal or REF_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects REF_CLK when HIGH. LVCMOS/LVTTL interface levels.
20, 21	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
23, 24	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.

NOTE: refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	82.3°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.15$	3.3	$V_{CC}$	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				130	mA
$I_{CCA}$	Analog Supply Current	Included in $I_{EE}$			15	mA

**TABLE 3B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	REF_CLK, MR, nPLL_SEL, nXTAL_SEL $V_{CC} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	REF_CLK, MR, nPLL_SEL, nXTAL_SEL $V_{CC} = 3.465V$ , $V_{IN} = 0V$	-5			$\mu A$

**TABLE 3C. LVPECL DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ .

**TABLE 4. CRYSTAL CHARACTERISTICS**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF, parallel resonant crystal.

**TABLE 5. AC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		112	125	136	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2				50	ps
$t_{jit}(\emptyset)$	RMS Phase Jitter; NOTE 3	125MHz (1.875MHz - 20MHz)		0.58		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300		600	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditons.

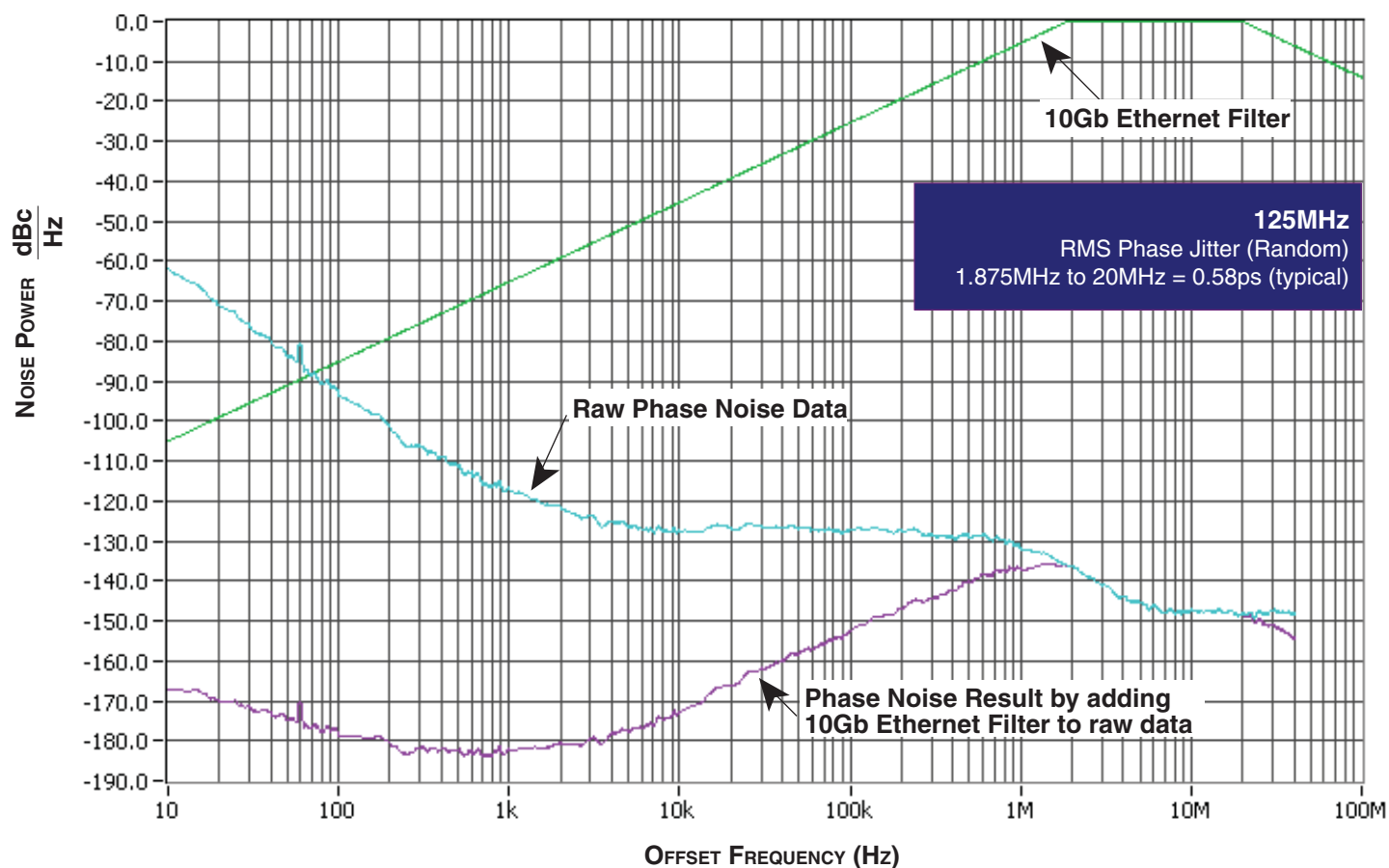
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at the differential cross points.

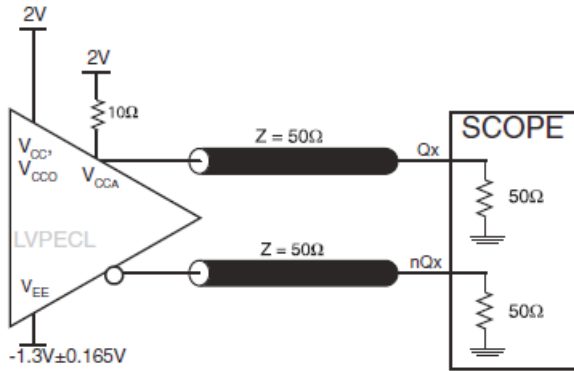
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Phase jitter is dependent on the input source used.

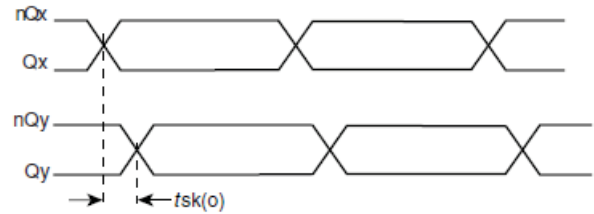
## TYPICAL PHASE NOISE AT 125MHz



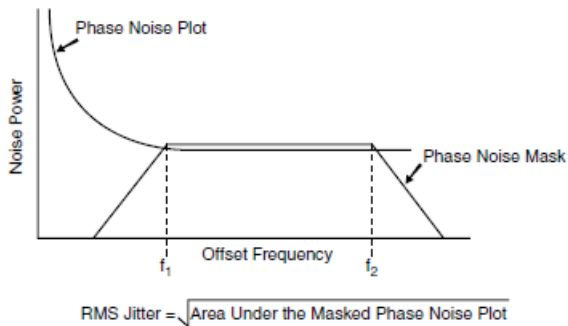
## PARAMETER MEASUREMENT INFORMATION



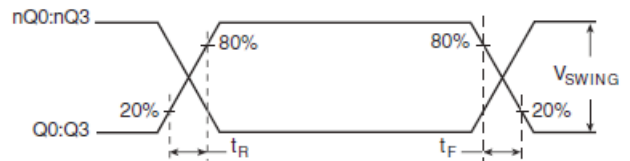
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



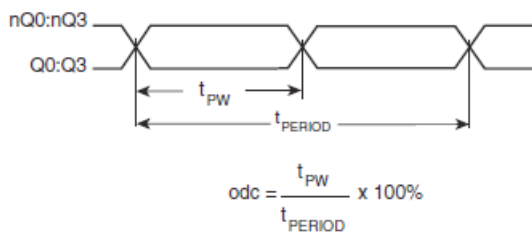
OUTPUT SKEW



RMS PHASE JITTER



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843004-125 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$  and  $V_{CCO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{CC}$  pin and also shows that  $V_{CCA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{CCA}$  pin.

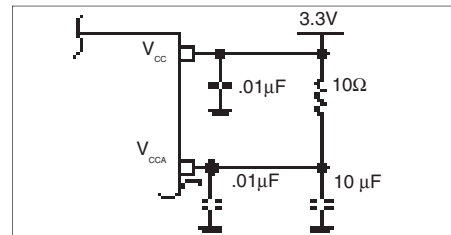


FIGURE 1. POWER SUPPLY FILTERING

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from XTAL\_IN to ground.

##### REF\_CLK INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from the REF\_CLK to ground.

##### LVC MOS CONTROL PINS

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

#### OUTPUTS:

##### LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

### CRYSTAL INPUT INTERFACE

The 843004-125 has been characterized with  $18\text{pF}$  parallel resonant crystals. The capacitor values shown in *Figure 2* below

were determined using a  $25\text{MHz}$ ,  $18\text{pF}$  parallel resonant crystal and were chosen to minimize the ppm error.

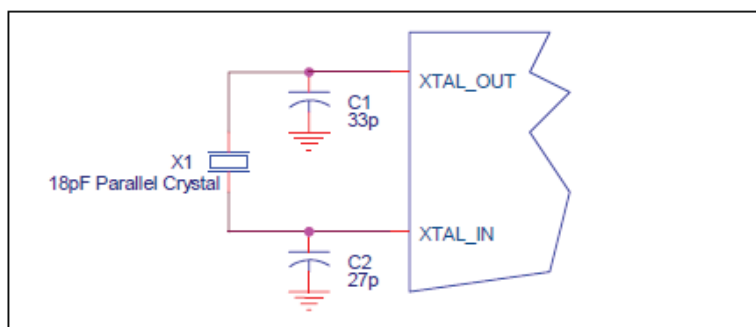


FIGURE 2. CRYSTAL INPUT INTERFACE

## LVC MOS TO XTAL INTERFACE

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in Figure 3. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω.

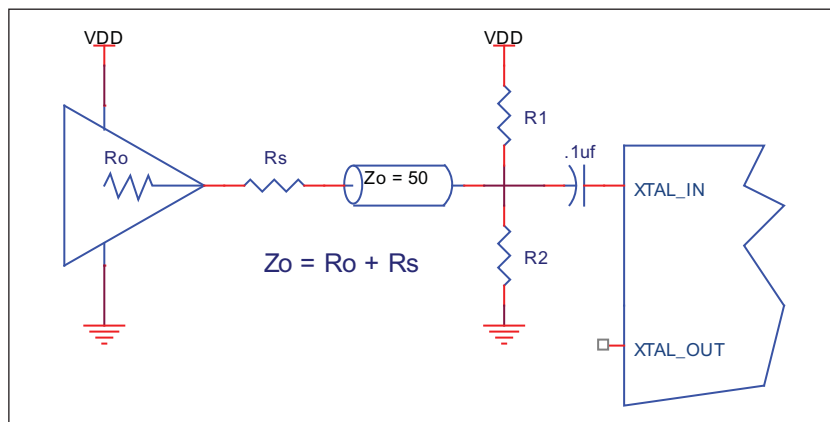


FIGURE 3. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

## TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission

lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 4A and 4B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

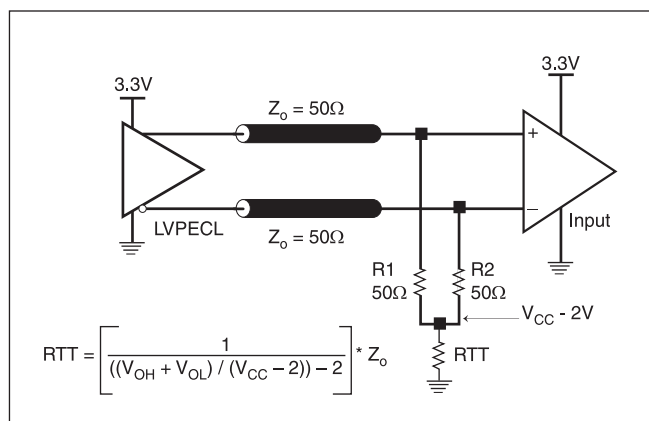


FIGURE 4A. LVPECL OUTPUT TERMINATION

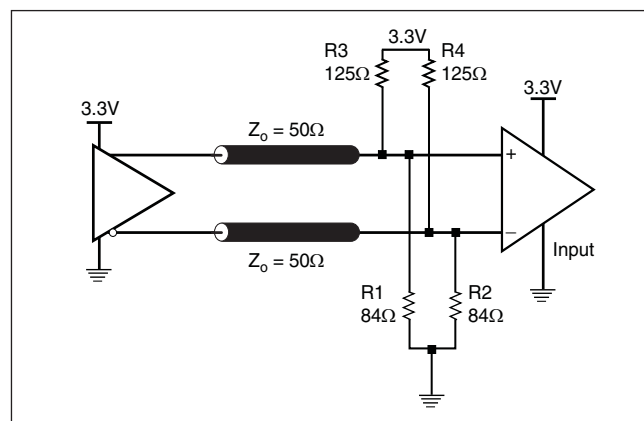


FIGURE 4B. LVPECL OUTPUT TERMINATION

## LAYOUT GUIDELINE

Figure 5 shows an example of 843004-125 application schematic. In this example, the device is operated at  $V_{cc} = V_{cco} = 3.3V$ . The 18pF parallel resonant 25MHz crystal is used. The  $C1 = 33pF$  and  $C2 = 27pF$  are recommended for frequency accuracy. For different

board layout, the  $C1$  and  $C2$  may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL terminations are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

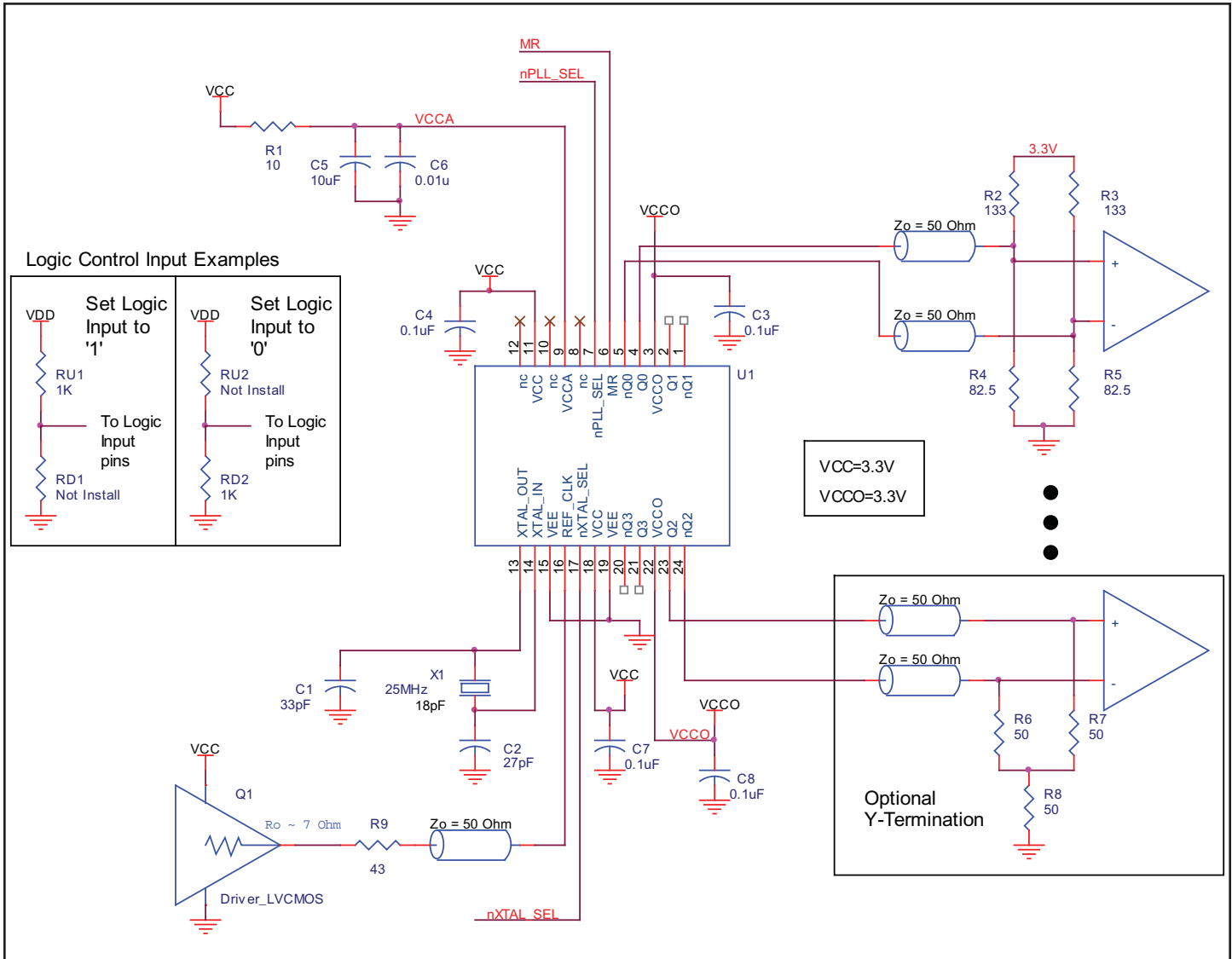


FIGURE 5. ICS843004-01 SCHEMATIC EXAMPLE

# POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843004-125. Equations and example calculations are also provided.

## 1. Power Dissipation.

The total power dissipation for the 843004-125 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 130mA = 450.45mW$

- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $4 * 30mW = 120mW$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $450.45mW + 120mW = 570.45mW$

## 2. Junction Temperature.

Junction temperature, T<sub>J</sub>, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T<sub>J</sub> is as follows:  $T_J = \theta_{JA} * Pd\_total + T_A$

T<sub>J</sub> = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Pd<sub>total</sub> = Total Device Power Dissipation (example calculation is in section 1 above)

T<sub>A</sub> = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 82.3°C/W per Table 6 below.

Therefore, T<sub>J</sub> for an ambient temperature of 70°C with all outputs switching is:  
 $70^\circ C + 0.570W * 82.3^\circ C/W = 116.9^\circ C$ . This is below the limit of 125°C.

This calculation is only an example. T<sub>J</sub> will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 24-PIN TSSOP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.9°C/W

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 6.

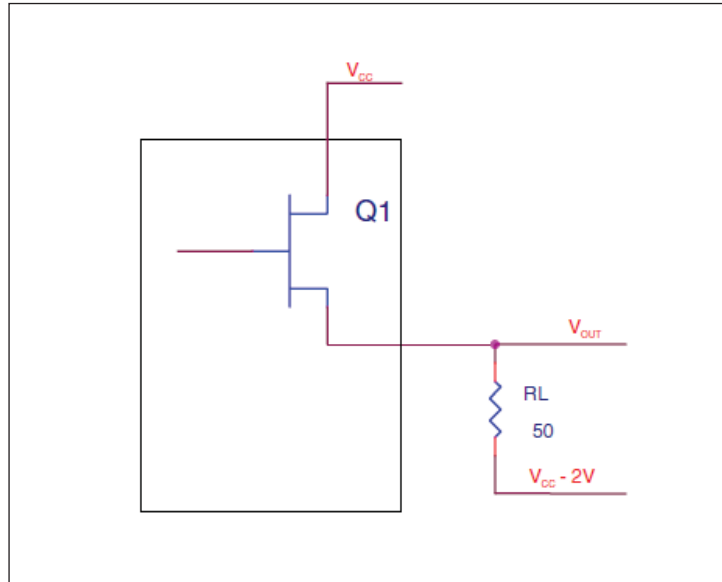


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.9V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 0.9V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$

$$(V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$$

$$[(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$$

$$[(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30mW$$

# RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.9°C/W

## TRANSISTOR COUNT

The transistor count for 843004-125 is: 2894

# PACKAGE OUTLINE AND DIMENSIONS

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

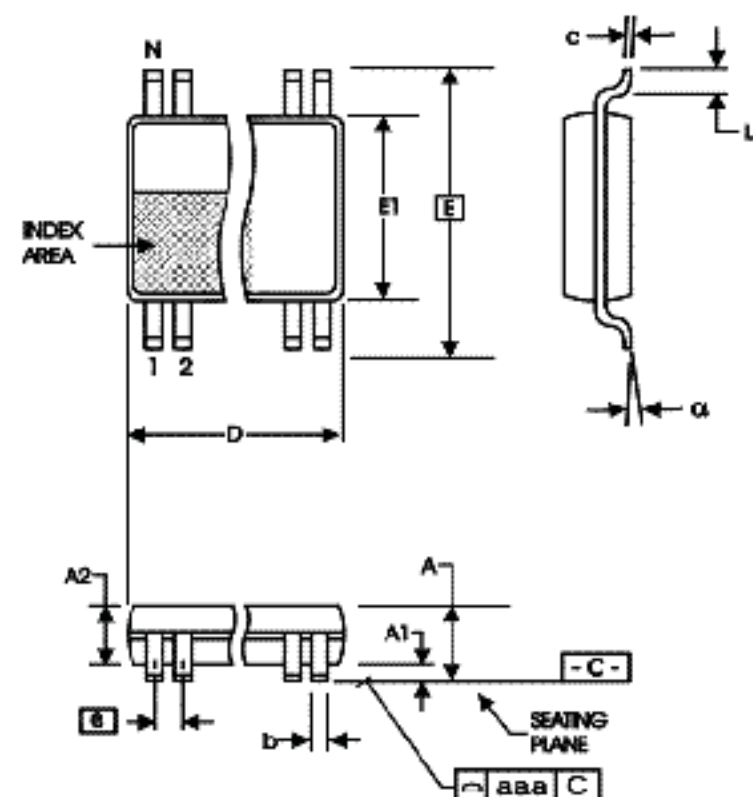


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

**TABLE 9. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843004AG-125LF	ICS43004A125L	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
843004AG-125LFT	ICS43004A125L	24 Lead "Lead-Free" TSSOP	tape & reel	0°C to 70°C

# REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
A	T9	1 13	Removed ICS from the part number where needed. General Description - Removed ICS Chip and Hipercllocks. Ordering Information - Removed quantity from tape and reel. Deleted LF note below the table. Updated Header and footer.	1/18/16



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.