## HS-302AEH

## Radiation Hardened BiCMOS Dual DPST Analog Switch

The HS-302AEH is a dual Double-Pole, Single-Throw (DPST) analog switch fabricated using the Renesas dielectrically isolated Radiation Hardened Silicon Gate (RSG) process technology to ensure latch-up free operation. The HS-302AEH is pin compatible and functionally equivalent to the HS-302RH.

The HS-302AEH offers convenient switching controlled by 5 V digital inputs and low-resistance switching performance for analog voltages up to the supply rails. ON-resistance is low and stays reasonably constant across the full range of operating voltage and current and as over exposure to radiation.

The HS-302AEH is available in a 14 Ld CDFP or die form and operates across the extended temperature range of $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.

## Applications

- Signal processing applications
- Power supply control


Figure 1. Logic Circuit

Table 1. Truth Table

| Logic | All Switches |
| :---: | :---: |
| 0 | OFF |
| 1 | ON |

## Features

- Electrically screened to DLA SMD\# 5962-95812
- No latch-up, dielectrically isolated device islands
- Pin and functionally compatible with Renesas HS-302RH series analog switches
- Analog signal range equal to the supply voltage range
- Low leakage: 150nA (maximum, post-rad)
- Low ron: $60 \Omega$ (maximum, post-rad)
- Low standby supply current: $\pm 150 \mu \mathrm{~A}$ (maximum, post-rad)
- Radiation assurance (Note 1)
- High dose rate (50 to 300rad(Si)/s): 100krad(Si)
- Low dose rate (0.01rad(Si)/s): 50krad(Si)
- Single event effects
- SEE for LET $=60 \mathrm{MeV} \cdot \mathrm{cm}^{2} / \mathrm{mg}$ at $60^{\circ}$ incident angle, $<150$ pC charge transferred to the output of an off switch (based on SOI design calculations) Note:

1. Product capability established by initial characterization. Acceptance tested on a wafer-by-wafer basis to $50 \mathrm{krad}(\mathrm{Si})$ at low dose rate.


Figure 2. ron vs Signal Level vs Temperature

## 1. Overview

### 1.1 Pin Configuration

14 Ld Flatpack, CDFP3-F14
Top View


### 1.2 Pin Descriptions

| Pin Number | Pin Name |  |
| :---: | :---: | :--- |
| 1 | NC | Not electrically connected |
| 2 | S3 | Analog switch: source connection |
| 5 | S1 |  |
| 10 | S2 |  |
| 13 | S4 |  |
| 3 | D3 | Analog switch: drain connection |
| 4 | D1 |  |
| 11 | D2 |  |
| 12 | D4 |  |
| 6 | IN1 | Digital control input for SW1 and SW3 |
| 7 | GND | Ground |
| 8 | V- | Negative power supply |
| 9 | IN2 | Digital control input for SW2 and SW4 |
| 14 | VID | Positive power supply |
| N/A | Electrically floating |  |

### 1.3 Ordering Information

| Ordering SMD Number (Note 3) | Part Number (Note 2) | Radiation Hardness (Total lonizing Dose) | Package (RoHS Compliant) | Pkg. Dwg. \# | Temp. Range |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 5962R9581205VXC | HS9-302AEH-Q | HDR to $100 \mathrm{krad}(\mathrm{Si})$ LDR to $50 \mathrm{krad}(\mathrm{Si})$ | 14 Ld Flatpack | K14.A | -55 to $+125^{\circ} \mathrm{C}$ |
| 5962R9581205V9A | HS0-302AEH-Q (Note 4) |  | Die | N/A |  |
| N/A | HS9-302AEH/PROTO (Note 5) | N/A | 14 Ld Flatpack | K14.A |  |
| N/A | HS0-302AEH/SAMPLE ( Notes 4, 5) |  | Die | N/A |  |

## Notes:

2. These Pb-free Hermetic packaged products employ $100 \%$ Au plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb -free soldering operations.
3. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
4. Die product tested at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in Electrical Specifications.
5. The /PROTO and /SAMPLE are not rated or certified for Total lonizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive $100 \%$ screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

## 2. Specifications

### 2.1 Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Unit |
| :---: | :---: | :---: | :---: |
| Voltage Between V+ and V- Terminals |  | 35 | V |
| $\pm \mathrm{V}_{\text {SUPPLY }}$ to Ground (V+, V -) |  | $\pm 17.5$ | V |
| Analog Input Voltage |  |  |  |
| $\left(+\mathrm{V}_{\mathrm{S}}\right)$ |  | $+\mathrm{V}_{\text {SUPPLY }}+1.5$ | V |
| $\left(-\mathrm{V}_{\mathrm{S}}\right)$ |  | - $\mathrm{V}_{\text {SUPPLY }}-1.5$ | V |
| Digital Input Voltage |  |  |  |
| $\left(+\mathrm{V}_{\mathrm{A}}\right)$ |  | $+\mathrm{V}_{\text {SUPPLY }}+4$ | V |
| $\left(-\mathrm{V}_{\mathrm{A}}\right)$ |  | $-V_{\text {SUPPLY }}-4$ | V |
| Peak Current (S or D), (Pulse at 1ms, 10\% Duty Cycle Max) |  | 40 | mA |
| Continuous Current |  | 10 | mA |
| ESD Rating | Value |  | Unit |
| Human Body Model (Tested per MIL-PRF-883 TM 3015.7) | 2 |  | kV |
| Machine Model (Tested per EIA/JESD22-A115-A) | 200 |  | V |
| Charged Device Model (Tested per JESD22-C101D) | 1 |  | kV |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

### 2.2 Thermal Information

| Thermal Resistance (Typical) | $\boldsymbol{\theta}_{\mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ | $\boldsymbol{\theta}_{\mathrm{JC}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ |
| :--- | :---: | :---: |
| Flatpack Package $(\underline{\text { Notes 6, }} \mathbf{7})$ | 105 | 17 |

Notes:
6. $\theta_{J A}$ is measured in free air with the component mounted on a low-effective thermal conductivity test board in free air. See TB379.
7. For $\theta_{\mathrm{JC}}$, the "case temp" location is the center of the package underside.

| Parameter | Minimum | Maximum | Unit |
| :--- | :---: | :---: | :---: |
| Package Power Dissipation at $125^{\circ} \mathrm{C}$, Flatpack Package |  | 0.48 | W |
| Junction Temperature $\left(T_{J}\right)$ |  | +175 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | -65 | +150 | ${ }^{\circ} \mathrm{C}$ |

### 2.3 Recommended Operation Conditions

| Parameter | Minimum | Maximum | Unit |
| :--- | :---: | :---: | :---: |
| Operating Temperature Range | -55 | +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Supply Voltage Range $\left( \pm \mathrm{V}_{\text {SUPPLY }}\right)$ |  | $\pm 15$ | V |
| Analog Input Voltage $\left(\mathrm{V}_{\mathrm{S}}\right)$ | 0 | $\pm \mathrm{V}_{\text {SUPPLY }}$ | V |
| Logic Low Level $\left(\mathrm{V}_{\mathrm{AL}}\right)$ | 4.0 | 0.8 | V |
| Logic High Level $\left(\mathrm{V}_{\mathrm{AH}}\right)$ |  | $+\mathrm{V}_{\text {SUPPLY }}$ | V |

### 2.4 Electrical Specifications

$V_{\text {SUPPLY }}= \pm 15 \mathrm{~V}$ unless otherwise specified. Boldface limits either apply across the operating temperature range $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ or across a total ionizing dose of $100 \mathrm{krad}(\mathrm{Si})$ with exposure of a high dose rate of 50 to $300 \mathrm{rad}(\mathbf{S i}) / \mathrm{s}$ and a total ionizing dose of $50 \mathrm{krad}(\mathrm{Si})$ with exposure at a low dose rate of $<10 \mathrm{mrad}(\mathrm{Si}) / \mathrm{s}$.

| Parameter | Symbol | Test Conditions | $\begin{gathered} \text { Min } \\ \text { (Note 8) } \end{gathered}$ | Typ | Max (Note 8) <br> (Note 8 ) | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Switch On-Resistance | +r ${ }_{\text {DS }}(\mathrm{ON})$ | $\mathrm{V}_{\mathrm{D}}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{S}}=-10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | - | 50 | $\Omega$ |
|  |  | $\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | - | 35 | 75 | $\Omega$ |
|  |  | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, post radiation | - | - | 60 | $\Omega$ |
| Switch On-Resistance | $-^{\text {r }}$ D(ON) | $\mathrm{V}_{\mathrm{D}}=-10 \mathrm{~V}, \mathrm{I}_{\mathrm{S}}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | - | 50 | $\Omega$ |
|  |  | $\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | - | 35 | 75 | $\Omega$ |
|  |  | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, post radiation | - | - | 60 | $\Omega$ |
| Leakage Current into Source Terminal of an OFF Switch | ${ }^{+} \mathrm{I}_{\text {S(OFF) }}$ | $\mathrm{V}_{S}=+14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -100 | - | 100 | nA |
|  |  | $\mathrm{V}_{S}=+14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | -150 | 0.05 | 150 | nA |
|  |  | $\mathrm{V}_{S}=+14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | -150 | - | 150 | nA |
|  |  | $\mathrm{V}_{S}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -1 | - | 1 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{S}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | -20 | - | 20 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{S}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | -20 | - | 20 | $\mu \mathrm{A}$ |
| Leakage Current into Source Terminal of an OFF Switch | ${ }^{-1}$ S(OFF) | $\mathrm{V}_{S}=-14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -100 | - | 100 | nA |
|  |  | $V_{S}=-14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | -150 | 0.05 | 150 | nA |
|  |  | $\mathrm{V}_{S}=-14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | -150 | - | 150 | nA |
|  |  | $\mathrm{V}_{S}=-15 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -1 | - | 1 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{S}=-15 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | -20 | - | 20 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{S}=-15 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | -20 | - | 20 | $\mu \mathrm{A}$ |
| Leakage Current into Drain Terminal of an OFF Switch | ${ }^{+l_{\text {D(OFF })}}$ | $\mathrm{V}_{S}=+14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -100 | - | 100 | nA |
|  |  | $\mathrm{V}_{\mathrm{S}}=+14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | -150 | 0.05 | 150 | nA |
|  |  | $\mathrm{V}_{S}=+14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | -150 | - | 150 | nA |
|  |  | $\mathrm{V}_{S}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -1 | - | 1 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{S}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | -20 | - | 20 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{S}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | -20 | - | 20 | $\mu \mathrm{A}$ |
| Leakage Current into Drain Terminal of an OFF Switch | $-^{\text {d (OFF) }}$ | $\mathrm{V}_{S}=-14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -100 | - | 100 | nA |
|  |  | $\mathrm{V}_{S}=-14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | -150 | 0.5 | 150 | nA |
|  |  | $\mathrm{V}_{S}=-14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | -150 | - | 150 | nA |
|  |  | $\mathrm{V}_{\mathrm{S}}=-15 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -1 | - | 1 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{S}=-15 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | -20 | - | 20 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{S}=-15 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+15 \mathrm{~V}, \mathrm{~T}_{A}=+25^{\circ} \mathrm{C}$, post radiation | -20 | - | 20 | $\mu \mathrm{A}$ |
| Leakage Current from an ON Driver into the Switch (Drain and Source) | $+_{\text {d(ON) }}$ | $\mathrm{V}_{S}=+14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -20 | - | 20 | nA |
|  |  | $\mathrm{V}_{\mathrm{S}}=+14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | -100 | -0.1 | 100 | nA |
|  |  | $\mathrm{V}_{\mathrm{S}}=+14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=+14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \text {, post }$ radiation | -100 | - | 100 | nA |
| Leakage Current from an ON Driver into the Switch (Drain and Source) | ${ }^{-\mathrm{I}_{\text {(ON }}}$ | $\mathrm{V}_{S}=-14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -20 | - | 20 | nA |
|  |  | $V_{S}=-14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-14 \mathrm{~V}, \mathrm{~T}_{A}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | -100 | -0.1 | 100 | nA |
|  |  | $\mathrm{V}_{S}=-14 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=-14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | -100 | - | 100 | nA |

$V_{\text {SUPPLY }}= \pm 15 \mathrm{~V}$ unless otherwise specified. Boldface limits either apply across the operating temperature range $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ or across a total ionizing dose of $100 \mathrm{krad}(\mathrm{Si})$ with exposure of a high dose rate of 50 to $\mathbf{3 0 0} \mathrm{rad}(\mathbf{S i}) / \mathrm{s}$ and a total ionizing dose of $50 \mathrm{krad}(\mathrm{Si})$ with exposure at a low dose rate of $<10 \mathrm{mrad}(\mathrm{Si}) / \mathrm{s}$. (Continued)

| Parameter | Symbol | Test Conditions | Min (Note 8) | Typ | Max <br> (Note 8) | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Low Level Input Address Current | $\mathrm{I}_{\text {AL }}$ | All Channels $\mathrm{V}_{\mathrm{A}}=0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | -1 | - | 1 | $\mu \mathrm{A}$ |
|  |  | All Channels $\mathrm{V}_{\mathrm{A}}=0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | -1 | - | 1 | $\mu \mathrm{A}$ |
| High Level Input Address Current | $\mathrm{I}_{\text {AH }}$ | All Channels $\mathrm{V}_{\mathrm{A}}=4.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | -1 | - | 1 | $\mu \mathrm{A}$ |
|  |  | All Channels $\mathrm{V}_{\mathrm{A}}=4.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | -1 | - | 1 | $\mu \mathrm{A}$ |
| Positive Supply Current | I+ | All Channels $\mathrm{V}_{\mathrm{A}}=0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | - | 100 | $\mu \mathrm{A}$ |
|  |  | All Channels $\mathrm{V}_{\mathrm{A}}=0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | - | 45 | 150 | $\mu \mathrm{A}$ |
|  |  | All Channels $\mathrm{V}_{\mathrm{A}}=0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | - | - | 150 | $\mu \mathrm{A}$ |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{A} 1}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 2}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 1}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 2}=0 \mathrm{~V}, \\ & \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \end{aligned}$ | - | - | 0.4 | mA |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{A} 1}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 2}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 1}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 2}=0 \mathrm{~V}, \\ & \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | - | 0.15 | 0.6 | mA |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{A} 1}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 2}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 1}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 2}=0 \mathrm{~V}, \\ & \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \text {, post radiation } \end{aligned}$ | - | - | 0.6 | mA |
| Negative Supply Current | I- | All Channels $\mathrm{V}_{\mathrm{A}}=0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | - | -10 | $\mu \mathrm{A}$ |
|  |  | All Channels $\mathrm{V}_{\mathrm{A}}=0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | - | -0.1 | -100 | $\mu \mathrm{A}$ |
|  |  | All Channels $\mathrm{V}_{\mathrm{A}}=0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | - | - | -100 | $\mu \mathrm{A}$ |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{A} 1}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 2}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 1}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 2}=0 \mathrm{~V}, \\ & \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \end{aligned}$ | - | - | -10 | $\mu \mathrm{A}$ |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{A} 1}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 2}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 1}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 2}=0 \mathrm{~V}, \\ & \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | - | -0.1 | -100 | $\mu \mathrm{A}$ |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{A} 1}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 2}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 1}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{A} 2}=0 \mathrm{~V}, \\ & \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \text {, post radiation } \end{aligned}$ | - | - | -100 | $\mu \mathrm{A}$ |
| Switch Input Capacitance | $\mathrm{C}_{\text {IS (OFF) }}$ | From Source to GND (Note 9) | - | - | 28 | pF |
| Driver Input Capacitance | $\mathrm{C}_{\mathrm{C} 1}$ | $\mathrm{V}_{\mathrm{A}}=0 \mathrm{~V}$ ( Note 9) | - | - | 10 | pF |
| Driver Input Capacitance | $\mathrm{C}_{\mathrm{C} 2}$ | $\mathrm{V}_{\mathrm{A}}=15 \mathrm{~V}$ ( Note 9) | - | - | 10 | pF |
| Switch Output | $\mathrm{Cos}^{\text {S }}$ | Measured Drain to GND ( Note 9) | - | - | 32 | pF |
| Off Isolation | $V_{\text {ISO }}$ | $\mathrm{V}_{\mathrm{GEN}}=1 \mathrm{~V}_{\text {P-P }, ~} \mathrm{f}=1 \mathrm{MHz}$ ( Note 9) | 40 | - | - | dB |
| Cross Talk | $\mathrm{V}_{\mathrm{CR}}$ | $\mathrm{V}_{\mathrm{GEN}}=1 \mathrm{~V}_{\text {P-P },} \mathrm{f}=1 \mathrm{MHz}$ ( $\underline{\text { Note 9 }}$ ) | 40 | - | - | dB |
| Charge Transfer Error | $\mathrm{V}_{\text {CTE }}$ | $\mathrm{V}_{\mathrm{S}}=\mathrm{GND}, \mathrm{C}_{\mathrm{L}}=0.01 \mu \mathrm{~F}(\underline{\text { Note 9 }}$ ) | - | - | 15 | mV |
| Switch Turn-On Time | $\mathrm{t}_{\mathrm{ON}}$ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=300 \Omega, \mathrm{~V}_{\mathrm{S}}=3 \mathrm{~V}, \mathrm{~V}_{\mathrm{AH}}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{AL}}=0 \mathrm{~V}, \\ & \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \end{aligned}$ | - | - | 375 | ns |
|  |  | $\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | - | 250 | 500 | ns |
|  |  | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | - | - | 1 | $\mu \mathrm{s}$ |
| Switch Turn-Off Time | $\mathrm{t}_{\text {OFF }}$ | $\mathrm{R}_{\mathrm{L}}=300 \Omega, \mathrm{~V}_{\mathrm{S}}=3 \mathrm{~V}, \mathrm{~V}_{\mathrm{AH}}=4 \mathrm{~V}, \mathrm{~V}_{\mathrm{AL}}=0 \mathrm{~V}$ | - | - | 300 | ns |
|  |  | $\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | - | 200 | 450 | ns |
|  |  | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, post radiation | - | - | 1 | $\mu \mathrm{s}$ |

## Notes:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
9. $\mathrm{V}_{\mathrm{AL}}=0 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{AH}}=4 \mathrm{~V}$.

## 3. Test Circuits and Waveforms

### 3.1 Switching Times



Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 3. Switching Times Measurement Points


Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 5. Charge Transfer Error Measurement Points



Repeat test for all switches. $C_{L}$ includes fixture and stray capacitance.

$$
V_{\mathrm{OUT}}=V_{(\mathrm{NO} \text { or } \mathrm{NC})} \frac{R_{\mathrm{L}}}{R_{\mathrm{L}}+\mathrm{r}_{\mathrm{ON}}}
$$

Figure 4. Switching Times Test Circuit


Repeat test for all switches. $C_{L}$ includes fixture and stray capacitance.

Figure 6. Charge Transfer Error Test Circuit


Figure 8. $\mathrm{r}_{\mathrm{ON}}$ Test Circuit


Figure 9. Crosstalk Test Circuit


Figure 10. Capacitance Test Circuit

## 4. Typical Performance Curves

$\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=$ Open, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise specified.


Figure 11. $\mathrm{r}_{\mathrm{ON}}$ vs Signal Level vs Temperature


Figure 13. $\mathrm{t}_{\mathrm{ON}}$ and $\mathrm{t}_{\mathrm{OFF}}$ vs Temperature


Figure 15. $\mathrm{t}_{\text {OFF }}$ vs Temperature vs Supply Voltages


Figure 12. $\mathrm{r}_{\mathrm{ON}}$ vs Signal Level vs Supply Voltages


Figure 14. $\mathrm{t}_{\mathrm{ON}}$ vs Temperature vs Supply Voltages


Figure 16. $\mathrm{t}_{\mathrm{ON}}$ and $\mathrm{t}_{\mathrm{OFF}}$ vs Temperature
$\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=$ Open, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise specified. (Continued)


Figure 17. Frequency Response vs Frequency


Figure 19. $\mathbf{V}_{\mathrm{IH}} / \mathrm{V}_{\mathrm{IL}}$ vs Temperature vs Supply Voltages


Figure 18. Off Isolation vs Frequency


Figure 20. I+ vs Logic In

## 5. Die Characteristics

## Table 2. Die and Assembly Related Information

| Die Information |  |
| :--- | :--- |
| Dimensions | $2815 \mu \mathrm{~m} \times 5325 \mu \mathrm{~m}(110.83 \mathrm{mils} \times 209.65 \mathrm{mils})$ <br> Thickness: $483 \mu \mathrm{~m} \pm 25.4 \mu \mathrm{~m}(19 \mathrm{mils} \pm 1 \mathrm{mil})$ |
| Interface Materials | Type: PSG (Phosphorous Silicon Glass) <br> Thickness: $8.0 \mathrm{k} \AA \pm 1.0 \mathrm{k} \AA$ |
| Glassivation | Type: AlSiCu <br> Thickness: $16.0 \mathrm{k} \AA \pm 2 \mathrm{k} \AA$ |
| Top Metallization | Silicon |
| Backside Finish | Radiation Hardened Silicon Gate, <br> Dielectric Isolation |
| Substrate |  |
| Assembly Information | Unbiased (DI) |
| Substrate Potential |  |
| Additional Information | 348 |
| Worst Case Current Density | Floating |
| Transistor Count |  |

## 6. Metallization Mask Layout



### 6.1 Layout Characteristics

Step and Repeat: $2815 \mu \mathrm{mx} 5325 \mu \mathrm{~m}$
Table 3. Layout $X-Y$ Coordinates

| Pad Name | $\mathbf{X}(\mu \mathrm{m})$ | $\mathbf{Y}(\mu \mathrm{m})$ | $\mathbf{D X}(\mu \mathrm{m})$ | $\mathbf{D Y}(\boldsymbol{\mu m})$ |
| :---: | :---: | :---: | :---: | :---: |
| S3 | 0 | 4672.5 | 109 | 109 |
| D3 | -4.5 | 3861 | 109 | 109 |
| D1 | -4.5 | 1314 | 109 | 109 |
| S1 | 0 | 617.5 | 109 | 109 |
| IN1 | 0 | 0 | 109 | 109 |
| GND | 878 | 0 | 109 | 109 |
| V- | 1246 | 0 | 109 | 109 |
| S2 | 2124 | 617.5 | 109 | 109 |
| D2 | 2124 | 1314 | 109 | 109 |
| S4 | 2128.5 | 3861 | 109 | 109 |

Note: "Origin" as labeled in the Metallization Mask layout is the centroid of the pad labeled "IN1".

## 7. Revision History

| Date | Revision | Change |
| :---: | :---: | :--- |
| Jul 7, 2021 | 3.0 | Removed Related Literature section. <br> Updated Ordering information table format, added Rad hard information, and updated notes. <br> On page 11 in table 2, Die Characteristics in the Dimensions row change from (106mils x 205mils) <br> to (110.83mils x 209.65mils). |
| Jul 18, 2019 | 2.0 | Updated single event effects information on page 1. <br> Updated links. <br> Removed About Intersil section. <br> Applied new template. |
| Mar 17, 2017 | 1.0 | Changed the title from "CMOS" to "BiCMOS" <br> Added "Related Literature" section <br> Added Note 5. |
| Jul 15, 2016 | 0.0 | Initial release |

## 8. Package Outline Drawing

For the most recent package outline drawing, see K14.A.


## NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions $b$ and $c$ or $M$ shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension $Q$ shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension $Q$ minimum shall be reduced by 0.0015 inch $(0.038 \mathrm{~mm})$ maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M-1982.
10. Controlling dimension: INCH.

K14.A MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B) 14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

| SYMBOL | INCHES |  | MILLIMETERS |  | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |  |
| A | 0.045 | 0.115 | 1.14 | 2.92 | - |
| b | 0.015 | 0.022 | 0.38 | 0.56 | - |
| b1 | 0.015 | 0.019 | 0.38 | 0.48 | - |
| c | 0.004 | 0.009 | 0.10 | 0.23 | - |
| c1 | 0.004 | 0.006 | 0.10 | 0.15 | - |
| D | - | 0.390 | - | 9.91 | 3 |
| E | 0.235 | 0.260 | 5.97 | 6.60 | - |
| E1 | - | 0.290 | - | 7.11 | 3 |
| E2 | 0.125 | - | 3.18 | - | - |
| E3 | 0.030 | - | 0.76 | - | 7 |
| e |  | BSC |  | SC | - |
| k | 0.008 | 0.015 | 0.20 | 0.38 | 2 |
| L | 0.270 | 0.370 | 6.86 | 9.40 | - |
| Q | 0.026 | 0.045 | 0.66 | 1.14 | 8 |
| S1 | 0.005 | - | 0.13 | - | 6 |
| M | - | 0.0015 | - | 0.04 | - |
| N | 14 |  | 14 |  | - |

# IMPORTANT NOTICE AND DISCLAIMER 

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

## Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

## Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

