

# HS-302AEH

## Radiation Hardened BiCMOS Dual DPST Analog Switch

The [HS-302AEH](#) is a dual Double-Pole, Single-Throw (DPST) analog switch fabricated using the Renesas dielectrically isolated Radiation Hardened Silicon Gate (RSG) process technology to ensure latch-up free operation. The HS-302AEH is pin compatible and functionally equivalent to the HS-302RH.

The HS-302AEH offers convenient switching controlled by 5V digital inputs and low-resistance switching performance for analog voltages up to the supply rails. ON-resistance is low and stays reasonably constant across the full range of operating voltage and current and as over exposure to radiation.

The HS-302AEH is available in a 14 Ld CDFP or die form and operates across the extended temperature range of -55°C to +125°C.

### Related Literature

For a full list of related documents, visit our website

- [HS-302AEH](#) device page

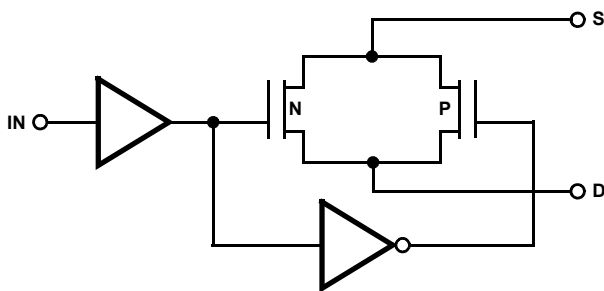


Figure 1. Logic Circuit

Table 1. Truth Table

Logic	All Switches
0	OFF
1	ON

### Features

- Electrically screened to DLA SMD# [5962-95812](#)
- No latch-up, dielectrically isolated device islands
- Pin and functionally compatible with Renesas HS-302RH series analog switches
- Analog signal range equal to the supply voltage range
- Low leakage: 150nA (maximum, post-rad)
- Low  $r_{ON}$ : 60Ω (maximum, post-rad)
- Low standby supply current: ±150μA (maximum, post-rad)
- Radiation assurance
  - High dose rate (50 to 300rad(Si)/s): 100krad(Si)
  - Low dose rate (0.01rad(Si)/s): 50krad(Si) ([Note 1](#))
- Single event effects
  - SEE for LET = 60MeV·cm<sup>2</sup>/mg at 60° incident angle, <150pC charge transferred to the output of an off switch (based on SOI design calculations)

Note:

1. Product capability established by initial characterization. The EH version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate.

### Applications

- Signal processing applications
- Power supply control

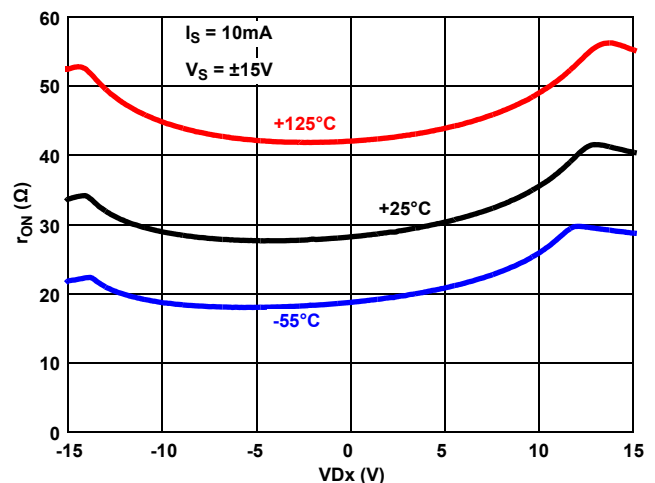
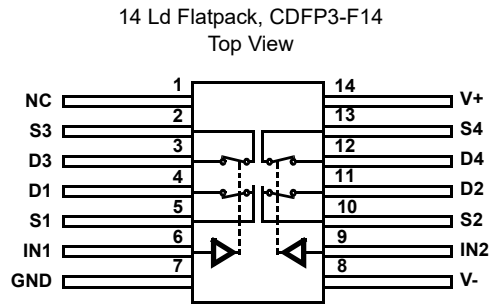


Figure 2.  $r_{ON}$  vs Signal Level vs Temperature

# 1. Overview

## 1.1 Pin Configuration



## 1.2 Pin Descriptions

Pin Number	Pin Name	Pin Description
1	NC	Not electrically connected
2	S3	Analog switch: source connection
5	S1	
10	S2	
13	S4	
3	D3	Analog switch: drain connection
4	D1	
11	D2	
12	D4	
6	IN1	Digital control input for SW1 and SW3
7	GND	Ground
8	V-	Negative power supply
9	IN2	Digital control input for SW2 and SW4
14	V+	Positive power supply
N/A	LID	Electrically floating

### 1.3 Ordering Information

Ordering SMD Number ( <a href="#">Note 3</a> )	Part Number ( <a href="#">Note 2</a> )	Temp. Range (°C)	Package (RoHS Compliant)	Pkg. Dwg. #
5962R9581205VXC	HS9-302AEH-Q	-55 to +125	14 Ld Flatpack	K14.A
5962R9581205V9A	HS0-302AEH-Q	-55 to +125	Die	N/A
N/A	HS9-302AEH/PROTO ( <a href="#">Note 4</a> )	-55 to +125	14 Ld Flatpack	K14.A
N/A	HS0-302AEH/SAMPLE ( <a href="#">Note 4</a> )	-55 to +125	Die	N/A

## Notes:

- These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
- Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
- The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening across the temperature range to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because there is no radiation assurance testing and they are not DLA qualified devices.

## 2. Specifications

### 2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Voltage Between V+ and V- Terminals		35	V
$\pm V_{\text{SUPPLY}}$ to Ground (V+, V-)		$\pm 17.5$	V
<b>Analog Input Voltage</b>			
(+V <sub>S</sub> )		+V <sub>SUPPLY</sub> + 1.5	V
(-V <sub>S</sub> )		-V <sub>SUPPLY</sub> - 1.5	V
<b>Digital Input Voltage</b>			
(+V <sub>A</sub> )		+V <sub>SUPPLY</sub> + 4	V
(-V <sub>A</sub> )		-V <sub>SUPPLY</sub> - 4	V
Peak Current (S or D), (Pulse at 1ms, 10% Duty Cycle Max)		40	mA
Continuous Current		10	mA
<b>ESD Rating</b>		<b>Value</b>	<b>Unit</b>
Human Body Model (Tested per MIL-PRF-883 TM 3015.7)		2	kV
Machine Model (Tested per EIA/JESD22-A115-A)		200	V
Charged Device Model (Tested per JESD22-C101D)		1	kV

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

### 2.2 Thermal Information

Thermal Resistance (Typical)	$\theta_{\text{JA}}$ (°C/W)	$\theta_{\text{JC}}$ (°C/W)
Flatpack Package (Notes 5, 6)	105	17

Notes:

- $\theta_{\text{JA}}$  is measured in free air with the component mounted on a low-effective thermal conductivity test board in free air. See [TB379](#).
- For  $\theta_{\text{JC}}$ , the "case temp" location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Package Power Dissipation at 125°C, Flatpack Package		0.48	W
Junction Temperature (T <sub>J</sub> )		+175	°C
Storage Temperature Range	-65	+150	°C

### 2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Operating Temperature Range	-55	+125	°C
Operating Supply Voltage Range ( $\pm V_{\text{SUPPLY}}$ )		$\pm 15$	V
Analog Input Voltage (V <sub>S</sub> )		$\pm V_{\text{SUPPLY}}$	V
Logic Low Level (V <sub>AL</sub> )	0	0.8	V
Logic High Level (V <sub>AH</sub> )	4.0	+V <sub>SUPPLY</sub>	V

## 2.4 Electrical Specifications

$V_{SUPPLY} = \pm 15V$  unless otherwise specified. **Boldface limits either apply across the operating temperature range -55°C to +125°C or across a total ionizing dose of 100krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s and a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Switch On-Resistance	$+r_{DS(ON)}$	$V_D = 10V, I_S = -10mA, T_A = +25^\circ C$	-	-	50	$\Omega$
		$T_A = -55^\circ C$ to $+125^\circ C$	-	35	<b>75</b>	$\Omega$
		$T_A = 25^\circ C$ , post radiation	-	-	<b>60</b>	$\Omega$
Switch On-Resistance	$-r_{DS(ON)}$	$V_D = -10V, I_S = 10mA, T_A = +25^\circ C$	-	-	50	$\Omega$
		$T_A = -55^\circ C$ to $+125^\circ C$	-	35	<b>75</b>	$\Omega$
		$T_A = 25^\circ C$ , post radiation	-	-	<b>60</b>	$\Omega$
Leakage Current into Source Terminal of an OFF Switch	$+I_{S(OFF)}$	$V_S = +14V, V_D = -14V, T_A = +25^\circ C$	-100	-	100	nA
		$V_S = +14V, V_D = -14V, T_A = -55^\circ C$ to $+125^\circ C$	<b>-150</b>	0.05	<b>150</b>	nA
		$V_S = +14V, V_D = -14V, T_A = +25^\circ C$ , post radiation	<b>-150</b>	-	<b>150</b>	nA
		$V_S = +15V, V_D = -15V, T_A = +25^\circ C$	-1	-	1	$\mu A$
		$V_S = +15V, V_D = -15V, T_A = -55^\circ C$ to $+125^\circ C$	<b>-20</b>	-	<b>20</b>	$\mu A$
		$V_S = +15V, V_D = -15V, T_A = +25^\circ C$ , post radiation	<b>-20</b>	-	<b>20</b>	$\mu A$
Leakage Current into Source Terminal of an OFF Switch	$-I_{S(OFF)}$	$V_S = -14V, V_D = +14V, T_A = +25^\circ C$	-100	-	100	nA
		$V_S = -14V, V_D = +14V, T_A = -55^\circ C$ to $+125^\circ C$	<b>-150</b>	0.05	<b>150</b>	nA
		$V_S = -14V, V_D = +14V, T_A = +25^\circ C$ , post radiation	<b>-150</b>	-	<b>150</b>	nA
		$V_S = -15V, V_D = +15V, T_A = +25^\circ C$	-1	-	1	$\mu A$
		$V_S = -15V, V_D = +15V, T_A = -55^\circ C$ to $+125^\circ C$	<b>-20</b>	-	<b>20</b>	$\mu A$
		$V_S = -15V, V_D = +15V, T_A = +25^\circ C$ , post radiation	<b>-20</b>	-	<b>20</b>	$\mu A$
Leakage Current into Drain Terminal of an OFF Switch	$+I_{D(OFF)}$	$V_S = +14V, V_D = -14V, T_A = +25^\circ C$	-100	-	100	nA
		$V_S = +14V, V_D = -14V, T_A = -55^\circ C$ to $+125^\circ C$	<b>-150</b>	0.05	<b>150</b>	nA
		$V_S = +14V, V_D = -14V, T_A = +25^\circ C$ , post radiation	<b>-150</b>	-	<b>150</b>	nA
		$V_S = +15V, V_D = -15V, T_A = +25^\circ C$	-1	-	1	$\mu A$
		$V_S = +15V, V_D = -15V, T_A = -55^\circ C$ to $+125^\circ C$	<b>-20</b>	-	<b>20</b>	$\mu A$
		$V_S = +15V, V_D = -15V, T_A = +25^\circ C$ , post radiation	<b>-20</b>	-	<b>20</b>	$\mu A$
Leakage Current into Drain Terminal of an OFF Switch	$-I_{D(OFF)}$	$V_S = -14V, V_D = +14V, T_A = +25^\circ C$	-100	-	100	nA
		$V_S = -14V, V_D = +14V, T_A = -55^\circ C$ to $+125^\circ C$	<b>-150</b>	0.5	<b>150</b>	nA
		$V_S = -14V, V_D = +14V, T_A = +25^\circ C$ , post radiation	<b>-150</b>	-	<b>150</b>	nA
		$V_S = -15V, V_D = +15V, T_A = +25^\circ C$	-1	-	1	$\mu A$
		$V_S = -15V, V_D = +15V, T_A = -55^\circ C$ to $+125^\circ C$	<b>-20</b>	-	<b>20</b>	$\mu A$
		$V_S = -15V, V_D = +15V, T_A = +25^\circ C$ , post radiation	<b>-20</b>	-	<b>20</b>	$\mu A$
Leakage Current from an ON Driver into the Switch (Drain and Source)	$+I_{D(ON)}$	$V_S = +14V, V_D = +14V, T_A = +25^\circ C$	-20	-	20	nA
		$V_S = +14V, V_D = +14V, T_A = -55^\circ C$ to $+125^\circ C$	<b>-100</b>	-0.1	<b>100</b>	nA
		$V_S = +14V, V_D = +14V, T_A = +25^\circ C$ , post radiation	<b>-100</b>	-	<b>100</b>	nA
Leakage Current from an ON Driver into the Switch (Drain and Source)	$-I_{D(ON)}$	$V_S = -14V, V_D = -14V, T_A = +25^\circ C$	-20	-	20	nA
		$V_S = -14V, V_D = -14V, T_A = -55^\circ C$ to $+125^\circ C$	<b>-100</b>	-0.1	<b>100</b>	nA
		$V_S = -14V, V_D = -14V, T_A = +25^\circ C$ , post radiation	<b>-100</b>	-	<b>100</b>	nA

$V_{SUPPLY} = \pm 15V$  unless otherwise specified. **Boldface limits either apply across the operating temperature range -55°C to +125°C or across a total ionizing dose of 100krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s and a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrads(Si)/s. (Continued)**

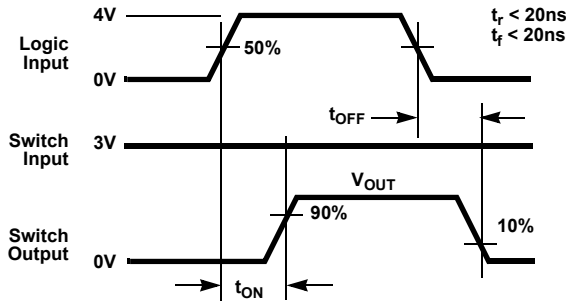
Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Low Level Input Address Current	$I_{AL}$	All Channels $V_A = 0.8V$ , $T_A = -55^\circ C$ to $+125^\circ C$	-1	-	<b>1</b>	$\mu A$
		All Channels $V_A = 0.8V$ , $T_A = +25^\circ C$ , post radiation	-1	-	<b>1</b>	$\mu A$
High Level Input Address Current	$I_{AH}$	All Channels $V_A = 4.0V$ , $T_A = -55^\circ C$ to $+125^\circ C$	-1	-	<b>1</b>	$\mu A$
		All Channels $V_A = 4.0V$ , $T_A = +25^\circ C$ , post radiation	-1	-	<b>1</b>	$\mu A$
Positive Supply Current	I+	All Channels $V_A = 0.8V$ , $T_A = +25^\circ C$	-	-	100	$\mu A$
		All Channels $V_A = 0.8V$ , $T_A = -55^\circ C$ to $+125^\circ C$	-	45	<b>150</b>	$\mu A$
		All Channels $V_A = 0.8V$ , $T_A = +25^\circ C$ , post radiation	-	-	<b>150</b>	$\mu A$
		$V_{A1} = 0V$ , $V_{A2} = 4V$ , $V_{A1} = 4V$ , $V_{A2} = 0V$ , $T_A = +25^\circ C$	-	-	0.4	mA
		$V_{A1} = 0V$ , $V_{A2} = 4V$ , $V_{A1} = 4V$ , $V_{A2} = 0V$ , $T_A = -55^\circ C$ to $+125^\circ C$	-	0.15	<b>0.6</b>	mA
		$V_{A1} = 0V$ , $V_{A2} = 4V$ , $V_{A1} = 4V$ , $V_{A2} = 0V$ , $T_A = +25^\circ C$ , post radiation	-	-	<b>0.6</b>	mA
Negative Supply Current	I-	All Channels $V_A = 0.8V$ , $T_A = +25^\circ C$	-	-	-10	$\mu A$
		All Channels $V_A = 0.8V$ , $T_A = -55^\circ C$ to $+125^\circ C$	-	-0.1	<b>-100</b>	$\mu A$
		All Channels $V_A = 0.8V$ , $T_A = +25^\circ C$ , post radiation	-	-	<b>-100</b>	$\mu A$
		$V_{A1} = 0V$ , $V_{A2} = 4V$ , $V_{A1} = 4V$ , $V_{A2} = 0V$ , $T_A = +25^\circ C$	-	-	-10	$\mu A$
		$V_{A1} = 0V$ , $V_{A2} = 4V$ , $V_{A1} = 4V$ , $V_{A2} = 0V$ , $T_A = -55^\circ C$ to $+125^\circ C$	-	-0.1	<b>-100</b>	$\mu A$
		$V_{A1} = 0V$ , $V_{A2} = 4V$ , $V_{A1} = 4V$ , $V_{A2} = 0V$ , $T_A = +25^\circ C$ , post radiation	-	-	<b>-100</b>	$\mu A$
Switch Input Capacitance	$C_{IS(OFF)}$	From Source to GND (Note 8)	-	-	28	pF
Driver Input Capacitance	$C_{C1}$	$V_A = 0V$ (Note 8)	-	-	10	pF
Driver Input Capacitance	$C_{C2}$	$V_A = 15V$ (Note 8)	-	-	10	pF
Switch Output	$C_{OS}$	Measured Drain to GND (Note 8)	-	-	32	pF
Off Isolation	$V_{ISO}$	$V_{GEN} = 1V_{P-P}$ , $f = 1MHz$ (Note 8)	40	-	-	dB
Cross Talk	$V_{CR}$	$V_{GEN} = 1V_{P-P}$ , $f = 1MHz$ (Note 8)	40	-	-	dB
Charge Transfer Error	$V_{CTE}$	$V_S = GND$ , $C_L = 0.01\mu F$ (Note 8)	-	-	15	mV
Switch Turn-On Time	$t_{ON}$	$R_L = 300\Omega$ , $V_S = 3V$ , $V_{AH} = 4V$ , $V_{AL} = 0V$ , $T_A = +25^\circ C$	-	-	375	ns
		$T_A = -55^\circ C$ to $+125^\circ C$	-	250	<b>500</b>	ns
		$T_A = +25^\circ C$ , post radiation	-	-	<b>1</b>	$\mu s$
Switch Turn-Off Time	$t_{OFF}$	$R_L = 300\Omega$ , $V_S = 3V$ , $V_{AH} = 4V$ , $V_{AL} = 0V$	-	-	300	ns
		$T_A = -55^\circ C$ to $+125^\circ C$	-	200	<b>450</b>	ns
		$T_A = +25^\circ C$ , post radiation	-	-	<b>1</b>	$\mu s$

## Notes:

- Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
- $V_{AL} = 0V$  and  $V_{AH} = 4V$ .

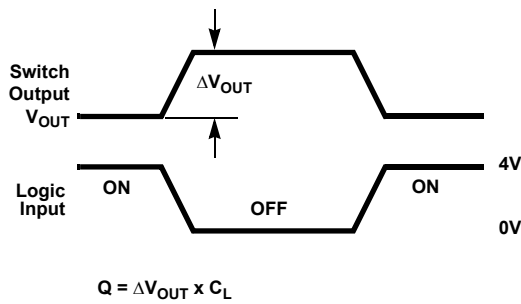
### 3. Test Circuits and Waveforms

#### 3.1 Switching Times



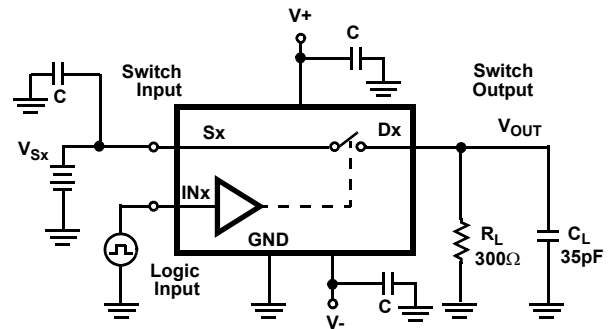
Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 3. Switching Times Measurement Points



Logic input waveform is inverted for switches that have the opposite logic sense.

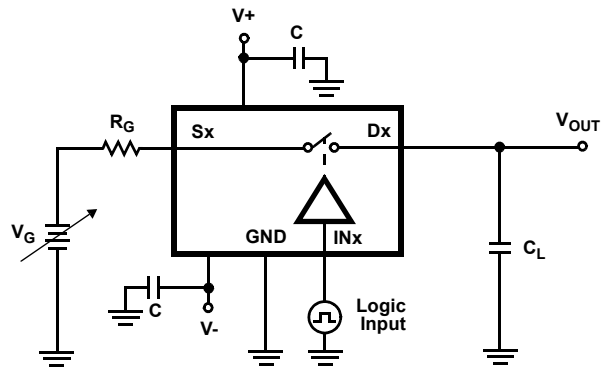
Figure 5. Charge Transfer Error Measurement Points



Repeat test for all switches.  $C_L$  includes fixture and stray capacitance.

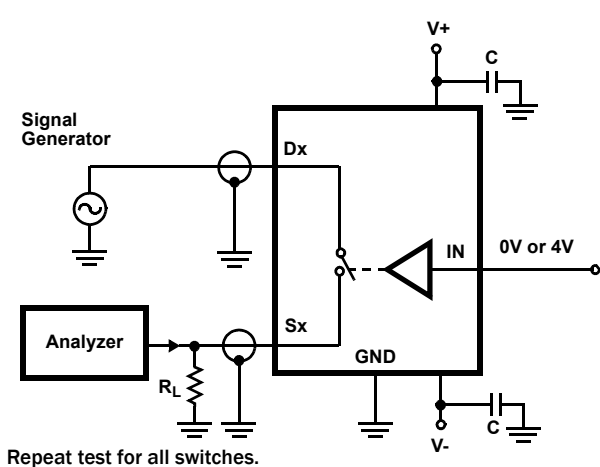
$$V_{OUT} = V_{(NO \text{ or } NC)} \frac{R_L}{R_L + r_{ON}}$$

Figure 4. Switching Times Test Circuit



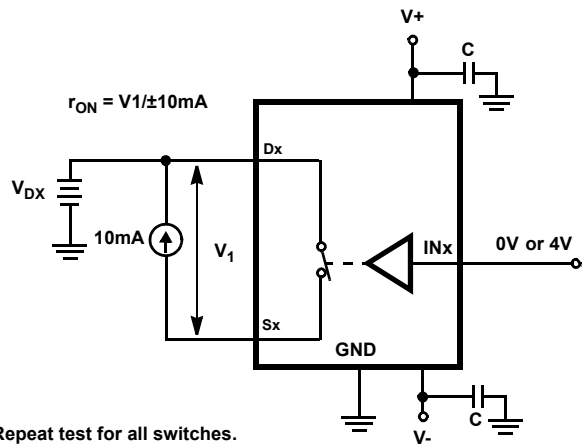
Repeat test for all switches.  $C_L$  includes fixture and stray capacitance.

Figure 6. Charge Transfer Error Test Circuit



Repeat test for all switches.

Figure 7. Off Isolation Test Circuit



Repeat test for all switches.

Figure 8.  $r_{ON}$  Test Circuit

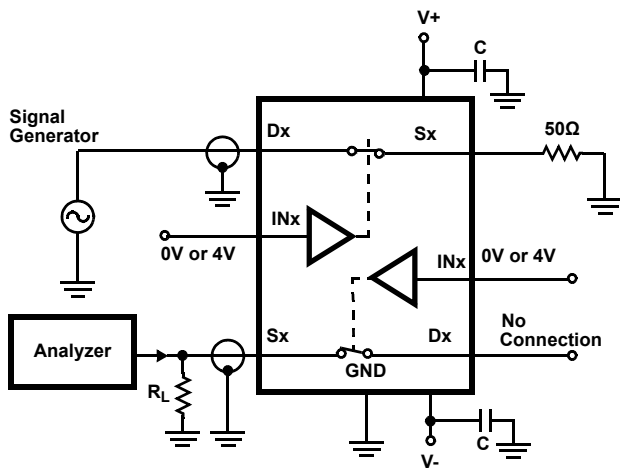


Figure 9. Crosstalk Test Circuit

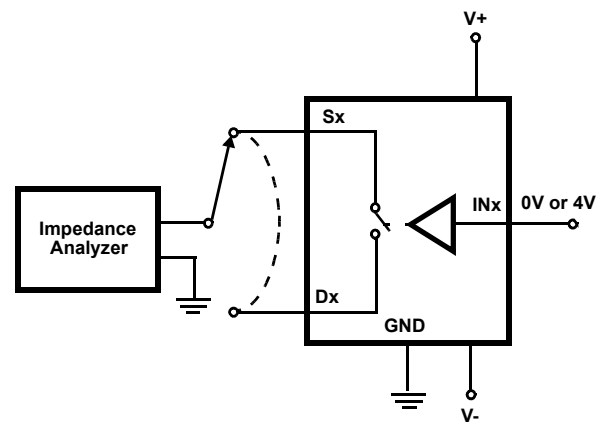


Figure 10. Capacitance Test Circuit



### 4. Typical Performance Curves

$V_S = \pm 15V$ ,  $V_{CM} = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ C$ , unless otherwise specified.

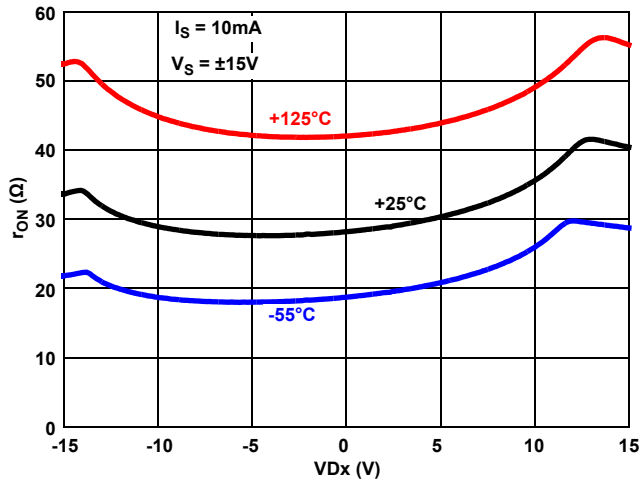


Figure 11.  $r_{ON}$  vs Signal Level vs Temperature

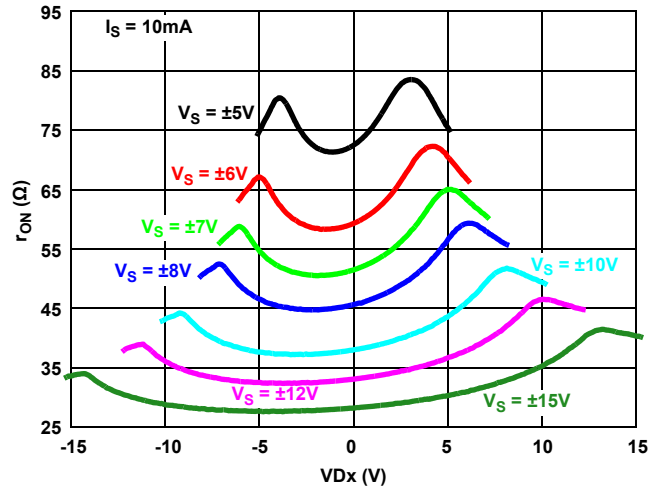


Figure 12.  $r_{ON}$  vs Signal Level vs Supply Voltages

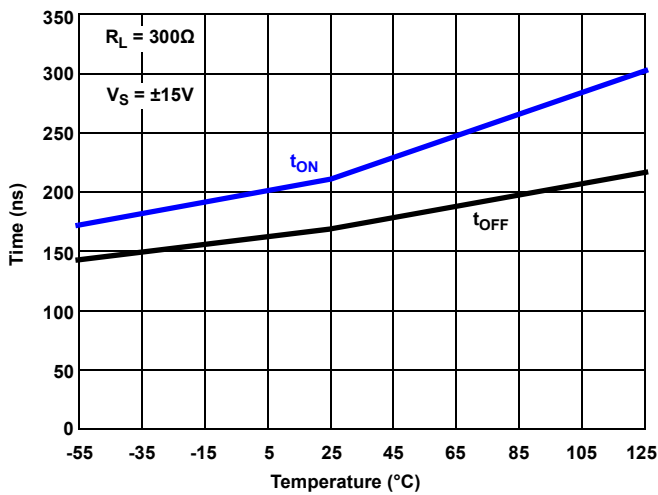


Figure 13.  $t_{ON}$  and  $t_{OFF}$  vs Temperature

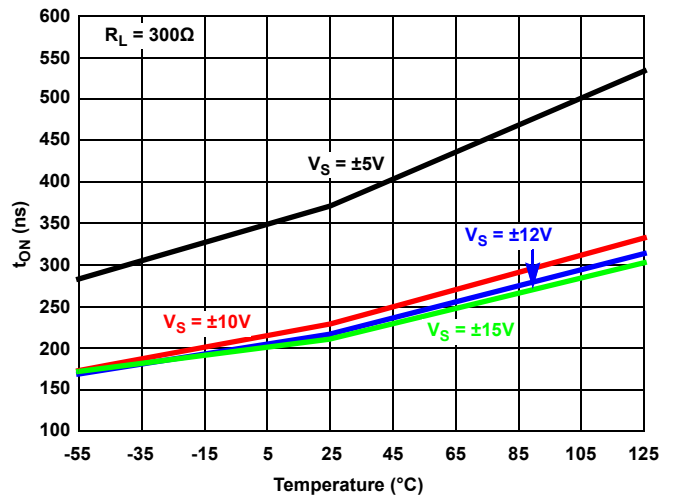


Figure 14.  $t_{ON}$  vs Temperature vs Supply Voltages

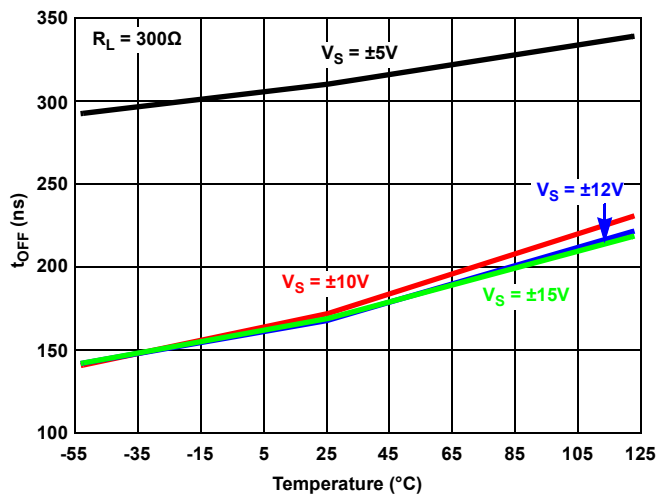


Figure 15.  $t_{OFF}$  vs Temperature vs Supply Voltages

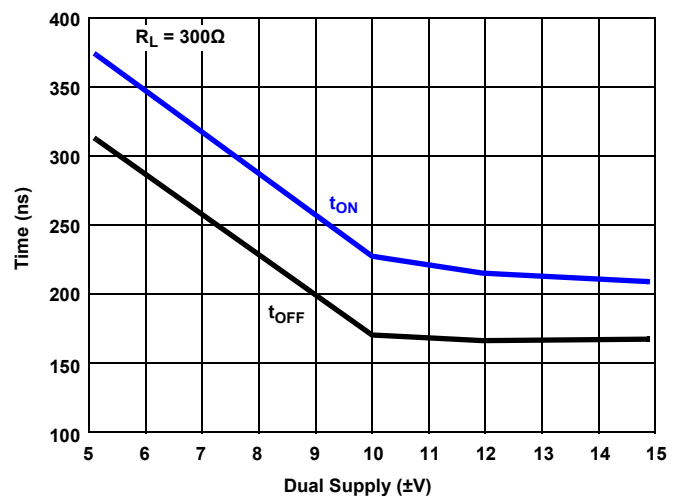


Figure 16.  $t_{ON}$  and  $t_{OFF}$  vs Temperature

$V_S = \pm 15V$ ,  $V_{CM} = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ C$ , unless otherwise specified. (Continued)

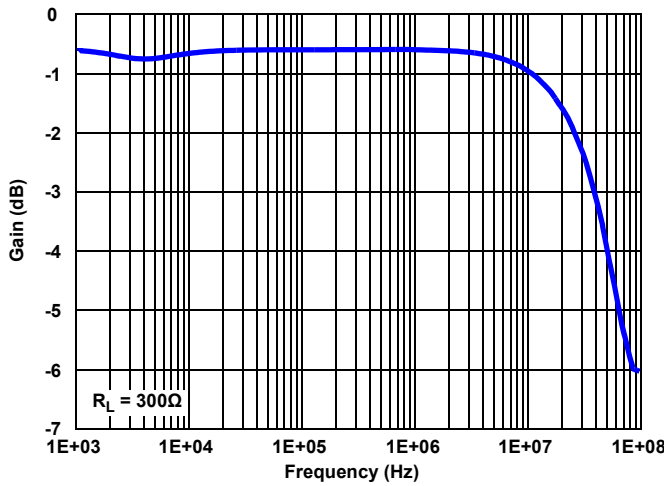


Figure 17. Frequency Response vs Frequency

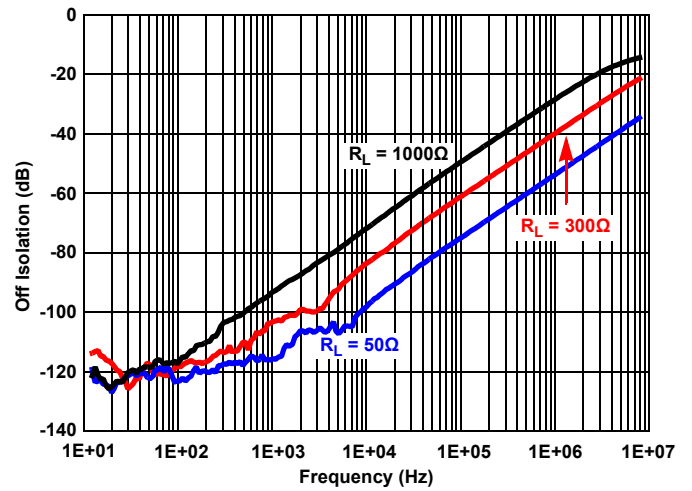


Figure 18. Off Isolation vs Frequency

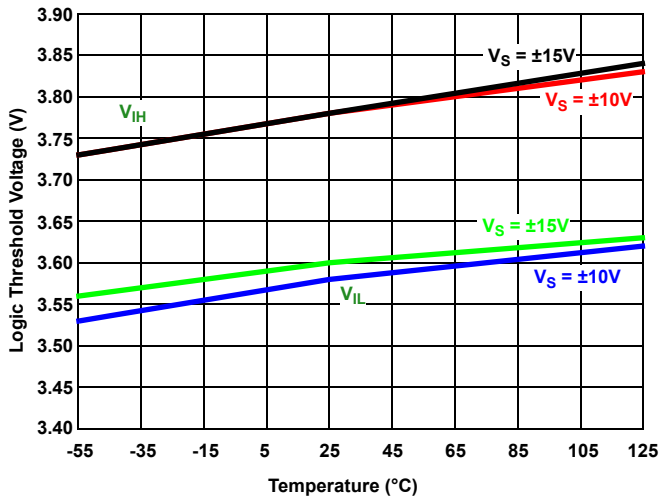


Figure 19.  $V_{IH} / V_{IL}$  vs Temperature vs Supply Voltages

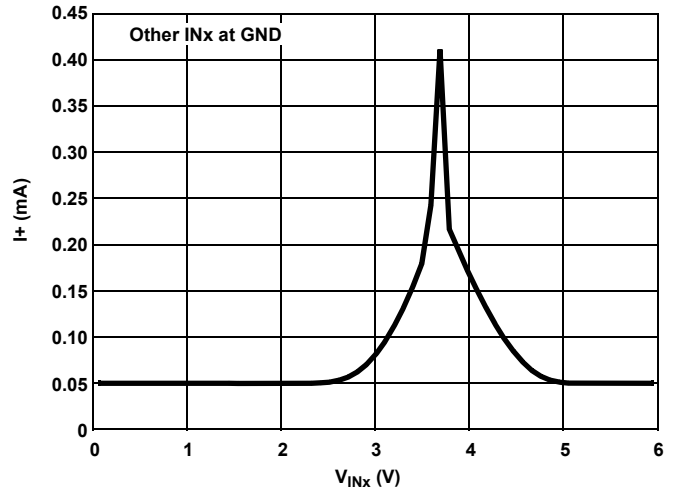


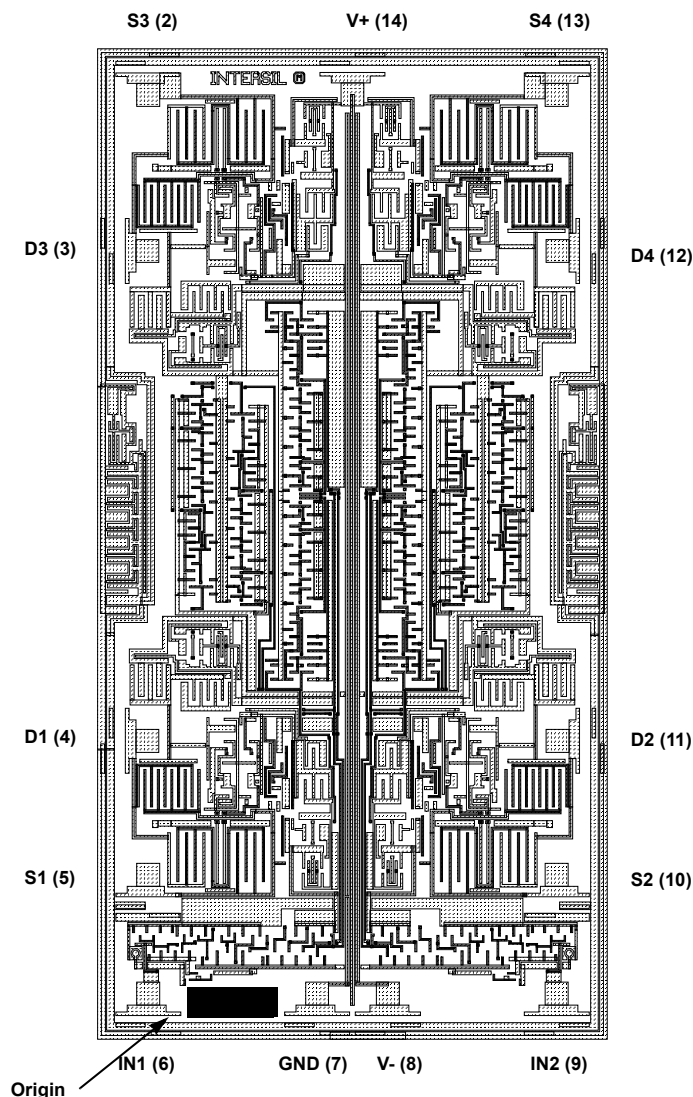
Figure 20.  $I_+$  vs Logic In

## 5. Die Characteristics

**Table 2. Die and Assembly Related Information**

<b>Die Information</b>	
Dimensions	2815 $\mu$ m x 5325 $\mu$ m (106 mils x 205 mils) Thickness: 483 $\mu$ m $\pm$ 25.4 $\mu$ m (19 mils $\pm$ 1 mil)
<b>Interface Materials</b>	
Glassivation	Type: PSG (Phosphorous Silicon Glass) Thickness: 8.0k $\text{\AA}$ $\pm$ 1.0k $\text{\AA}$
Top Metallization	Type: AlSiCu Thickness: 16.0k $\text{\AA}$ $\pm$ 2k $\text{\AA}$
Backside Finish	Silicon
Substrate	Radiation Hardened Silicon Gate, Dielectric Isolation
<b>Assembly Information</b>	
Substrate Potential	Unbiased (DI)
<b>Additional Information</b>	
Worst Case Current Density	<2.0 x 10 <sup>5</sup> A/cm <sup>2</sup>
Transistor Count	348
Package Lid Potential	Floating

## 6. Metallization Mask Layout



### 6.1 Layout Characteristics

Step and Repeat: 2815 $\mu$ m x 5325 $\mu$ m

Table 3. Layout X-Y Coordinates

Pad Name	X ( $\mu$ m)	Y ( $\mu$ m)	DX ( $\mu$ m)	DY ( $\mu$ m)
S3	0	4672.5	109	109
D3	-4.5	3861	109	109
D1	-4.5	1314	109	109
S1	0	617.5	109	109
IN1	0	0	109	109
GND	878	0	109	109
V-	1246	0	109	109
IN2	2124	0	109	109
S2	2124	617.5	109	109
D2	2128.5	1314	109	109

**Table 3. Layout X-Y Coordinates (Continued)**

Pad Name	X ( $\mu\text{m}$ )	Y ( $\mu\text{m}$ )	DX ( $\mu\text{m}$ )	DY ( $\mu\text{m}$ )
D4	2128.5	3861	109	109
S4	2124	4672	109	109
V+	1062	4675	109	109

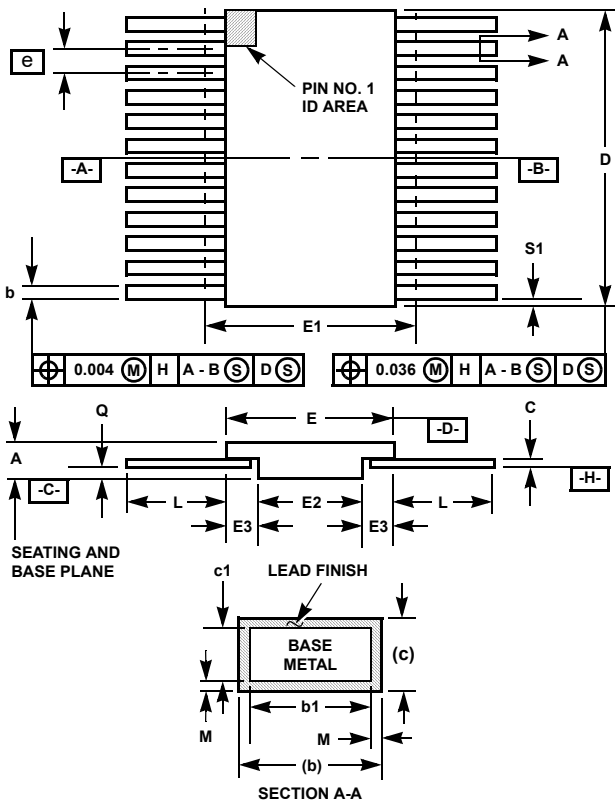
Note: "Origin" as labeled in the Metallization Mask layout is the centroid of the pad labeled "IN1".

## 7. Revision History

Date	Revision	Change
Jul.18.19	FN8815.2	Updated single event effects information on page 1. Updated links. Removed About Intersil section. Applied new template.
Mar.17.17	FN8815.1	Changed the title from "CMOS" to "BiCMOS" Added "Related Literature" section Added <a href="#">Note 4</a> .
Jul.15.16	FN8815.0	Initial release

### 8. Package Outline Drawing

For the most recent package outline drawing, see [K14.A](#).



**K14.A MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B)  
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

Rev. 0 5/18/94

**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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