# HS-26CT32RH, HS-26CT32EH

Radiation Hardened Quad Differential Line Receivers

FN2930
Rev 6.00
May 23, 2013

The Intersil HS-26CT32RH, HS-26CT32EH are differential line receivers designed for digital data transmission over balanced lines and meets the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CT32RH, HS-26CT32EH have an input sensitivity typically of 200mV over the common mode input voltage range of ±7V. The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic "1" when the inputs are open. Enable and Disable functions are common to all four receivers.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" must be used when ordering.

**Detailed Electrical Specifications for these devices are contained in SMD 5962-95631. A "hot-link" is also provided on our homepage for downloading.**

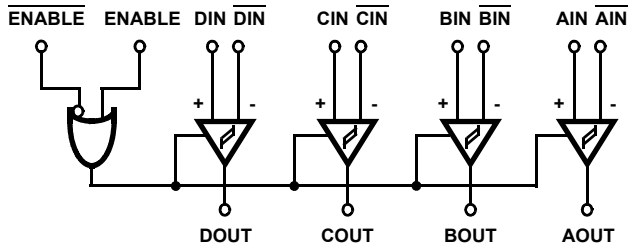
## Features

- Electrically screened to SMD # 5962-95631
- QML qualified per MIL-PRF-38535 requirements
- 1.2 Micron radiation hardened CMOS
  - Total dose . . . . . Up to 300kRAD(Si)
- Latch-up free
- EIA RS-422 compatible outputs
- Operation with TTL based on $V_{IH} = V_{DD}/2$
- Input fail safe circuitry
- High impedance inputs when disabled or powered down
- Low power dissipation standby (Max) . . . . . 138mW
- Single 5V supply
- Full Military temperature range . . . . . -55°C to +125°C

## Applications

- Line receiver for MIL-STD-1553 serial data bus
- Line receiver for RS422

## Logic Diagram




## Ordering Information

| ORDERING NUMBER (Note 1) | INTERNAL MKT. NUMBER | PART MARKING | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|---|---|
| 5962F9563101QEC | HS1-26CT32RH-8 | Q 5962F95 63101QEC | -55 to +125 | 16 Ld SBDIP | D16.3 |
| 5962F9563101QXC | HS9-26CT32RH-8 | Q 5962F95 63101QXC | -55 to +125 | 16 Ld Flatpack | K16.A |
| 5962F9563101V9A | HS0-26CT32RH-Q | | -55 to +125 | Die | |
| HS0-26CT32RH/SAMPLE | HS0-26CT32RH/SAMPLE | | -55 to +125 | Die | |
| 5962F9563101VEC | HS1-26CT32RH-Q | Q 5962F95 63101VEC | -55 to +125 | 16 Ld SBDIP | D16.3 |
| 5962F9563101VXC | HS9-26CT32RH-Q | Q 5962F95 63101VXC | -55 to +125 | 16 Ld Flatpack | K16.A |
| 5962F9563102VXC | HS9-26CT32EH-Q | Q 5962F95 63102VXC | -55 to +125 | 16 Ld Flatpack | K16.A |
| HS1-26CT32RH/PROTO | HS1-26CT32RH/PROTO | HS1- 26CT32RH /PROTO | -55 to +125 | 16 Ld SBDIP | D16.3 |
| HS9-26CT32RH/PROTO | HS9-26CT32RH/PROTO | HS9- 26CT32RH /PROTO | -55 to +125 | 16 Ld Flatpack | K16.A |
| 5962F9563102VEC | HS1-26CT32EH-Q | Q 5962F95 63102VEC | -55 to +125 | 16 Ld SBDIP | D16.3 |

## Ordering Information (Continued)

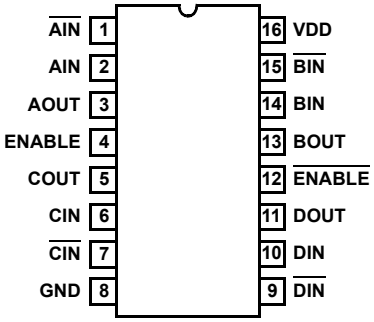
| ORDERING NUMBER (Note 1) | INTERNAL MKT. NUMBER | PART MARKING | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|---|---|
| 5962F9563102VXC | HS9-26CT32EH-Q | Q 5962F95 63102VXC | -55 to +125 | 16 Ld Flatpack | K16.A |
| 5962F9563102V9A | HS0-26CT32EH-Q | | -55 to +125 | Die | |
| 5962F9563101VYC | HS9G-26CT32RH-Q (Note2) | Q 5962F95 63101VYC | -55 to +125 | 16 Ld Flatpack | K16.A |
| HS9G-26CT32RH/PROTO | HS9G-26CT32RH/PROTO (Note 2) | HS9G-26CT32RH/PROTO | -55 to +125 | 16 Ld Flatpack | K16.A |

NOTES:

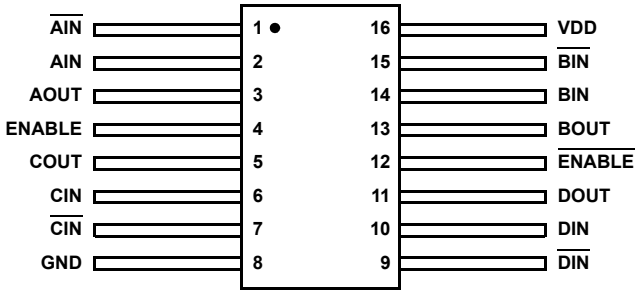
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. The lid of these packages are connected to the ground pin of the device.

## Pin Configurations

HS1-26CT32RH
(16 LD SBDIP, CDIP2-T16)
TOP VIEW




HS9-26CT32RH, HS9-26CT32EH
(16 LD FLATPACK, CDFP4-F16)
TOP VIEW



# Die Characteristics

**DIE DIMENSIONS:**

78 mils x 123 mils
(1970µm x 3120µm)

**INTERFACE MATERIALS:**

**Glassivation:**

Type: PSG (Phosphorus Silicon Glass)
Thickness: 10kÅ ±1kÅ

**Top Metallization:**

M1: Mo/Tiw
Thickness: 5800Å
M2: Al/Si/Cu
Thickness: 10kÅ ±1kÅ

**Substrate:**

AVLSI1RA

**Backside Finish:**

Silicon

**ASSEMBLY RELATED INFORMATION:**

**Substrate Potential:**

$V_{DD}$ (When Powered Up)

**ADDITIONAL INFORMATION:**

**Worst Case Current Density:**

$<2.0 \times 10^5 A/cm^2$

**Transistor Count:**

240

**Bond Pad Size:**

110µm x 100µm

# Metallization Mask Layout

**HS-26CT32RH, HS-26CT32EH**