intersil

DATASHEET

HS-26CLV32RH, HS-26CLV32EH

Radiation Hardened 3.3V Quad Differential Line Receivers

FN4907
Rev 6.00
February 6, 2017

The Intersil HS-26CLV32RH, HS-26CLV32EH are radiation hardened 3.3V quad differential line receivers designed for digital data transmission over balanced lines, in low voltage, RS-422 protocol applications. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CLV32RH, HS-26CLV32EH have an input sensitivity of 200mV (typical) over a common-mode input voltage range of -4V to +7V. The receivers are also equipped with input fail-safe circuitry, which causes the outputs to go to a logic “1” when the inputs are open. The device has unique inputs that remain high impedance when the receiver is disabled or powered-down, maintaining signal integrity in multi-receiver applications.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.

Related Literature

- For a full list of related documents, visit our website
  - HS-26CLV32RH and HS-26CLV32EH product pages

Features

- Electrically screened to SMD # 5962-95689
- QML qualified per MIL-PRF-38535 requirements
- 1.2 micron radiation hardened CMOS
  - Total dose . . . . 300krad(Si) (max)
  - Single event upset LET . . . . $100MeV/mg/cm^2$)
  - Single event latch-up immune
- Low stand-by current . . . . 13mA (max)
- Operating supply range . . . . 3.0V to 3.6V
- Enable input levels. . . . . $V_{IH} > 0.7 \times V_{DD}$; $V_{IL} < 0.3 \times V_{DD}$
- CMOS output levels . . . . $V_{OH} > 2.55V$; $V_{OL} < 0.4V$
- Input fail-safe circuitry
- High impedance inputs when disabled or powered-down
- Full -55°C to +125°C military temperature range
- Pb-free (RoHS compliant)

Applications

- Line receiver for MIL-STD-1553 serial data bus

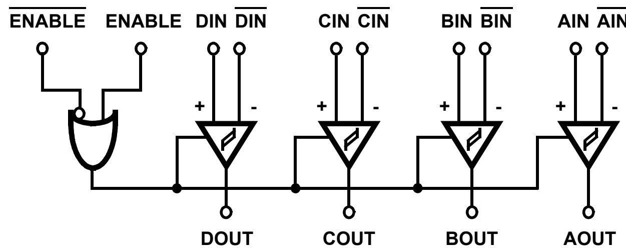


FIGURE 1. LOGIC DIAGRAM

Ordering Information

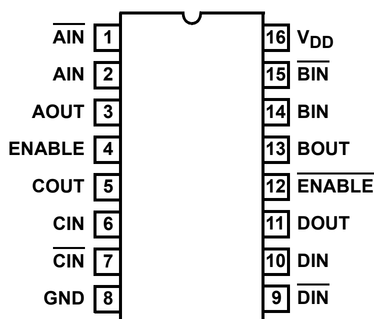
ORDERING SMD NUMBER (Note 2)	PART NUMBER (Note 1)	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
5962F9568902QEC	HS1-26CLV32RH-8	-55 to +125	16 Ld SBDIP	D16.3
5962F9568902QXC	HS9-26CLV32RH-8	-55 to +125	16 Ld Flatpack	K16.A
5962F9568902VEC	HS1-26CLV32RH-Q	-55 to +125	16 Ld SBDIP	D16.3
5962F9568902VXC	HS9-26CLV32RH-Q	-55 to +125	16 Ld Flatpack	K16.A
5962F9568902V9A	HS0-26CLV32RH-Q	-55 to +125	Die	
N/A	HS0-26CLV32RH/SAMPLE	-55 to +125	Die	
N/A	HS1-26CLV32RH/PROTO	-55 to +125	16 Ld SBDIP	D16.3
N/A	HS9-26CLV32RH/PROTO	-55 to +125	16 Ld Flatpack	K16.A
5962F9568904VEC	HS1-26CLV32EH-Q	-55 to +125	16 Ld SBDIP	D16.3
5962F9568904VXC	HS9-26CLV32EH-Q	-55 to +125	16 Ld Flatpack	K16.A
5962F9568904V9A	HS0-26CLV32EH-Q	-55 to +125	Die	
5962F9568904VYC	HS9G-26CLV32EH-Q (Note 3)	-55 to +125	16 Ld Flatpack	K16.A
5962F9568902VYC	HS9G-26CLV32RH-Q (Note 3)	-55 to +125	16 Ld Flatpack	K16.A
N/A	HS9G-26CLV32RH/PROTO (Notes 3)	-55 to +125	16 Ld Flatpack	K16.A

NOTES:

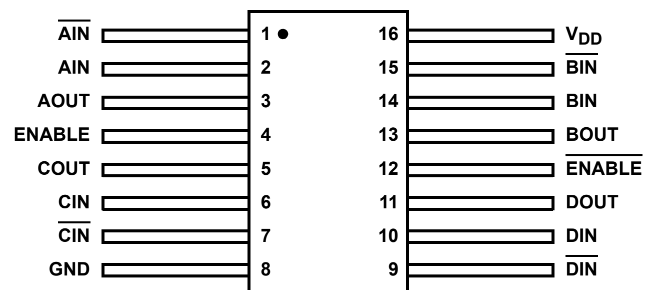
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
3. The lid of these packages are connected to the ground pin of the device.

Pin Configurations

HS1-26CLV32RH, HS1-26CLV32EH
(16 LD SBDIP)
MIL-STD-1835: CDIP2-T16
TOP VIEW



HS9-26CLV32RH, HS9-26CLV32EH
(16 LD FLATPACK)
MIL-STD-1835: CDFP4-F16
TOP VIEW



NOTES:

4. For details on input output structures refer to application note AN9520.
5. For details on package dimensions refer MIL STD 1835.

Die Characteristics

DIE DIMENSIONS:

78 mils x 123 mils x 21 mils
(1970µm x 3120µm)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorus Silicon Glass)
Thickness: 8kÅ ±1kÅ

Substrate:

AVLSI1RA, Silicon backside, V_{DD} backside potential

Metallization:

Bottom: Mo/TiW
Thickness: 5800Å ±1kÅ
Top: Al/Si/Cu
Thickness: 10kÅ ±1kÅ

Worst Case Current Density:

<2.0 x 10^5A/cm^2

Bond Pad Size:

110µmx100µm

Metallization Mask Layout

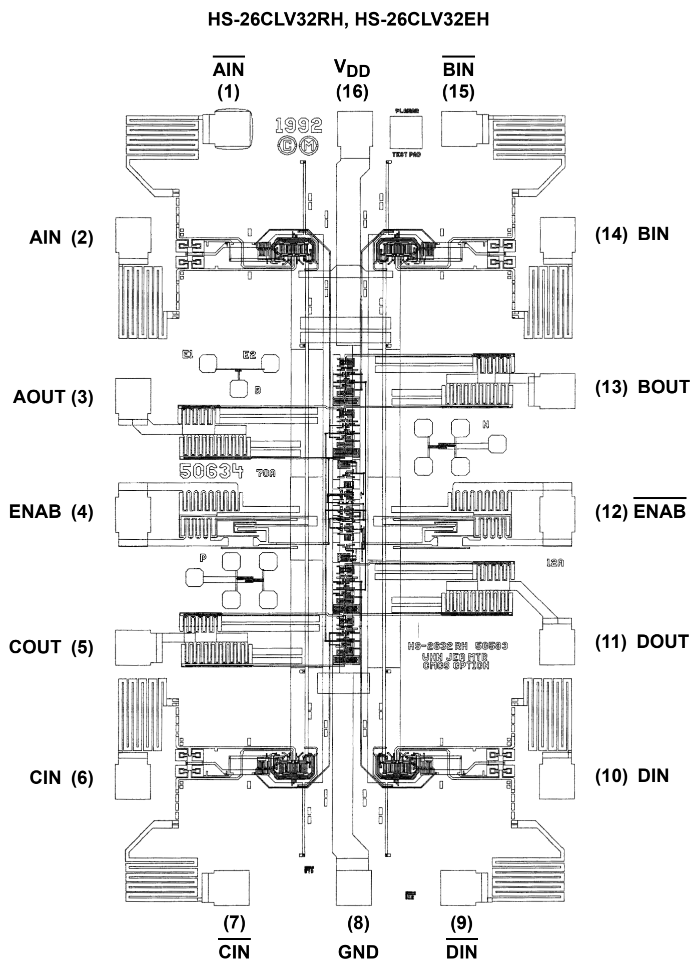


TABLE 1. HS-26CLV32RH, HS-26CLV32EH PAD COORDINATES

PIN NUMBER	PAD NAME	RELATIVE TO PIN 1	
		X COORDINATES	Y COORDINATES
1	AIN	0	0
2	AIN	-337.1	-362
3	AOUT	-337.1	-912.5
4	ENABLE	-337.1	-1319.3
5	COUT	-337.1	-1774.4
6	CIN	-337.1	-2233.7
7	CIN	0	-2595.7
8	GND	418.4	-2596.7
9	DIN	776.4	-2595.7
10	DIN	1113.5	-2233.7
11	DOUT	1113.5	-1774.4
12	ENABLE	1113.5	-1319.3
13	BOUT	1113.5	-898.4
14	BIN	1113.5	-362
15	BIN	776.4	0
16	V_{DD}	420.2	1

NOTE: Dimensions in microns

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
February 6, 2017	FN4907.6	Added Related Literature section. Updated Ordering Information table on page 2. Added Note 2 on page 2. Added Revision History and About Intersil sections. Added POD drawings.

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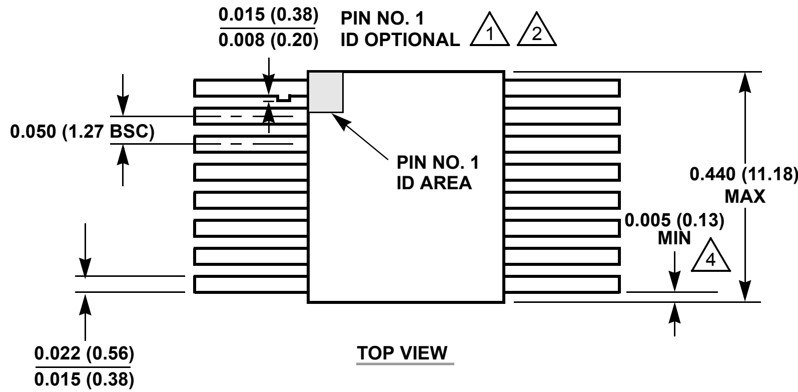
Package Outline Drawing

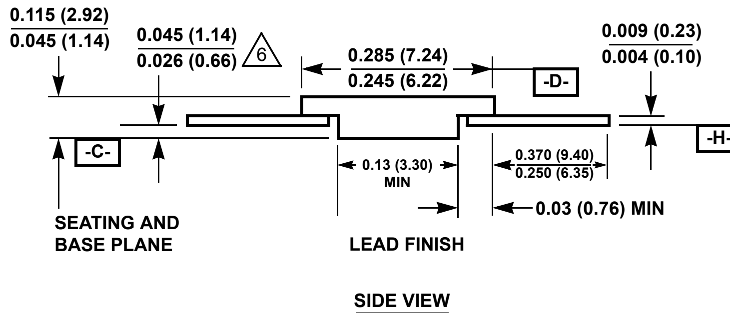
For the most recent package outline drawing, see K16.4.

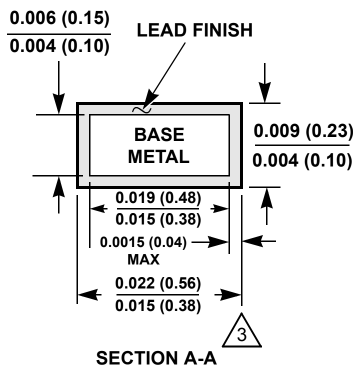
K16.A

16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 2, 1/10



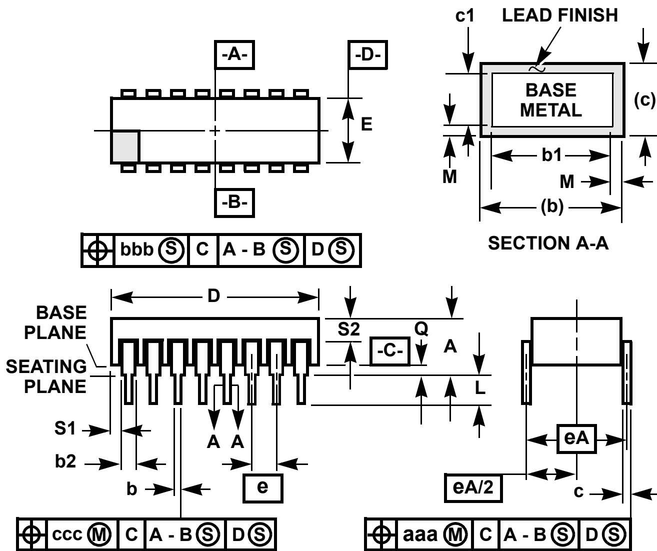




NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D16.3

MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)

16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

Rev. 0 4/94

For the most recent package outline drawing, see D16.3.