

HS-2420RH

Radiation Hardened Fast Sample and Hold

FN3554
 Rev 4.00
 December 2, 2013

The HS-2420RH is a radiation hardened monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and MOSFET input unity gain amplifier.

With an external hold capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operation amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

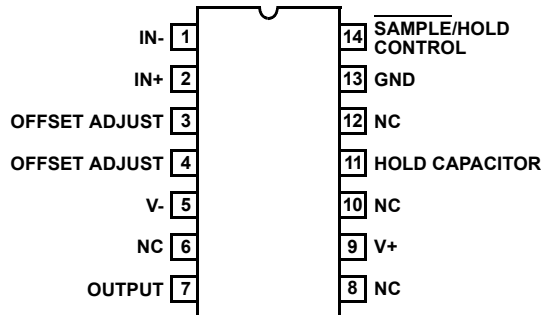
Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD [5962-95669](#).

14 LEAD METAL-SEALED SIDE-BRAZED CERAMIC DIP
MIL-STD-1835, CDIP2-T14
TOP VIEW



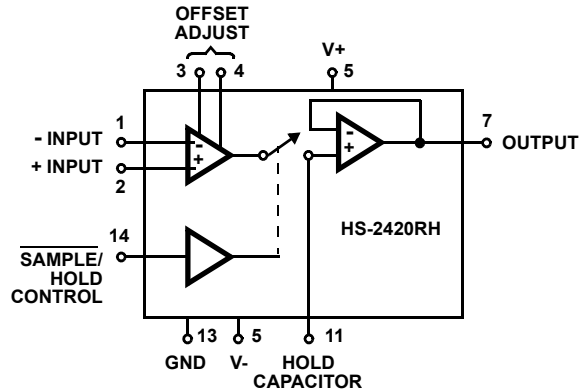
Features

- Electrically Screened to SMD # [5962-95669](#)
- QML Qualified per MIL-PRF-38535 Requirements
- Maximum Acquisition Time
 - 10V Step to 0.1% 4μs
 - 10V Step to 0.01% 6μs
- Maximum Drift Current 10nA (Maximum Over Temperature)
- TTL Compatible Control Input
- Power Supply Rejection ≥ 80dB
- Total Dose 100 krad(Si) (Max)
- No Latch-Up

Applications

- Data Acquisition Systems
- D to A Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Op Amp

Functional Diagram



Ordering Information

ORDERING SMD NUMBER (Note 1)	PART NUMBER (Note 2)	TEMPERATURE RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962R9566901VCC	HS1B-2420RH-Q	-55 to +125	14 Ld SBDIP	D14.3
HS1B-2420RH/PROTO	HS1B-2420RH/PROTO	-55 to +125	14 Ld SBDIP	D14.3

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table must be used when ordering.

Test Circuits

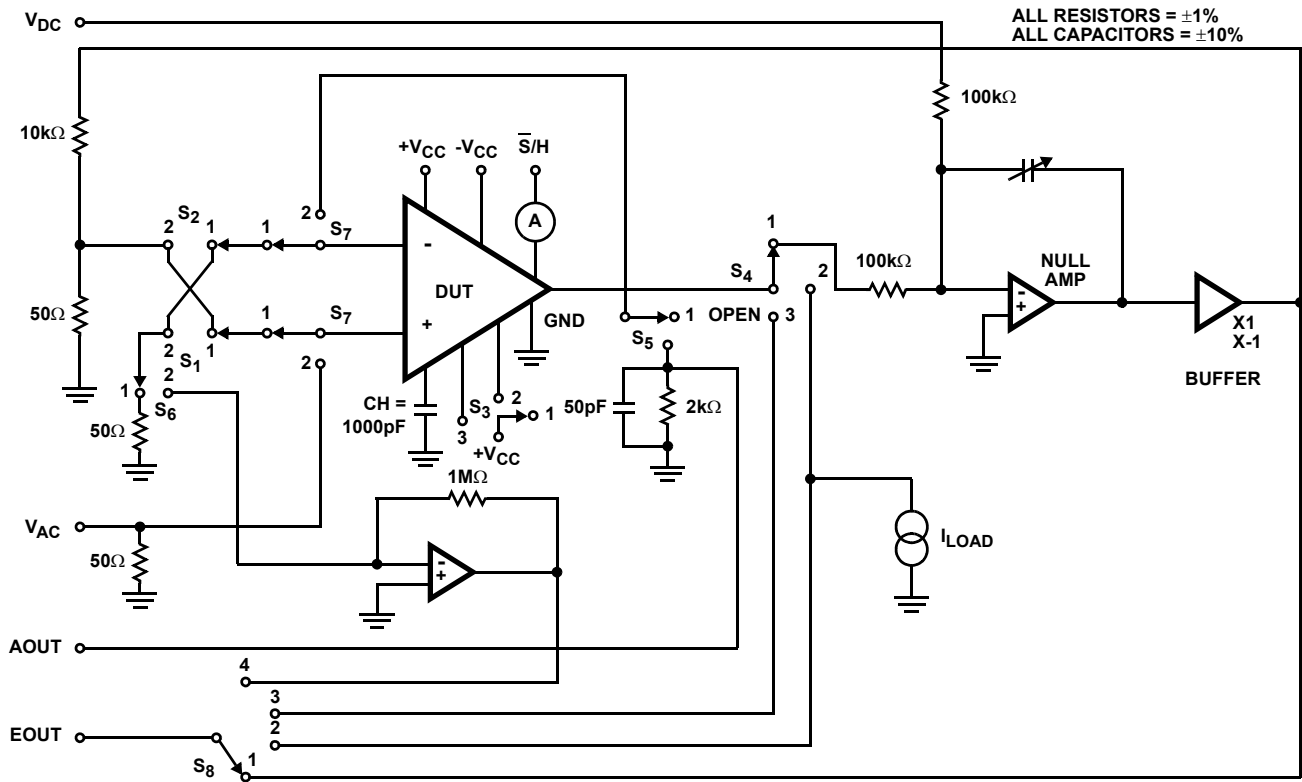
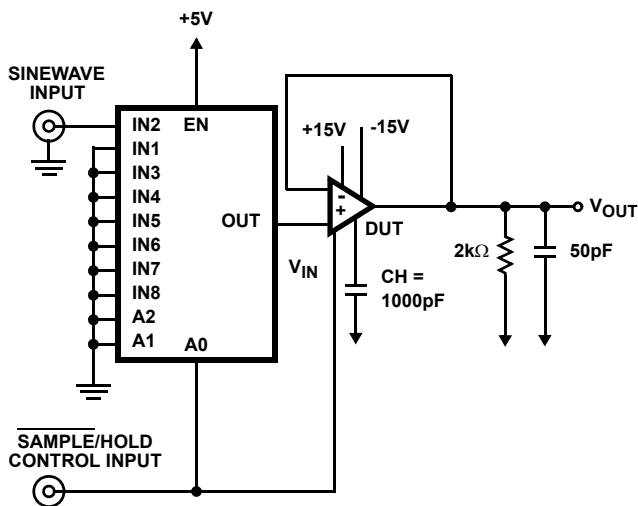


FIGURE 1. TEST FIXTURE SCHEMATIC (SWITCH POSITIONS S₁ - S₈ DETERMINE CONFIGURATION)

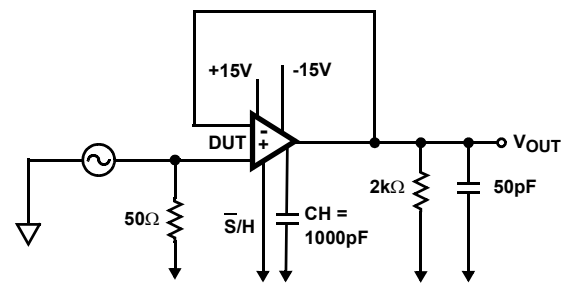


NOTE: Compute Hold Mode Feedthrough Attenuation from the Formula:

$$\text{FeedthroughAttenuation} = 20 \log \left(\frac{V_{\text{OUT HOLD}}}{V_{\text{IN HOLD}}} \right)$$

Where V_{OUT HOLD} = Peak-Peak Value of Output Sinewave during the Hold Mode.

FIGURE 2. HOLD MODE FEEDTHROUGH ATTENUATION

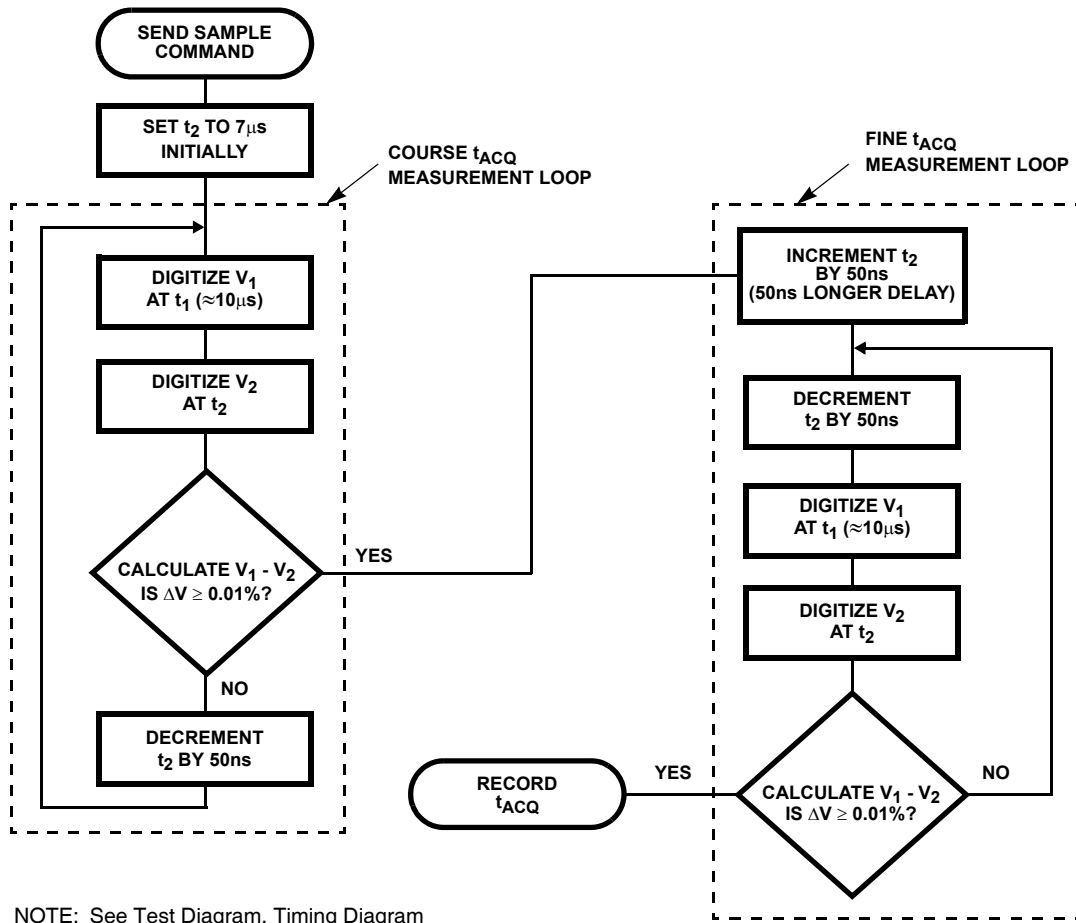


NOTE: GBWP is the Frequency of V_{INPUT} at which:

$$20 \log \left(\frac{V_{\text{OUT}}}{V_{\text{INPUT}}} \right) = -3\text{dB}$$

FIGURE 3. GAIN BANDWIDTH PRODUCT

Test Circuits (Continued)



NOTE: See Test Diagram, Timing Diagram

FIGURE 4. ACQUISITION TIME (t_{ACQ} TO 0.01% IS SHOWN, t_{ACQ} TO 0.1% IS DONE IN THE SAME MANNER)

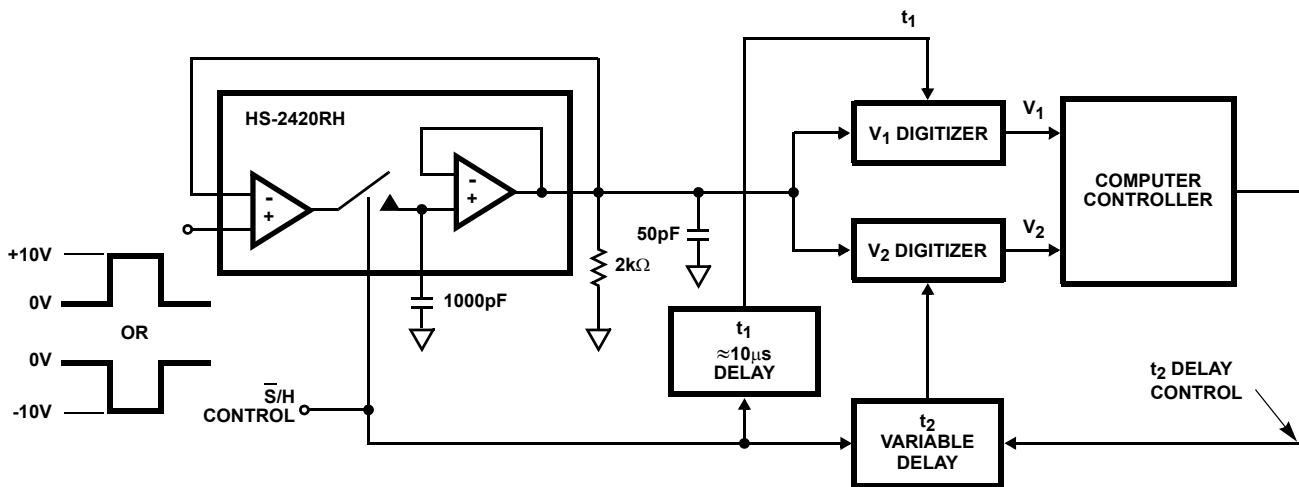


FIGURE 5.

Timing Waveforms

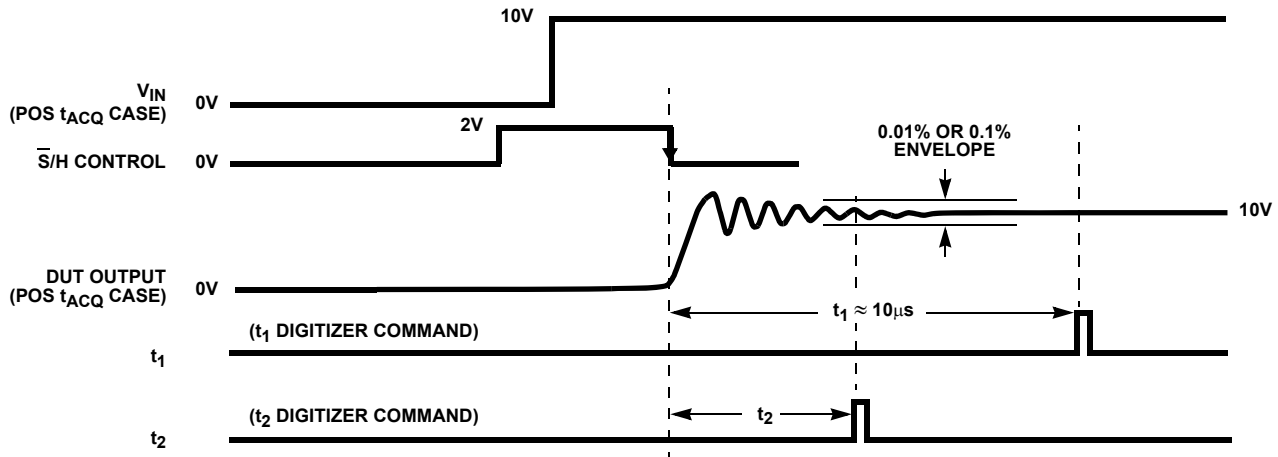


FIGURE 6. TIMING DIAGRAM FOR ACQUISITION TIME, (POSITIVE t_{ACQ} CASE)

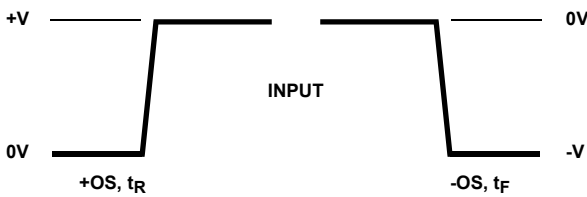


FIGURE 7A.

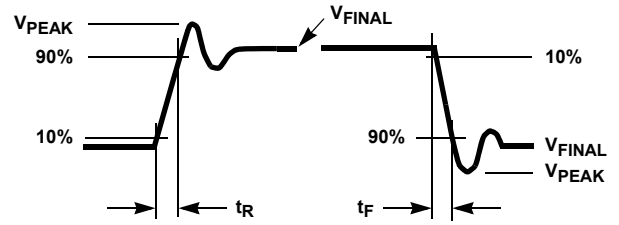


FIGURE 7B.

FIGURE 7. OVERSHOOT, RISE AND FALL TIME WAVEFORMS

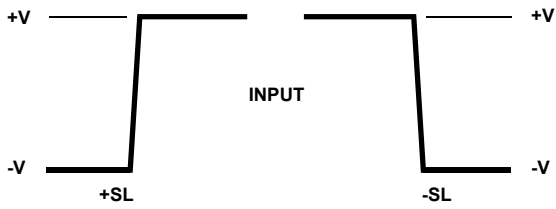


FIGURE 8A.

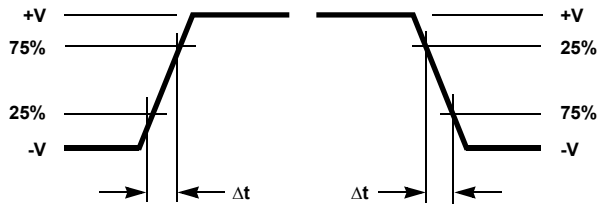


FIGURE 8B.

FIGURE 8. SLEW RATE WAVEFORMS

Typical Performance Curves $V_{SUPPLY} = \pm 15V_{DC}$, $T_A = +25^{\circ}C$, $CH = 1000pF$, Unless Otherwise Specified

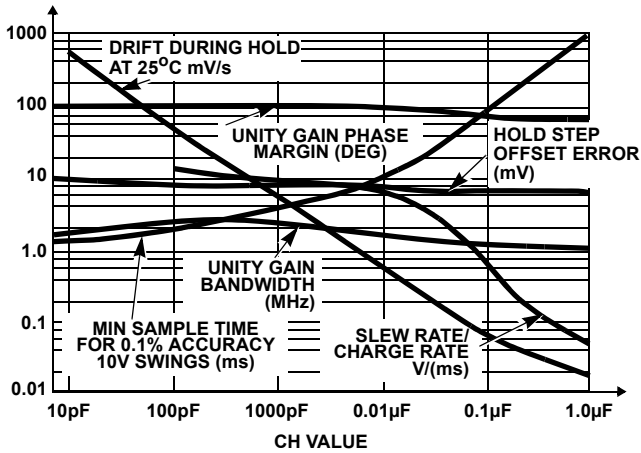


FIGURE 9. TYPICAL SAMPLE AND HOLD PERFORMANCE vs HOLDING CAPACITOR

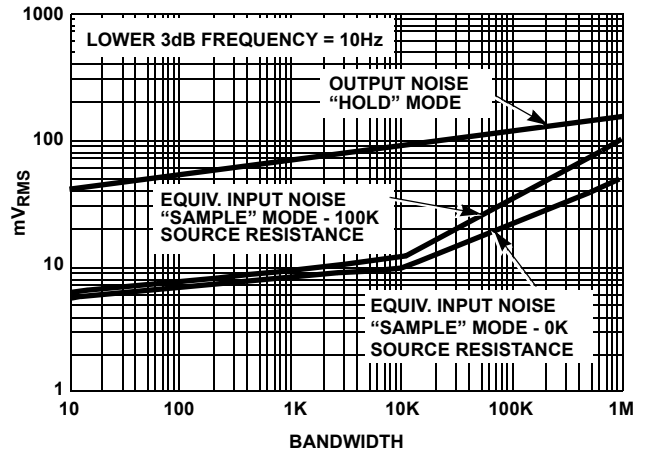


FIGURE 10. BROADBAND NOISE CHARACTERISTICS

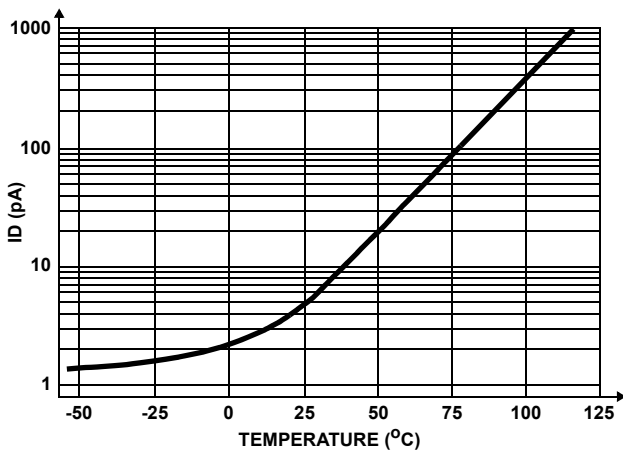


FIGURE 11. DRIFT CURRENT vs TEMPERATURE

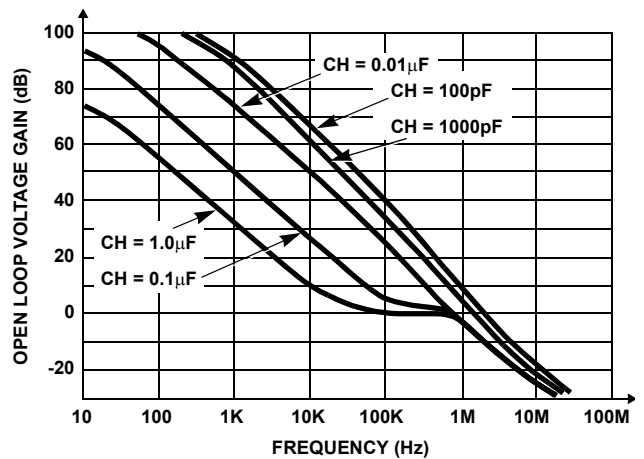


FIGURE 12. OPEN LOOP FREQUENCY RESPONSE

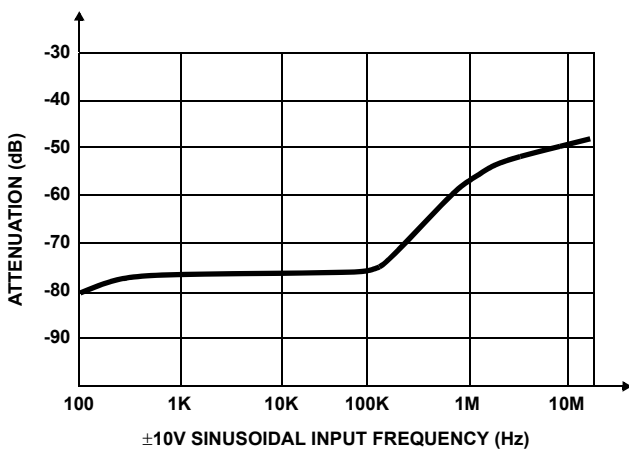


FIGURE 13. HOLD MODE FEEDTHROUGH ATTENUATION
CH = 1000pF

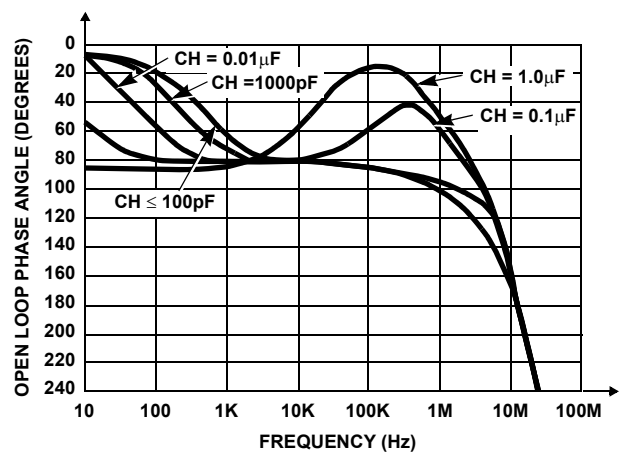
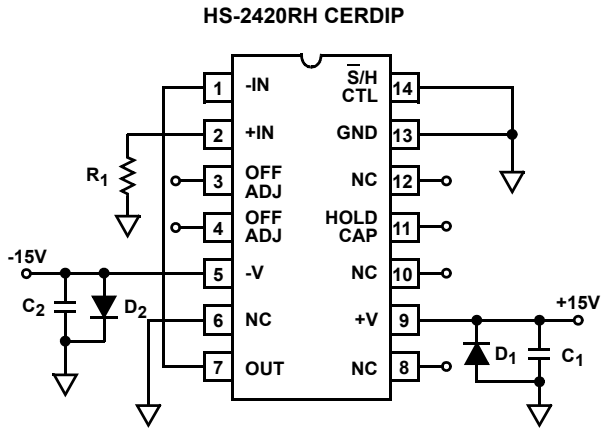


FIGURE 14. OPEN LOOP PHASE RESPONSE

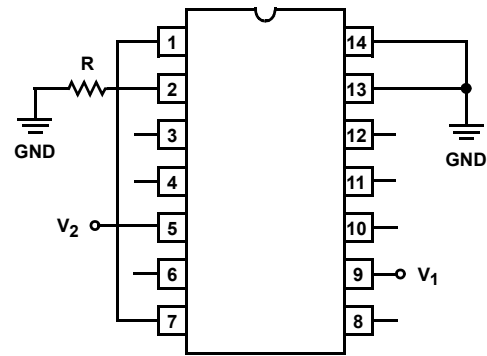
Burn-In Circuit



NOTES:

- R₁ = 100kΩ ±5% (per socket)
- C₁ = C₂ = 0.1μF (one per row) or 0.01μF (one per socket)
- D₁ = D₂ = 1N4002 or equivalent (per board)

Irradiation Circuit



NOTES:

- V₁ = +15V
- V₂ = -15V
- R = 100kΩ

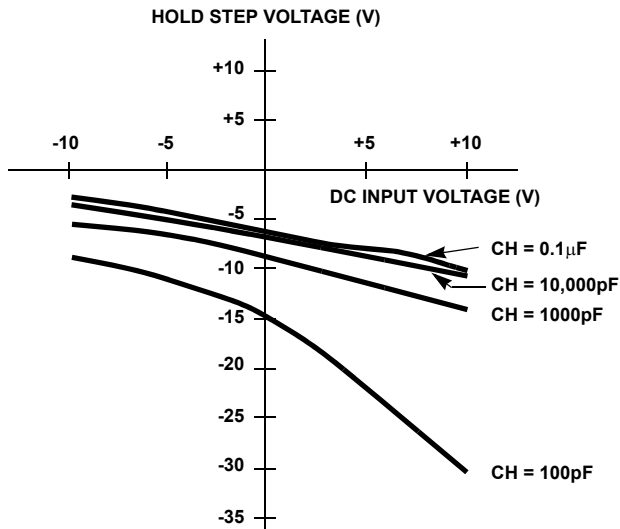


FIGURE 15. HOLD STEP vs INPUT VOLTAGE

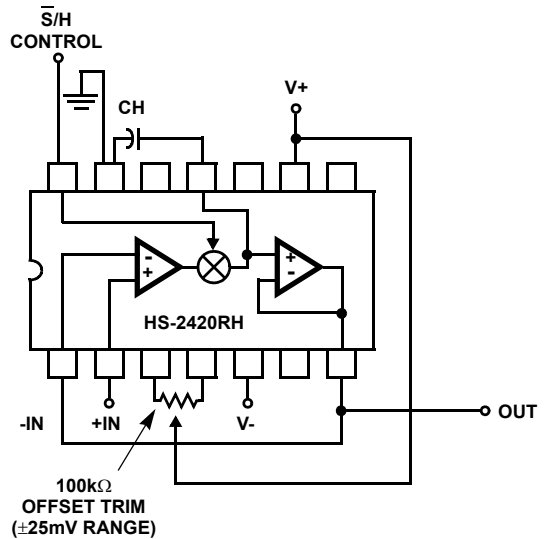


FIGURE 16. BASIC SAMPLE-AND-HOLD with OFFSET TRIM

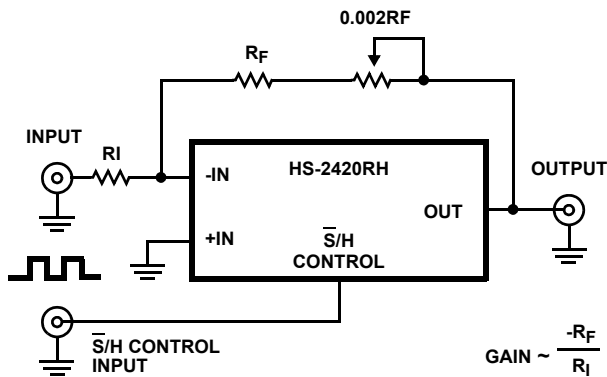


FIGURE 17. INVERTING CONFIGURATION with GAIN ADJUST

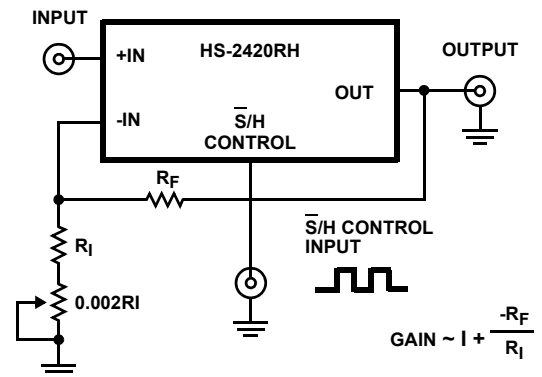


FIGURE 18. NONINVERTING CONFIGURATION WITH GAIN ADJUST

HS-2420RH

Offset and Gain Adjustment

Offset Adjustment

The offset voltage of the HS-2420RH may be adjusted using a 100k Ω trim pot, as shown in Figure 16. The recommended adjustment procedure is:

1. Apply 0V to the sample-and-hold input, and a square wave to the S/H control.
2. Adjust the trim pot for 0V output in the hold mode.

Gain Adjustment

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (CH = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. Figures 17 and 18 illustrate how to implement gain error adjust on the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.

Measure the output hold voltage (V-10 NOMINAL). Adjust the trim pot for an output hold voltage of:

$$\frac{(V-10 \text{ NOMINAL}) + (-10V)}{2}$$

Die Characteristics

DIE DIMENSIONS:

97 mils x 61 mils x 19 mils

METALLIZATION:

Type: Al
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:

Type: Silox
Thickness: 14kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:

$2.0 \times 10^5 \text{ A/cm}^2$

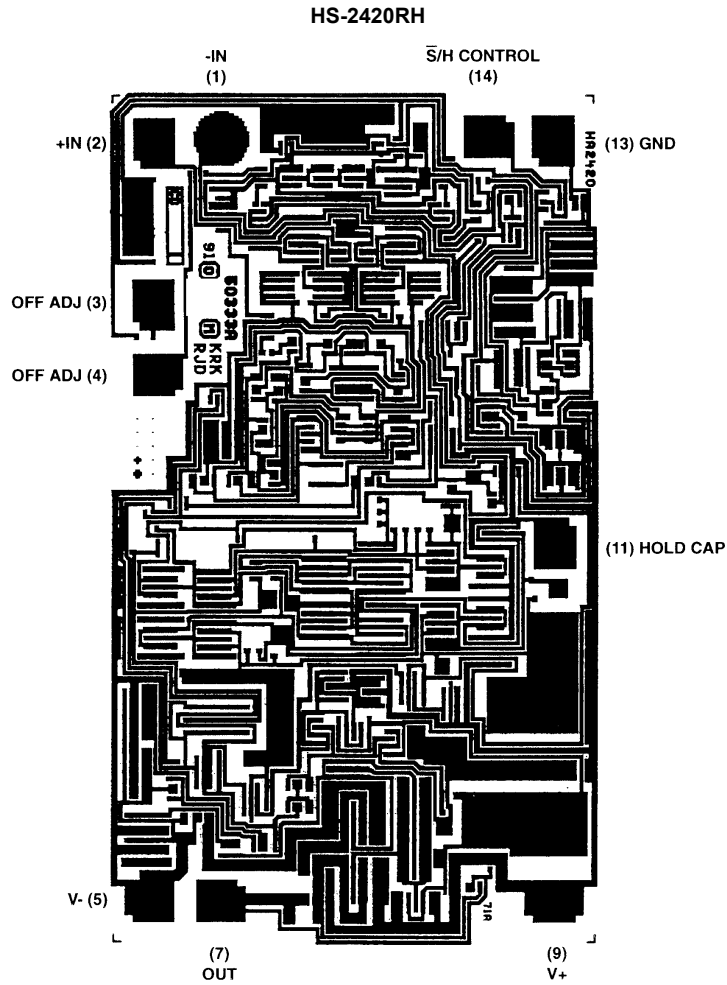
TRANSISTOR COUNT:

78

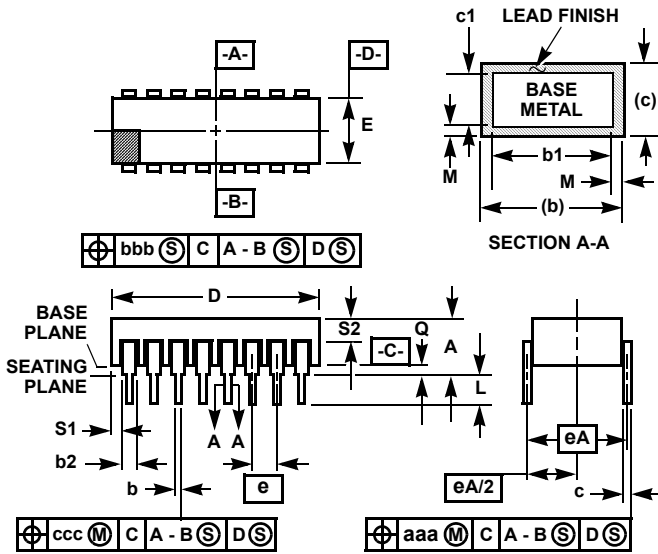
PROCESS:

Bipolar-Di

Metallization Mask Layout



Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



**D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C)
14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

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