# **inter<sub>sil</sub>**"

### HS-2420EH

Radiation Hardened Fast Sample and Hold

# DATASHEET

FN8727 Rev 0.00 March 17, 2015

The HS-2420EH is a radiation hardened monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier.

With an external hold capacitor connected to the switch output, a versatile high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened, the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD <u>5962-95669</u>.

#### **Features**

- Electrically screened to SMD #5962-95669
- QML qualified per MIL-PRF-38535 requirements
- · Maximum acquisition time

- 10V Step to 0.1% 4   - 10V Step to 0.01% 6	δµs
Maximum drift current 10 (maximum over-temperature)	nA

- TTL compatible control input
- Power supply rejection  $\ldots \ge 80 dB$
- Radiation tolerance
  - High dose rate (50 to 300rad(Si)/s) ..... 100krad(Si)
  - Low dose rate (0.01rad(Si)/s) ..... 100krad(Si)\*

\* Only the EH device is wafer-by-wafer acceptance tested at the low dose rate and guaranteed to 50krad(Si). The 100krad(Si) limit is established by characterization only.

No latch-up

### **Applications**

- · Data acquisition systems
- D to A deglitcher
- · Auto zero systems
- Peak detector
- · Gated op amp

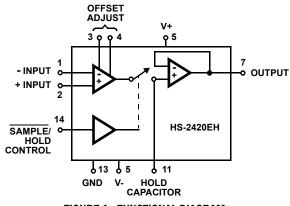
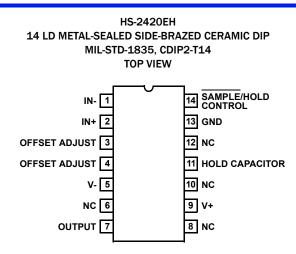


FIGURE 1. FUNCTIONAL DIAGRAM

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### **Pin Descriptions**

PIN #	PIN NAME	DESCRIPTION
1	IN-	Inverting input to the operational amplifier
2	IN+	Non-inverting input to the operational amplifier
3, 4	OFFSET ADJUST	Connect a 100 $k\Omega$ potentiometer across these pins to null out the offset voltage.
5	V-	Negative power supply
6, 8, 10, 12	NC	No connect pin.
7	OUTPUT	Output of the unity gain amplifier
9	V+	Positive Power Supply
11	HOLD CAPACITOR	Connect the hold capacitor between this pin and GND.
13	GND	Ground connection of the device
14	SAMPLE/HOLD CONTROL	Control input to the series analog switch.

### **Ordering Information**

ORDERING SMD NUMBER (Note 1)	PART NUMBER (Note 2)	TEMPERATURE RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962R9566902VCC	HS1B-2420EH-Q	-55 to +125	14 Ld SBDIP	D14.3
HS1B-2420EH/PROTO	HS1B-2420EH/PROTO	-55 to +125	14 Ld SBDIP	D14.3

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table must be used when ordering.

### **Test Circuits**

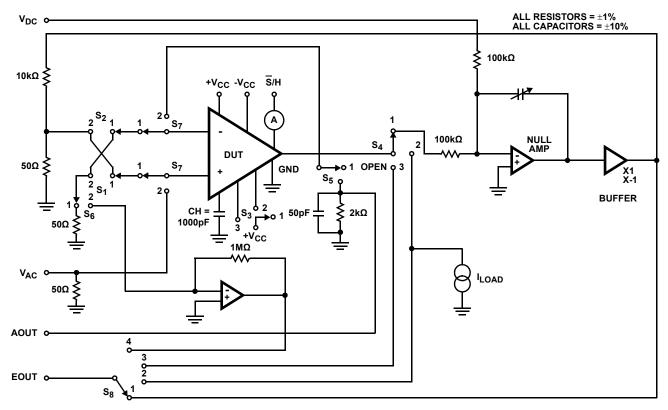
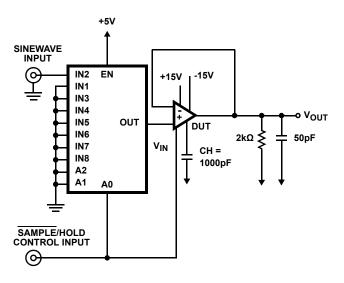


FIGURE 2. TEST FIXTURE SCHEMATIC (SWITCH POSITIONS  $S_1 - S_8$  DETERMINE CONFIGURATION)

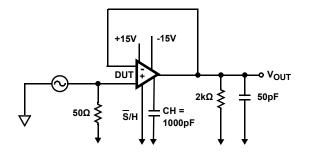


NOTE: Compute Hold mode feedthrough attenuation from the formula:

Feedthrough Attenuation =  $20 \log \left( \frac{V_{OUT HOLD}}{V_{OUT HOLD}} \right)$ 

Where  $V_{OUT HOLD}$  = peak-to-peak value of output Sinewave during the Hold mode.

#### FIGURE 3. HOLD MODE FEEDTHROUGH ATTENUATION

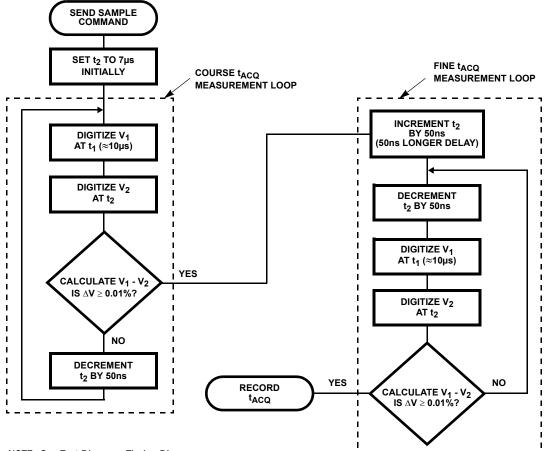


NOTE: GBWP is the frequency of  $V_{\mbox{\scriptsize INPUT}}$  at which:

$$20 \log \left( \frac{V_{OUT}}{V_{INPUT}} \right) = -3 dB$$

#### FIGURE 4. GAIN BANDWIDTH PRODUCT





NOTE: See Test Diagram, Timing Diagram

FIGURE 5. ACQUISITION TIME (t<sub>ACQ</sub> TO 0.01% IS SHOWN, t<sub>ACQ</sub> TO 0.1% IS DONE IN THE SAME MANNER)

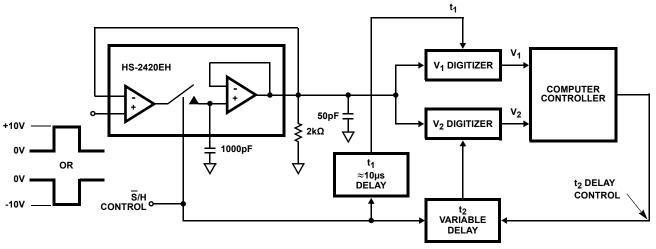


FIGURE 6. BLOCK DIAGRAM FOR ACQUISITION TIME MEASUREMENT

### **Timing Waveforms**

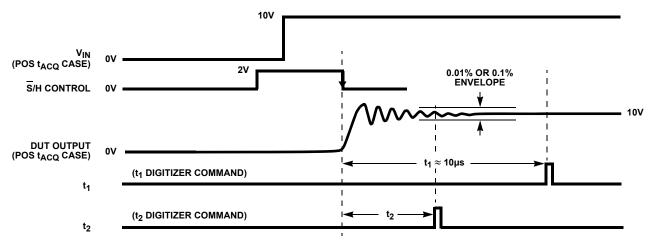


FIGURE 7. TIMING DIAGRAM FOR ACQUISITION TIME, (POSITIVE  $\ensuremath{\mathsf{t}_{\mathsf{ACQ}}}$  CASE)

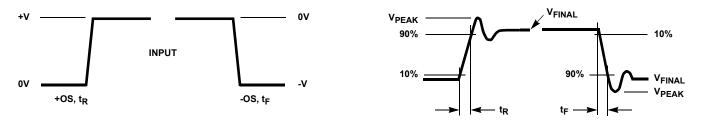
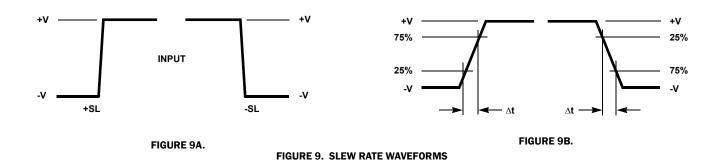


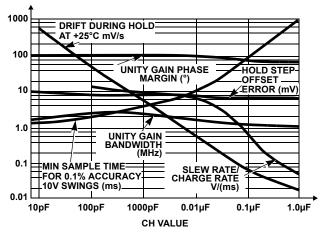
FIGURE 8A.

FIGURE 8B.

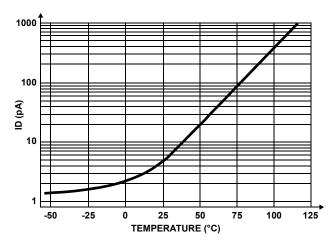




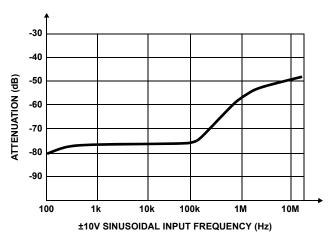
#### Typical Performance Curves V<sub>SUPPLY</sub> = ±15V<sub>DC</sub>, T<sub>A</sub> = +25°C, CH = 1000pF, Unless Otherwise Specified



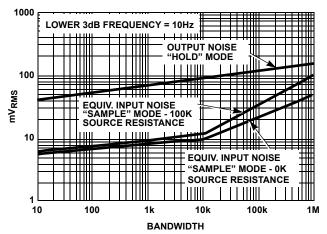














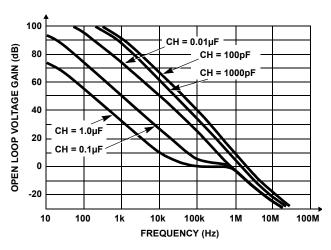


FIGURE 13. OPEN LOOP FREQUENCY RESPONSE

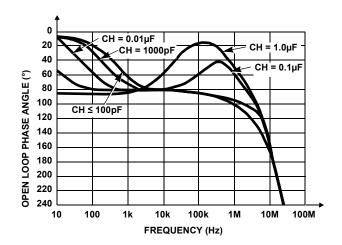
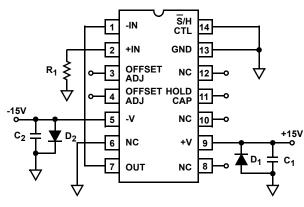


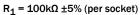
FIGURE 15. OPEN LOOP PHASE RESPONSE

### **Burn-in Circuit**





NOTES:



 $C_1^- = C_2 = 0.1 \mu F$  (one per row) or  $0.01 \mu F$  (one per socket)  $D_1 = D_2 = 1N4002$  or equivalent (per board)

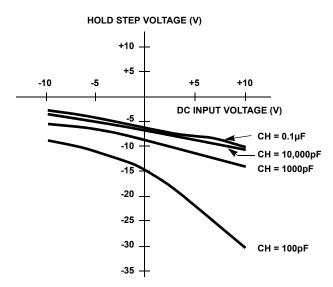


FIGURE 16. HOLD STEP vs INPUT VOLTAGE

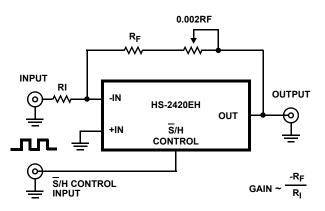
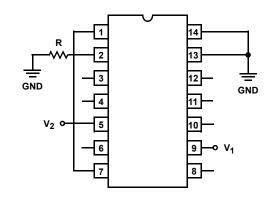


FIGURE 18. INVERTING CONFIGURATION with GAIN ADJUST

### **Irradiation Circuit**



NOTES:  $V_1 = +15V$  $V_2 = -15V$ R = 100k $\Omega$ 

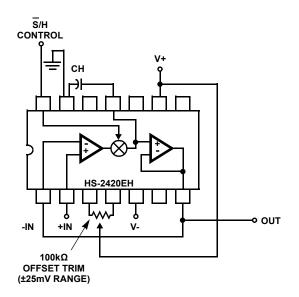


FIGURE 17. BASIC SAMPLE-AND-HOLD with OFFSET TRIM

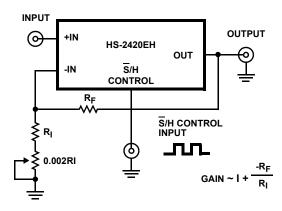


FIGURE 19. NONINVERTING CONFIGURATION WITH GAIN ADJUST

### **Offset and Gain Adjustment**

#### **Offset Adjustment**

The offset voltage of the HS-2420EH may be adjusted using a  $100k\Omega$  trim pot, as shown in Figure 17. The recommended adjustment procedure is:

- 1. Apply OV to the sample-and-hold input, and a square wave to the  $\overline{S}/H$  control.
- 2. Adjust the trim pot for OV output in the hold mode.

#### **Gain Adjustment**

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (CH = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. Figures 18 and 19 illustrate how to implement gain error adjust on the sample-and-hold.

The recommended procedure for adjusting gain error is:

- 1. Perform offset adjustment.
- 2. Apply the nominal input voltage that should produce a +10V output.
- 3. Adjust the trim pot for +10V output in the hold mode.
- 4. Apply the nominal input voltage that should produce a -10V output.

Measure the output hold voltage (V-10 NOMINAL). Adjust the trim pot for an output hold voltage of:

(V-10 NOMINAL) + (-10 V)

### **Die Characteristics**

#### **DIE DIMENSIONS:**

97mils x 61mils x 19mils

#### **METALLIZATION:**

Type: Al Thickness: 16kÅ ± 2kÅ

#### GLASSIVATION:

Type: Silox Thickness: 14kÅ ± 2kÅ

### **Metallization Mask Layout**

#### WORST CASE CURRENT DENSITY:

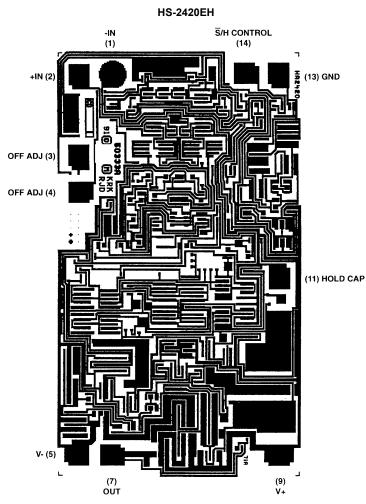
2.0 x 10<sup>5</sup>A/cm<sup>2</sup>

#### TRANSISTOR COUNT:

78

#### PROCESS:

Bipolar-Di



### **Revision History**

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
March 17, 2015	FN8727.0	Initial Release

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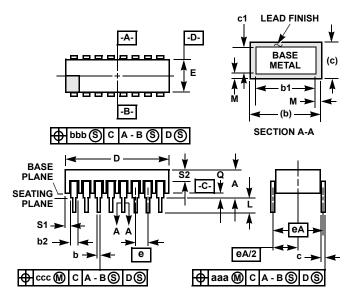
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#### Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



#### NOTES:

- 1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- 2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
- 3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
- Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
- 5. Dimension Q shall be measured from the seating plane to the base plane.
- 6. Measure dimension S1 at all four corners.
- 7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
- 8. N is the maximum number of terminal positions.
- 9. Braze fillets shall be concave.
- 10. Dimensioning and tolerancing per ANSI Y14.5M 1982.
- 11. Controlling dimension: INCH.

#### D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C) 14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

	INC	HES	MILLIN		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
с	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
е	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90 <sup>0</sup>	105 <sup>0</sup>	90 <sup>0</sup>	105 <sup>0</sup>	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ссс	-	0.010	-	0.25	-
м	-	0.0015	-	0.038	2
Ν	14		1	.4	8

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