

HS-1840ARH-T

Radiation Hardened 16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

FN4589
Rev 1.00
July 1999

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD Total Dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The HS-1840ARH-T is a Radiation Hardened, monolithic 16 channel multiplexer constructed with the Intersil Rad-Hard Silicon Gate, Dielectric Isolation process. It is designed to provide a high input impedance to the analog source if device power fails (open), or the analog signal voltage inadvertently exceeds the supply by up to $\pm 35V$, regardless of whether the device is powered on or off. Selection of one of sixteen channels is controlled by a 4-bit binary address plus an Enable-Inhibit input, which conveniently controls the ON/OFF operation of several multiplexers in a system. All inputs have electrostatic discharge protection.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HS-1840ARH-T are contained in SMD 5962-95630. For more information, visit us on our website at: www.intersil.com/

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.

www.intersil.com/

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)
5962R9563002TXC	HS1-1840ARH-T	-55 to 125
HS1-1840ARH/Proto	HS1-1840ARH/Proto	-55 to 125
5962R9563002TYC	HS9-1840ARH-T	-55 to 125
HS9-1840ARH/Proto	HS9-1840ARH/Proto	-55 to 125

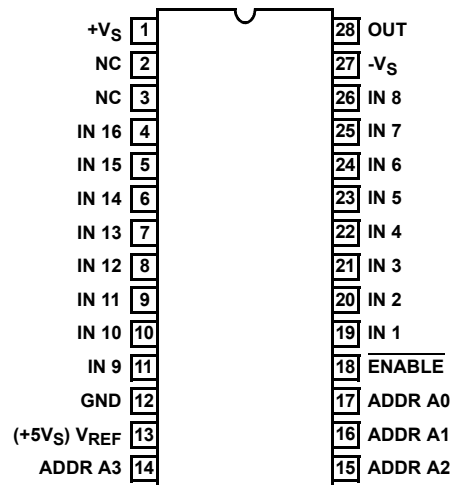
NOTE: **Minimum order quantity for -T is 150 units through distribution, or 450 units direct.**

Features

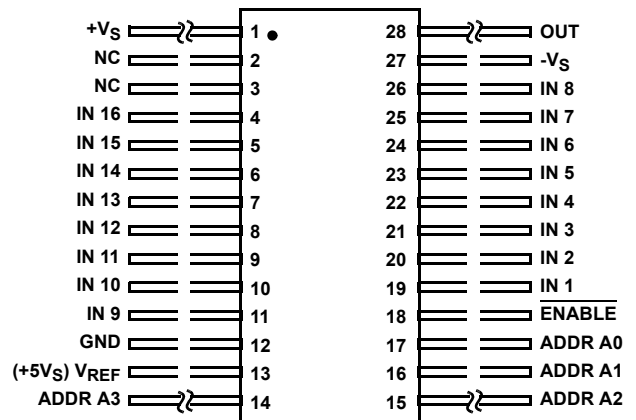
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
 - Gamma Dose (γ) 1×10^5 RAD(Si)
 - No Latch-Up, Dielectrically Isolated Device Islands
- Improved $r_{DS(ON)}$ Linearity
- Improved Access Time 1.5 μ s (Max) Over Temp and Rad
- High Analog Input Impedance 500M Ω During Power Loss (Open)
- $\pm 35V$ Input Over Voltage Protection (Power On or Off)
- Excellent in Hi-Rel Redundant Systems
- Break-Before-Make Switching

Pinouts

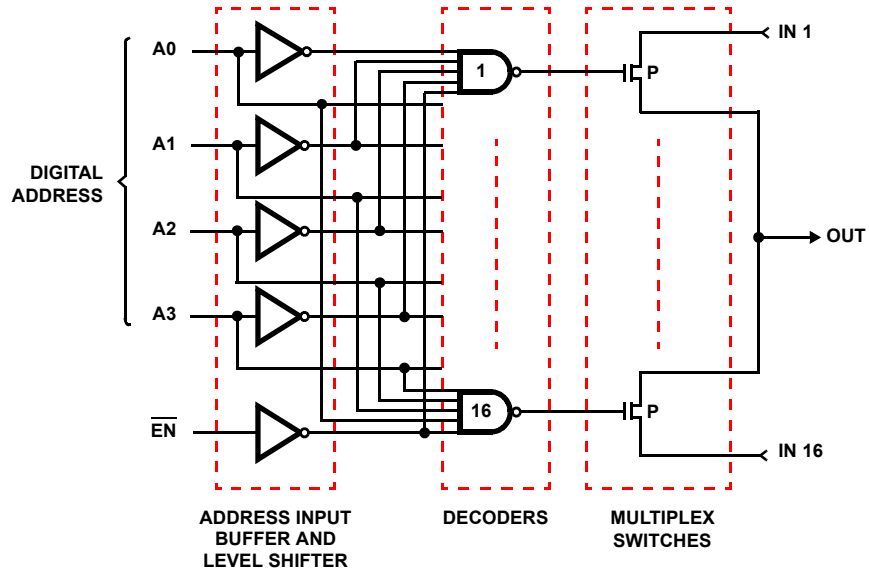
HS1-1840ARH-T (SBDIP), CDIP2-T28
TOP VIEW



HS9-1840ARH-T (FLATPACK) CDFP3-F28
TOP VIEW



Functional Diagram



TRUTH TABLE

A3	A2	A1	A0	$\overline{\text{EN}}$	"ON" CHANNEL
X	X	X	X	H	None
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

Die Characteristics

DIE DIMENSIONS:

(2820μm x 4080μm x 483μm ±25.4μm)
 111 x 161 x 19mils ±1mil

METALLIZATION:

Type: Al Si Cu
 Thickness: 16.0kÅ ±2kÅ

SUBSTRATE POTENTIAL:

Unbiased (DI)

BACKSIDE FINISH:

Silicon

PASSIVATION:

Type: Nitride (Si₃N₄) over Silox (SiO₂)
 Nitride Thickness: 4.0kÅ ±0.5kÅ
 Silox Thickness: 12.0kÅ ±1.3kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm²

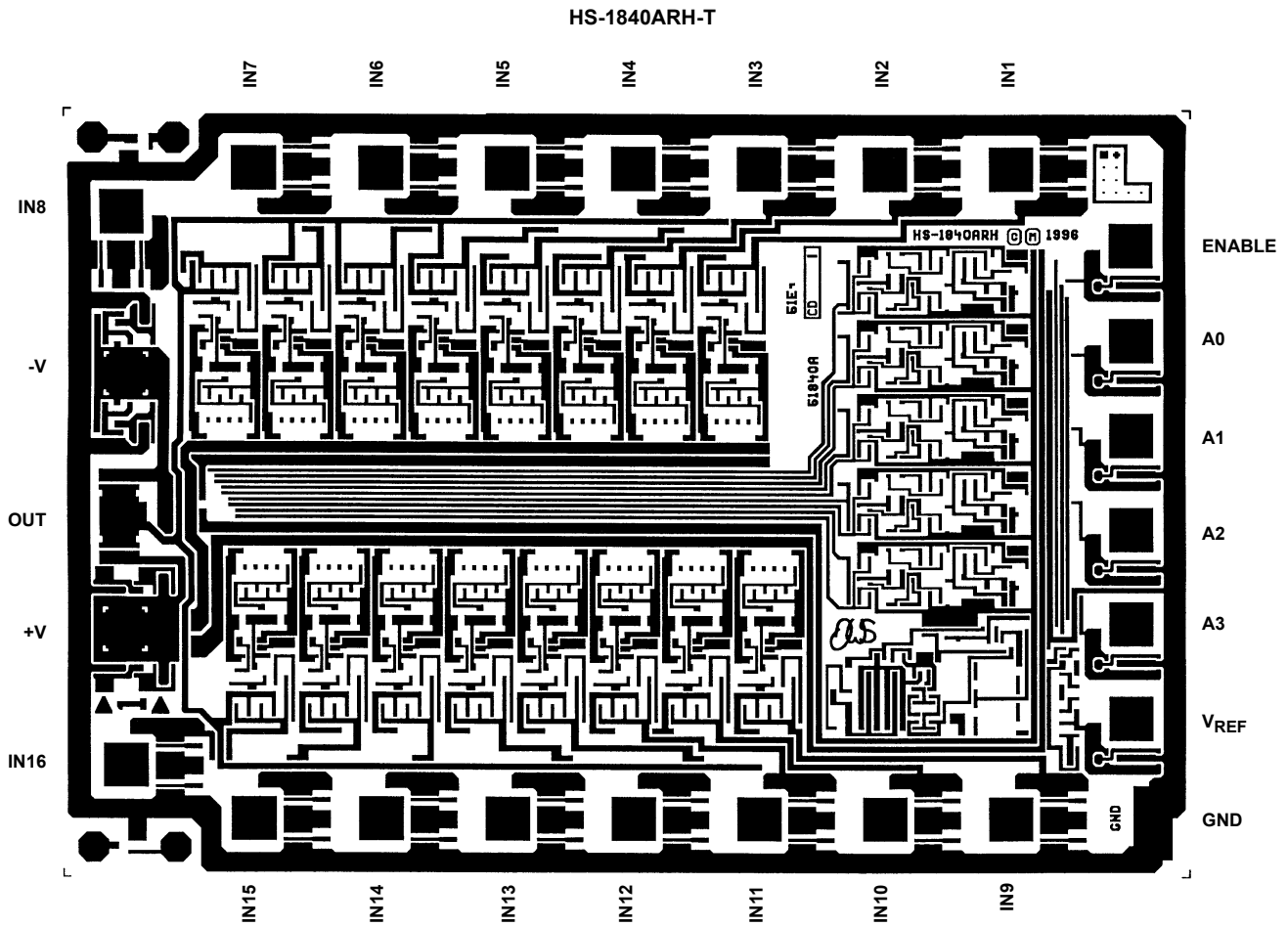
TRANSISTOR COUNT:

407

PROCESS:

Radiation Hardened Silicon Gate, Dielectric Isolation

Metallization Mask Layout



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