HN58C256AI Series

256k EEPROM (32-kword × 8-bit)

R10DS0218EJ0100
Rev.1.00
Oct 07, 2013

Description

Renesas Electronics' HN58C256AI are electrically erasable and programmable ROMs organized as 32768-word × 8-bit. They have realized high speed low power consumption and high reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

Features

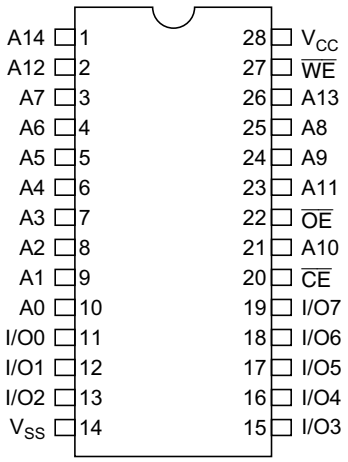
- Single 5 V supply: 5 V ±10%
- Access time: 85 ns/100 ns (max)
- Power dissipation
  - Active: 20 mW/MHz, (typ)
  - Standby: 110 µW (max)
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- $\overline{Data}$ polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- There are lead free products

Ordering Information

Orderable Part Name	Access time	Package	Shipping Container	Quantity
HN85C256API85E	85ns	600mil 28-pin plastic DIP PRDP0028AB-A (DP-28V)	Tube	Max. 13 pcs/tube Max. 325 pcs/inner box
HN85C256API10E	100ns			
HN85C256AFPI85E	85ns	400mil 28-pin plastic SOP PRSP0028DC-A (FP-28DV)	Tube	Max. 25 pcs/tube Max. 1,000 pcs/inner box
HN85C256AFPI10E	100ns			
HN85C256AFPI85EZ	85ns		Tape and reel	1,000 pcs/reel
HN85C256AFPI10EZ	100ns			
HN85C256ATI85E	85ns	28-pin plastic TSOP PTSA0028ZB-A (TFP-28DBV)	Tray	Max. 60 pcs/tray Max. 600 pcs/inner box
HN85C256ATI10E	100ns			

Pin Arrangement

HN58C256API/AFPI Series



(Top view)

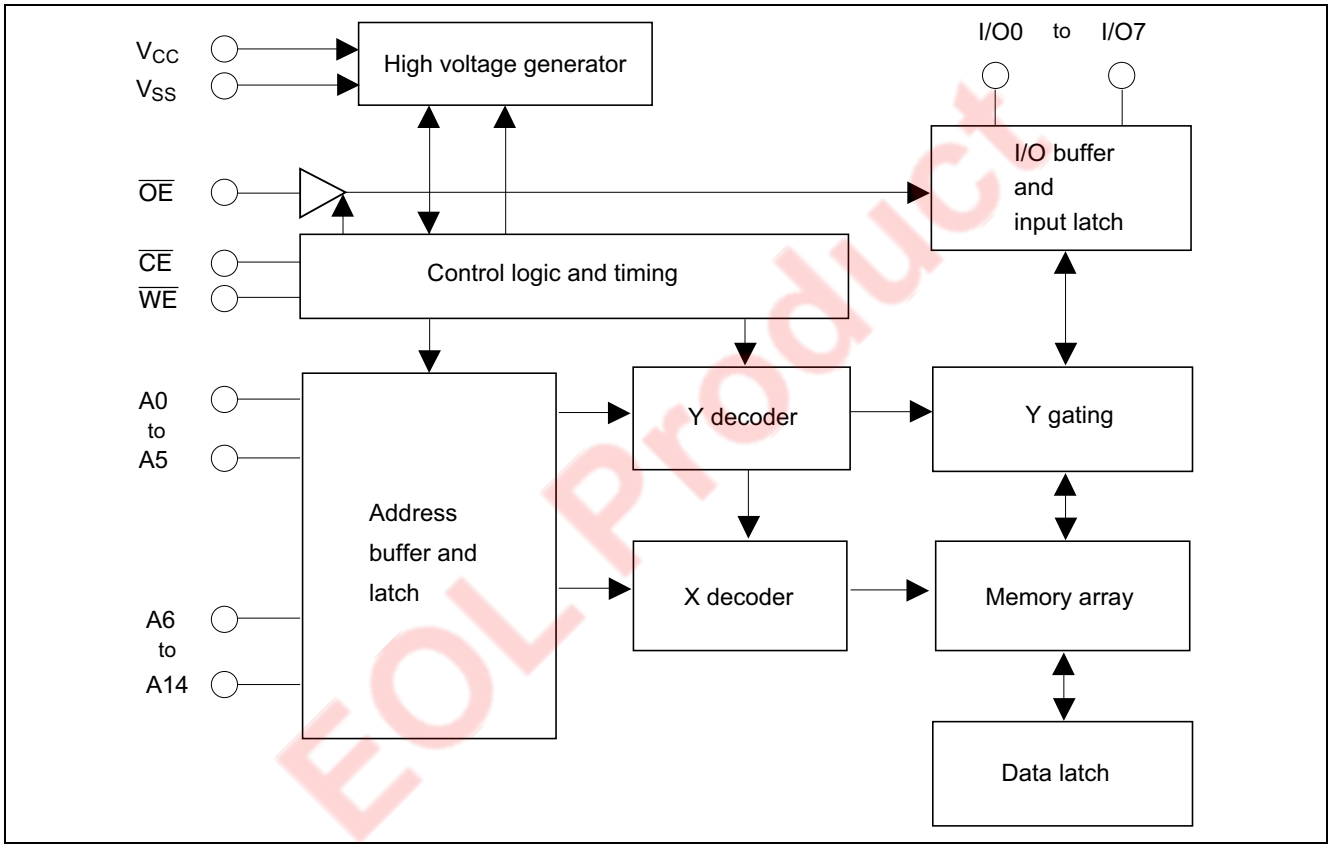
HN58C256ATI Series

(Top view)

Pin Description

Pin Name	Function
A0 to A14	Address input
I/O0 to I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Operation Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Dout
Standby	V_{IH}	×*1	×	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z
Write inhibit	×	×	V_{IH}	—
	×	V_{IL}	×	—
$\overline{Data}$ polling	V_{IL}	V_{IL}	V_{IH}	Dout (I/O7)
Program reset	×	×	×	High-Z

Note: 1. Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.6 to +7.0	V
Input voltage relative to V_{SS}	Vin	–0.5*1 to +7.0*3	V
Operating temperature range*2	Topr	–40 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. Vin min: –3.0 V for pulse width ≤ 50 ns
2. Including electrical characteristics and data retention
3. Should not exceed V_{CC} + 1 V.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IL}	–0.3*1	—	0.6	V
	V_{IH}	3.0	—	V_{CC} + 0.3*2	V
Operating temperature	Topr	–40	—	+85	°C

Notes: 1. V_{IL} min: –1.0 V for pulse width ≤ 50 ns
2. V_{IH} max: V_{CC} + 1.0 V for pulse width ≤ 50 ns

DC Characteristics

(Ta = –40 to +85°C, V_{CC} = 5.0 V ±10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
Standby V_{CC} current	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} current	I_{CC3}	—	—	12	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs, V_{CC} = 5.5 V
		—	—	30	mA	Iout = 0 mA, Duty = 100%, Cycle = 85 ns, V_{CC} = 5.5 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	$V_{CC} \times 0.8$	—	—	V	I_{OH} = –400 µA

Capacitance

(Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*[1]	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*[1]	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics

(Ta = –40 to +85°C, V_{CC} = 5.0 V ±10%)

Test Conditions

- Input pulse levels: 0.4 V to 3.0 V
- Input rise and fall time: ≤ 5 ns
- Input timing reference levels: 0.8, 2.0 V
- Output load: 1TTL Gate +100 pF
- Output reference levels: 1.5 V, 1.5 V

Read Cycle

Parameter	Symbol	HN58C256API/AFPI/ATI				Unit	Test conditions
		-85		-10			
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	—	85	—	100	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	85	—	100	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	40	10	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*[1]	t_{DF}	0	40	0	40	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

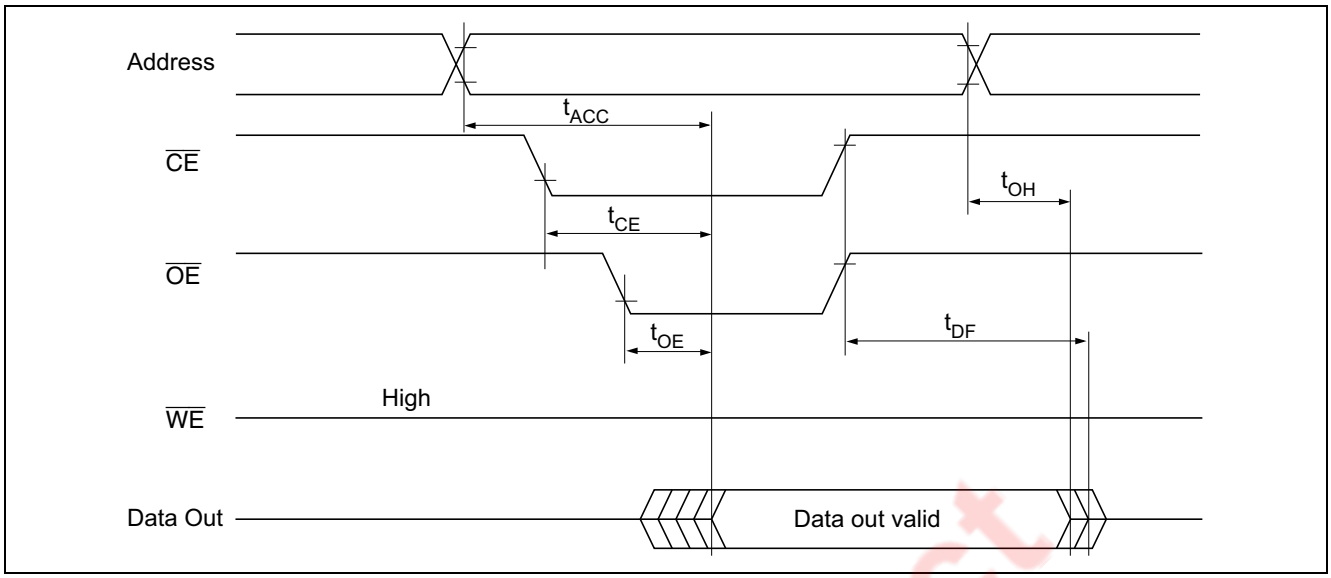
Write Cycle

Parameter	Symbol	Min*[2]	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	50	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	100	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	100	—	—	ns	
Data latch time	t_{DL}	50	—	—	ns	
Byte load cycle	t_{BLC}	0.2	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*[3]	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0*[4]	—	—	ns	

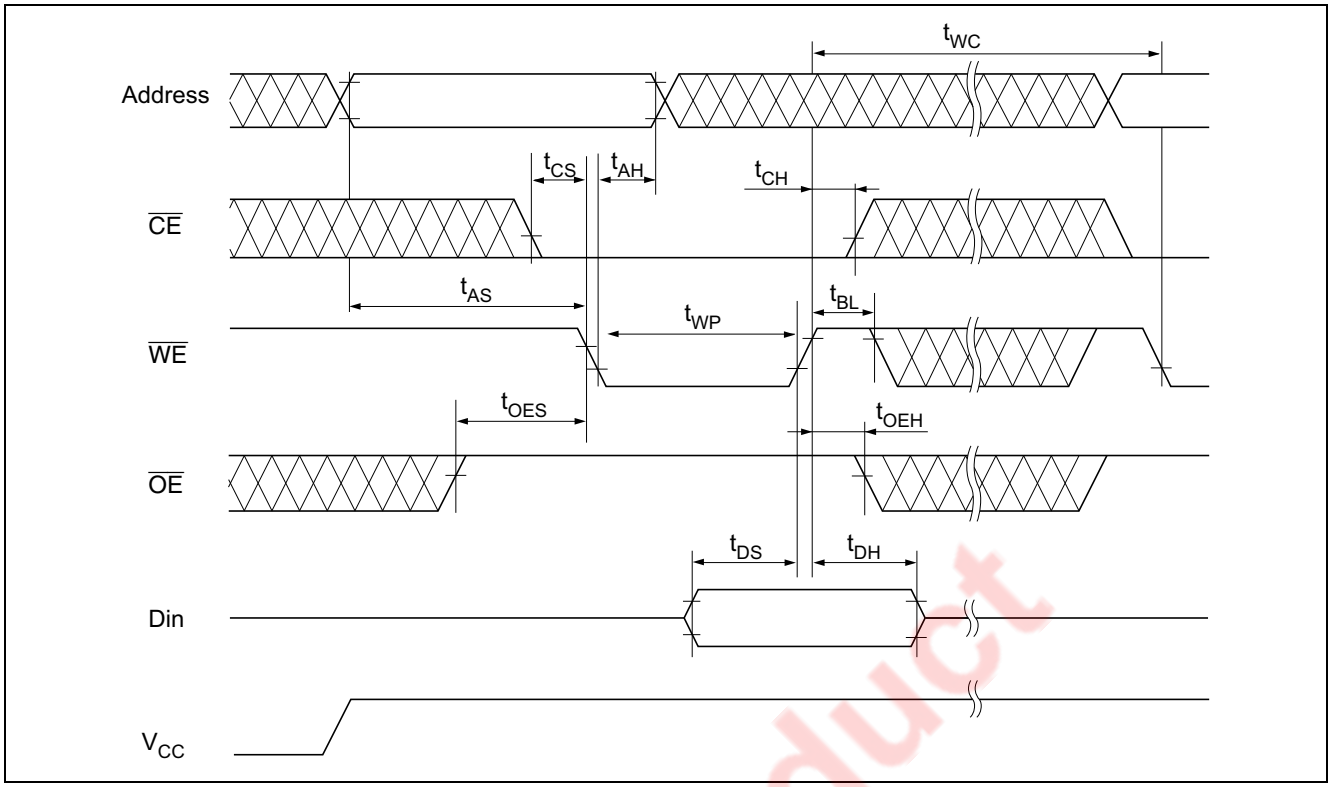
Notes: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
2. Use this device in longer cycle than this value.
3. t_{WC} must be longer than this value unless polling techniques are used. This device automatically completes the internal write operation within this value.
4. Next read or write operation can be initiated after t_{DW} if polling techniques are used.
5. A6 through A14 are page address and these addresses are latched at the first falling edge of $\overline{WE}$.
6. A6 through A14 are page address and these addresses are latched at the first falling edge of $\overline{CE}$.
7. See AC read characteristics.

Timing Waveforms

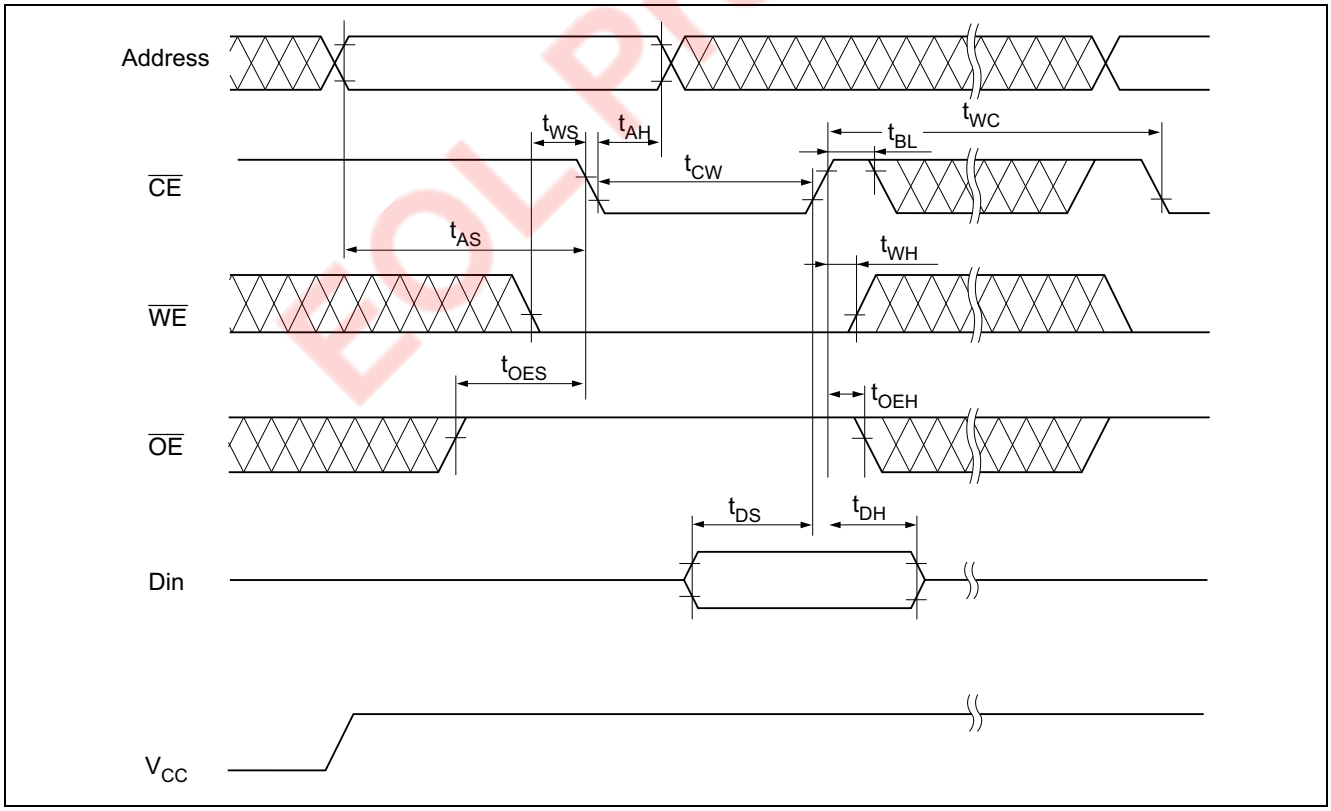
Read Timing Waveform



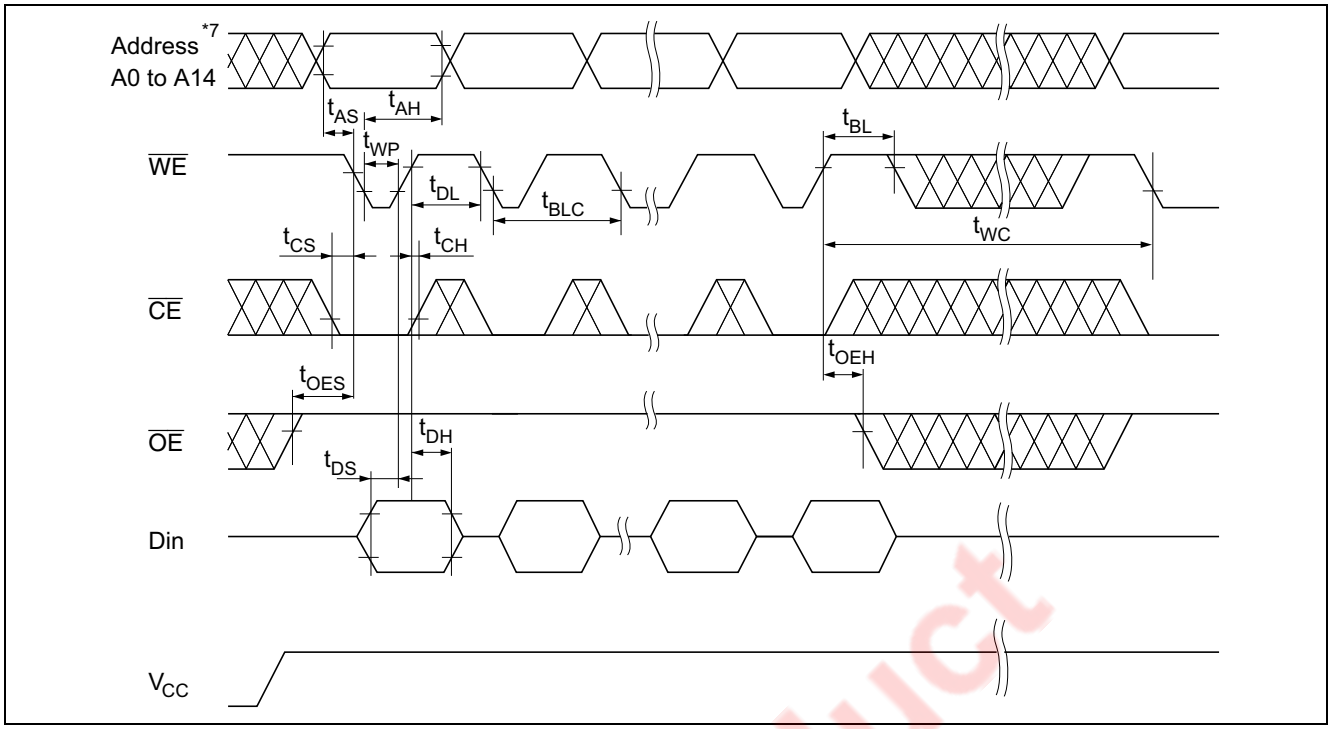
Byte Write Timing Waveform (1) ($\overline{WE}$ Controlled)



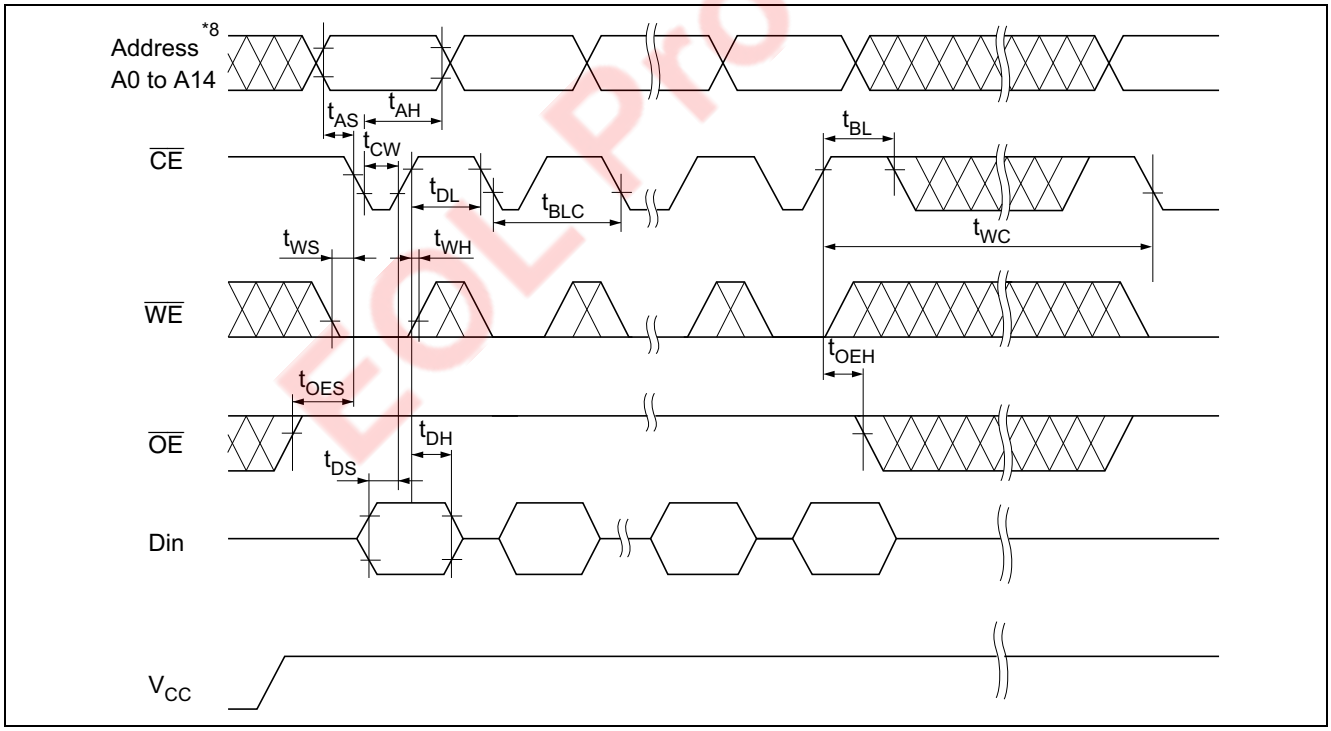
Byte Write Timing Waveform (2) ($\overline{CE}$ Controlled)



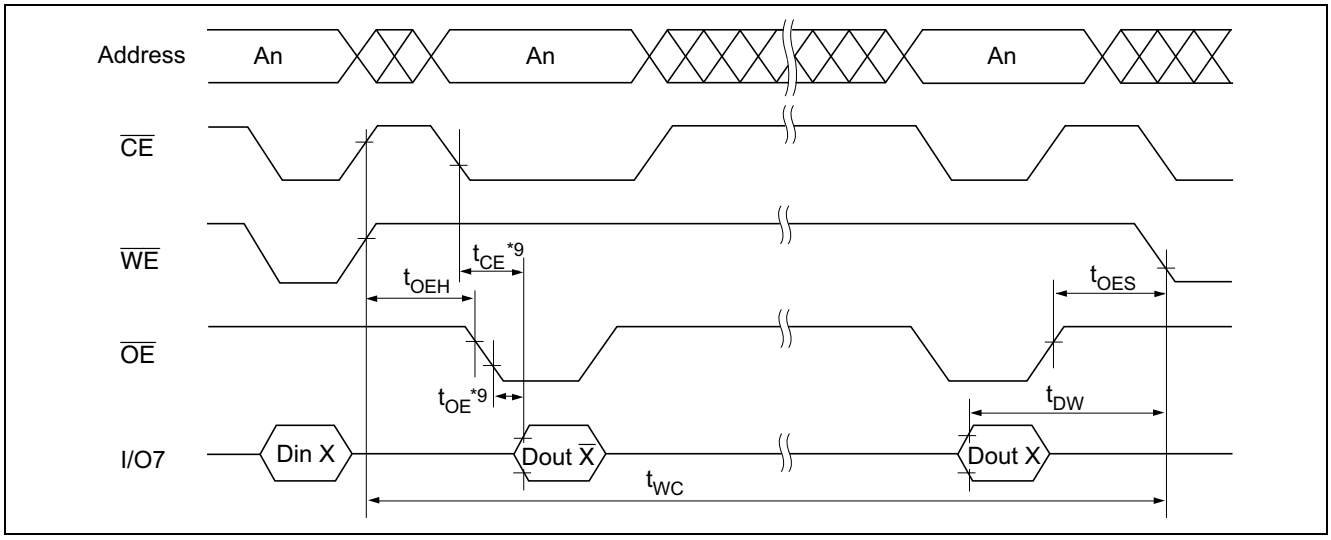
Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



$\overline{\text{Data}}$ Polling Timing Waveform

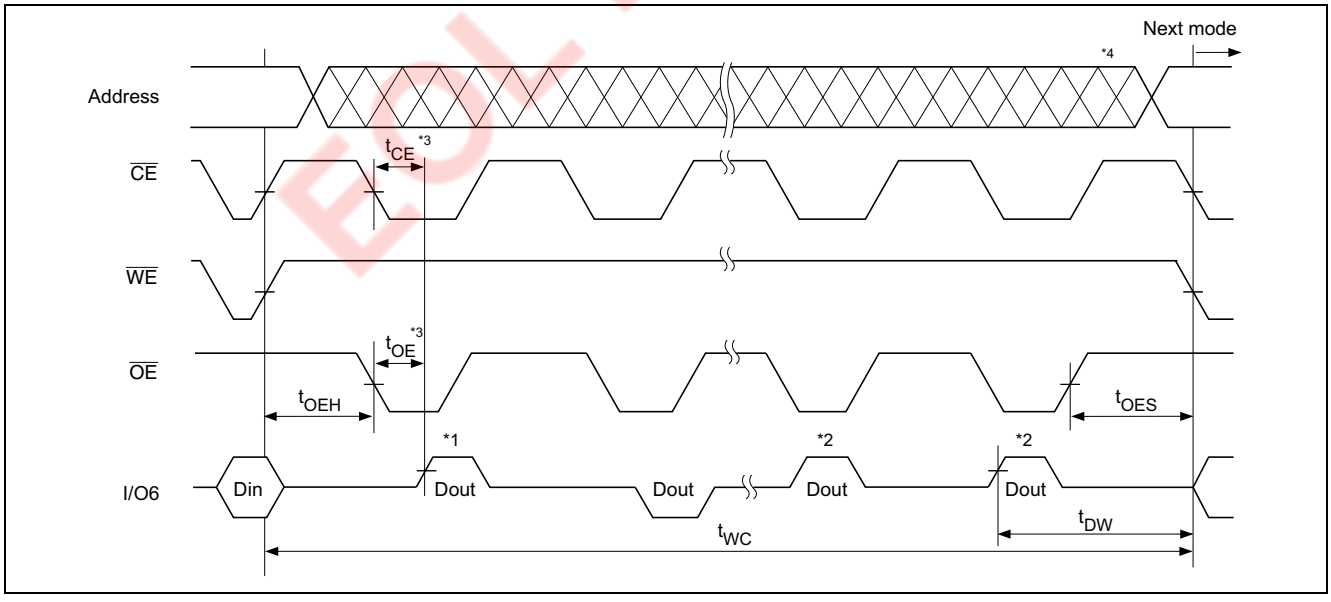


Toggle bit

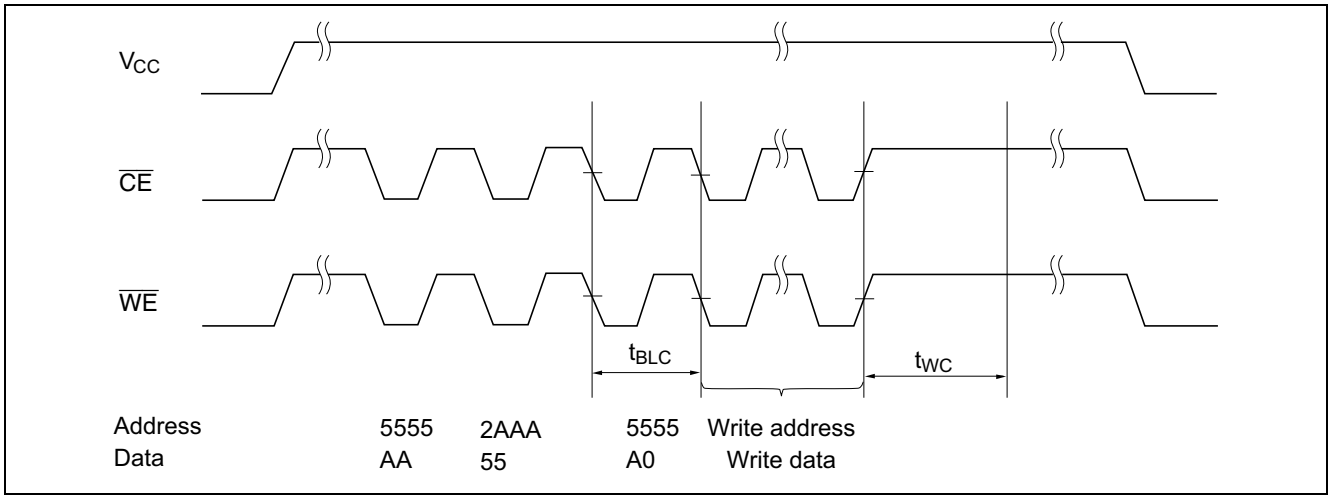
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle bit Waveform

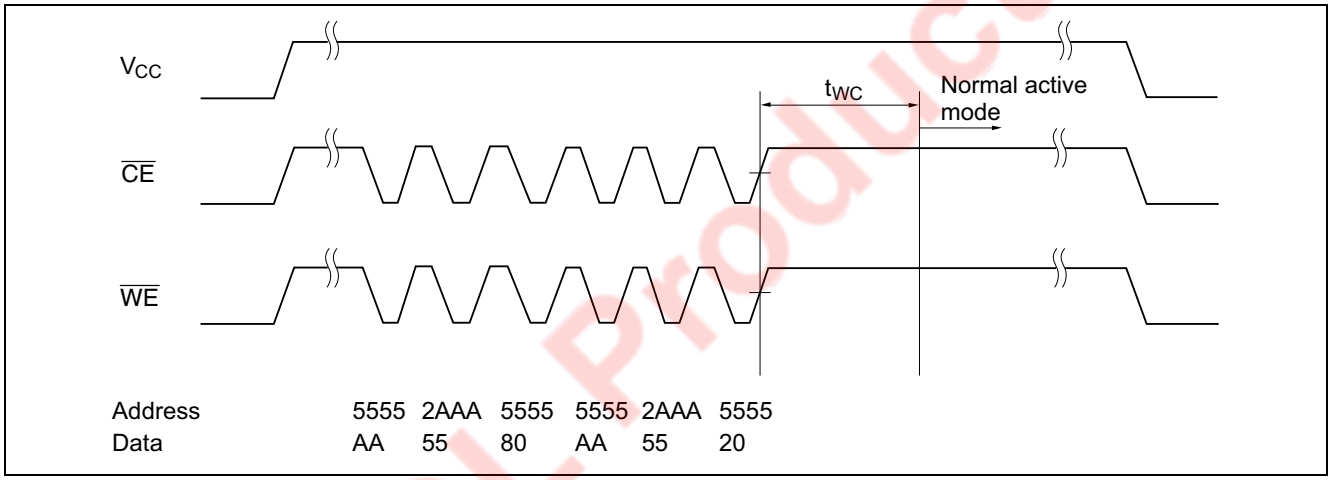
Notes: 1. I/O6 beginning state is "1".
2. I/O6 ending state will vary.
3. See AC read characteristics.
4. Any address location can be used, but the address must be fixed.



Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{Data}$ Polling

$\overline{Data}$ polling indicates the status that the EEPROM is in a write cycle or not. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data outputs from I/O7 to indicate that the EEPROM is performing a write operation.

$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

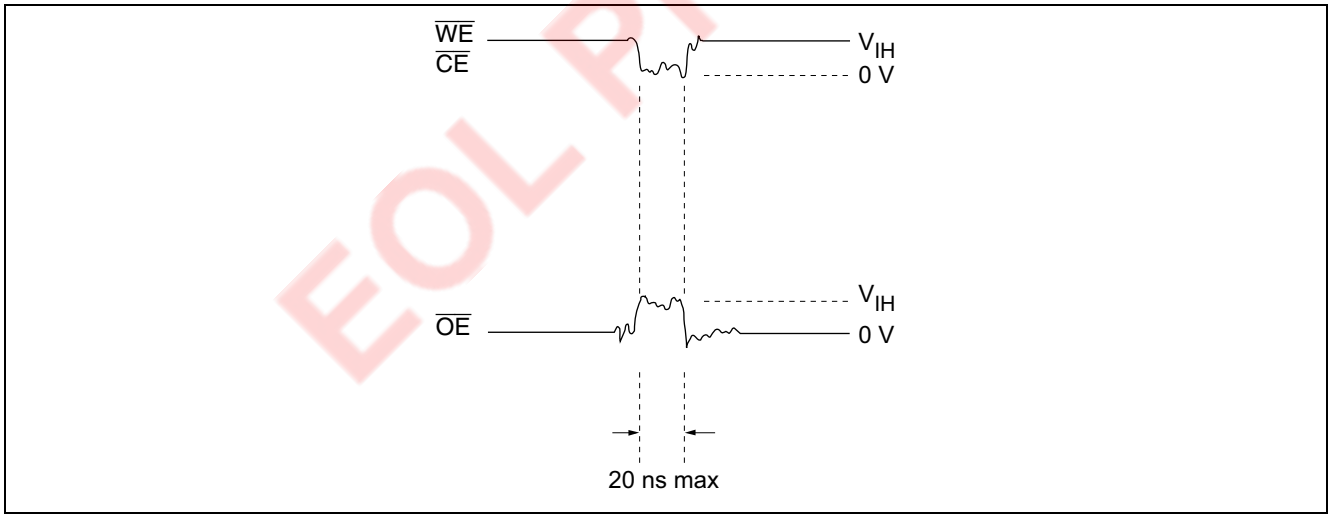
Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

Data Protection

To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less.

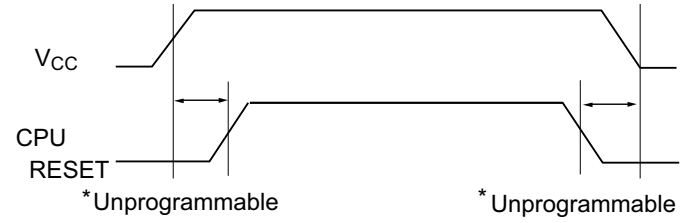
1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V_{CC} On/Off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

Note: The EEPROM shoud be kept in unprogrammable state during VCC on/off by using CPU RESET signal.



2.1 Protection by $\overline{CE}$, $\overline{OE}$, $\overline{WE}$

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	V_{CC}	×	×
$\overline{OE}$	×	V_{SS}	×
$\overline{WE}$	×	×	V_{CC}

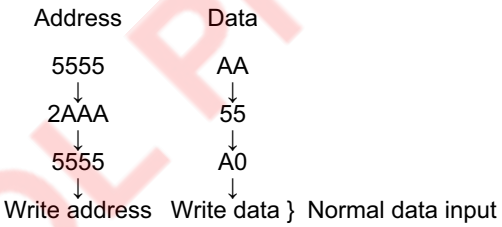
×: Don't care

V_{CC}: Pull-up to VCC level

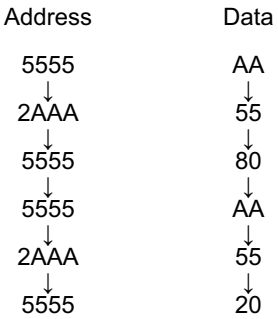
V_{SS}: Pull-down to VSS level

3. Software data protection

To prevent unintentional programming, this device has the software data protection (SDP) mode. The SDP is enabled by inputting the following 3 bytes code and write data. SDP is not enabled if only the 3 bytes code is input. To program data in the SDP enable mode, 3 bytes code must be input before write data.



The SDP mode is disabled by inputting the following 6 bytes code. Note that, if data is input in the SDP disable cycle, data can not be written.



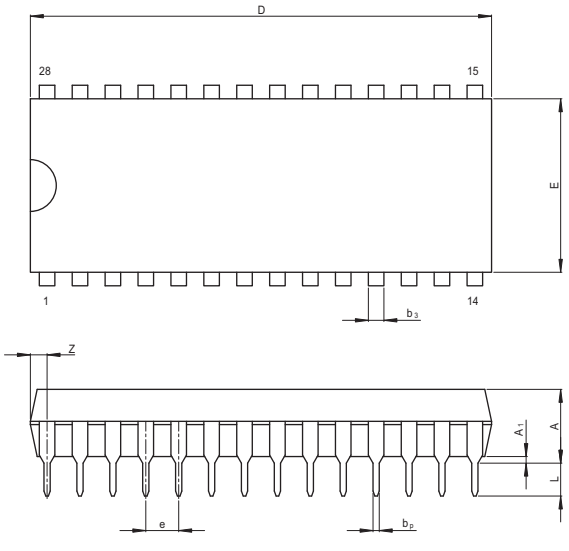
The software data protection is not enabled at the shipment.

Note: There are some differences between Renesas Electronics' and other company's for enable/disable sequence of software data protection. If there are any questions, please contact with Renesas Electronics' sales offices.

Package Dimensions

HN58C256API Series (PRDP0028AB-A / Previous Code: DP-28V)

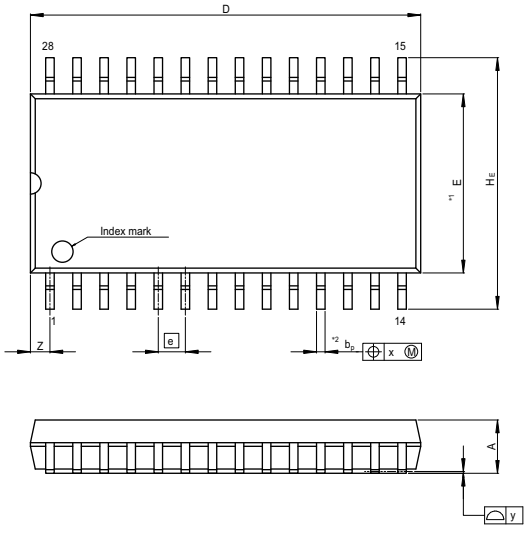
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP28-13.4x35.6-2.54	PRDP0028AB-A	DP-28/DP-28V	4.6g

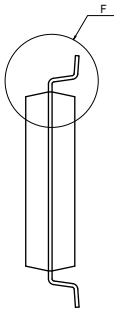


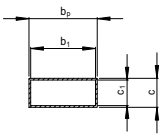
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	15.24	—
D	—	35.6	36.5
E	—	13.4	14.6
A	—	—	5.70
A_1	0.51	—	—
b_p	0.38	0.48	0.58
b_3	—	1.2	—
c	0.20	0.25	0.36
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.9
L	2.54	—	—

HN58C256AFPI Series (PRSP0028DC-A / Previous Code: FP-28DV)

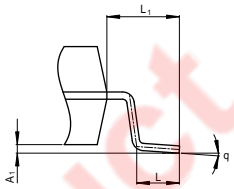
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP28-8.4x18.3-1.27	PRSP0028DC-A	FP-28D	0.7g







Terminal cross section



Detail F

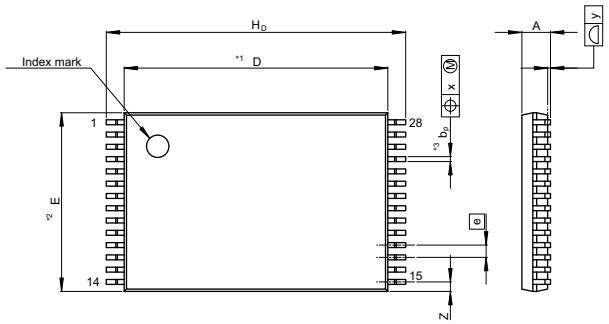
NOTE)
1. DIMENSION"*1"
DOES NOT INCLUDE MOLD FLASH.
2. DIMENSION"*2"DOES NOT
INCLUDE TRIM OFFSET.

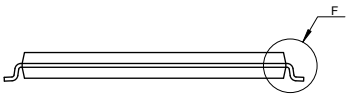
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	18.3	18.8
E	—	8.4	—
A_2	—	—	—
A_1	0.10	0.20	0.30
A	—	—	2.50
b_p	0.32	0.40	0.48
b_1	—	0.38	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
H_E	11.5	11.8	12.1
e	—	1.27	—
x	—	—	0.20
y	—	—	0.15
Z	—	—	1.12
L	0.8	1.0	1.2
L_1	—	1.7	—

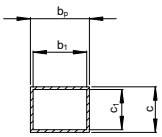
HN58C256ATI Series (PTSA0028ZB-A / Previous Code: TFP-28DBV)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSOP(1)28-8x11.8-0.55	PTSA0028ZB-A	TFP-28DB/TFP-28DBV	0.23g

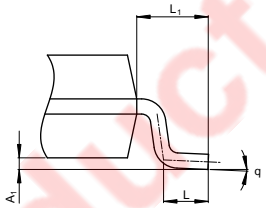
NOTE)
1. DIMENSION"*1"AND"*2(Nom)" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.







Terminal cross section



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	11.80	—
E	—	8.00	8.20
A_2	—	—	—
A_1	0.05	0.13	0.20
A	—	—	1.20
b_p	0.14	0.22	0.30
b_1	—	0.20	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	5°
H_D	13.10	13.40	13.70
e	—	0.55	—
x	—	—	0.10
y	—	—	0.10
Z	—	—	0.45
L	0.40	0.50	0.60
L_1	—	0.80	—

Revision History	HN58C256AI Series Data Sheet

Rev.	Date	Description	
		Page	Summary
Rev.1.00	Oct 07, 2013	—	Initial issue

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