

**HI-1818A**

Low Resistance, Single 8-Channel, CMOS Analog Multiplexer

FN3141  
Rev 4.00  
November 19, 2004

The HI-1818A is a monolithic, high performance CMOS analog multiplexer offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance. Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250Ω) assure optimum performance in low level or current mode applications.

The HI-1818A is a single-ended, 8-Channel multiplexer, and is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

**Features**

- Signal Range . . . . . +15V
- “ON” Resistance . . . . . 250Ω
- Input Leakage (Max) . . . . . .50nA
- Access Time . . . . . 350ns
- Power Consumption . . . . . .5mW
- DTL/TTL Compatible Address
- Operation . . . . . -55°C to 125°C

**Applications**

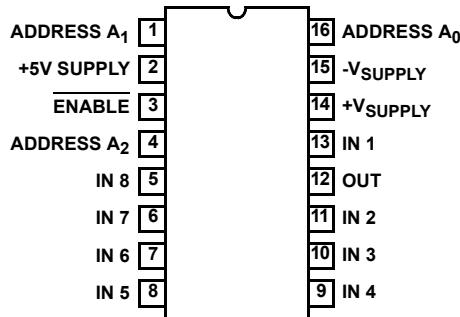
- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI1-1818A-2	-55 to 125	16 Ld CERDIP	F16.3

**Pinout**

HI-1818A (CERDIP)  
TOP VIEW



**Truth Table**

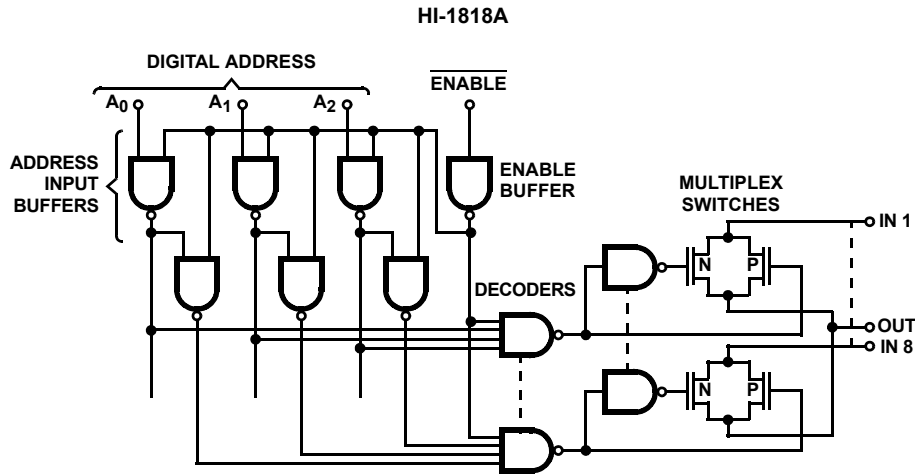
HI-1818A TRUTH TABLE

ADDRESS				"ON" CHANNEL
A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5

HI-1818A TRUTH TABLE

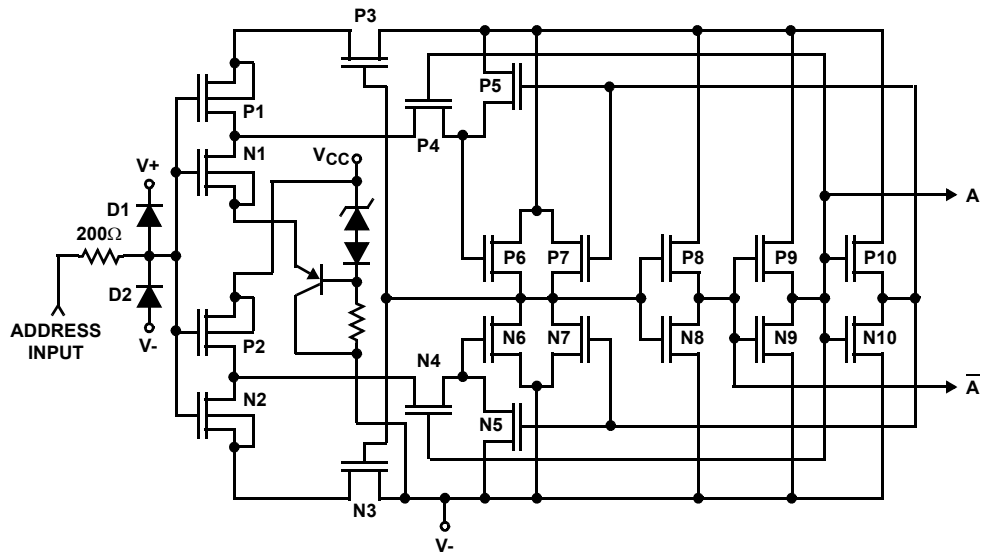
ADDRESS				"ON" CHANNEL
A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	None

**Functional Block Diagram**



**Schematic Diagrams**

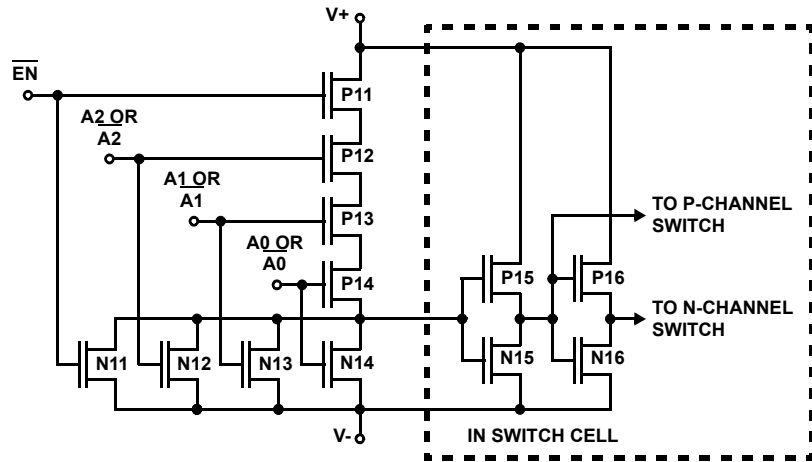
ADDRESS INPUT BUFFER



All N-Channel Bodies to V-  
All P-Channel Bodies to V+  
Unless Otherwise Specified

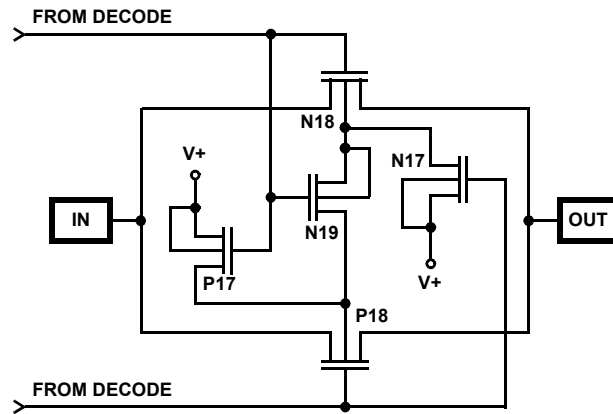
**Schematic Diagrams**

**ADDRESS DECODER**



All N-Channel Bodies to V-  
All P-Channel Bodies to V+

**MULTIPLEXER SWITCH**



All N-Channel Bodies to V-  
All P-Channel Bodies to V+  
Unless Otherwise Specified



**Electrical Specifications** Supplies = +15V, -15V, +5V;  $V_{AL} = 0.4V$ ,  $V_{AH} = 4.0V$ , Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY CHARACTERISTICS</b>						
Power Dissipation, $P_D$		Full	-	-	27.5	mW
Current, $I_+$		Full	-	-	0.5	mA
Current, $I_-$		Full	-	-	1	mA
Current, $I_L$		Full	-	-	1	mA

NOTES:

- $V_{OUT} = \pm 10V$ ,  $I_{OUT} = \mp 1mA$ .
- To drive from DTL/TTL circuits, 1k $\Omega$  pull-up resistors to 5.0V supply are recommended.
- Time measured to 90% of final output level;  $V_{OUT} = -5.0V$  to 5.0V, Digital Inputs = 0V to 4.0V.

**Test Circuits and Waveforms**

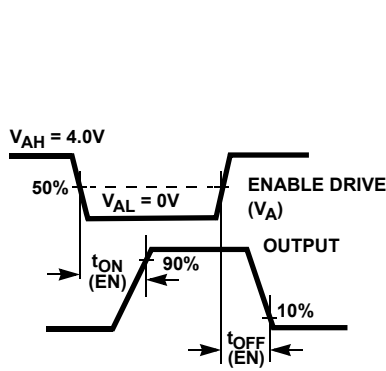


FIGURE 1A. MEASUREMENT POINTS

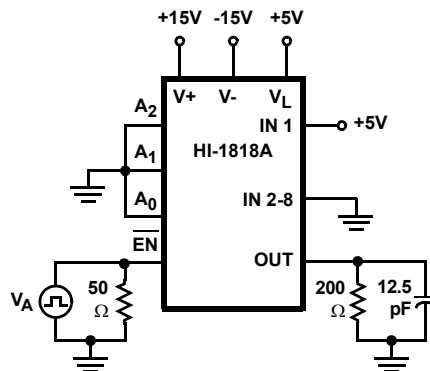


FIGURE 1B. TEST CIRCUIT

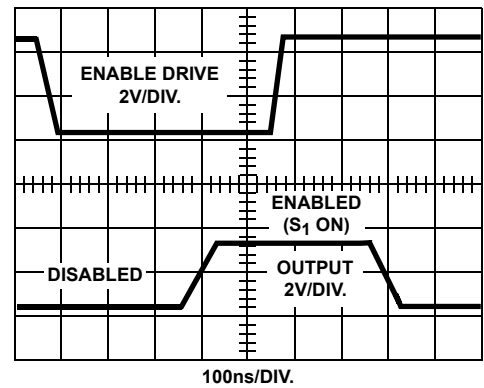


FIGURE 1C. WAVEFORMS

FIGURE 1. ENABLE DELAYS

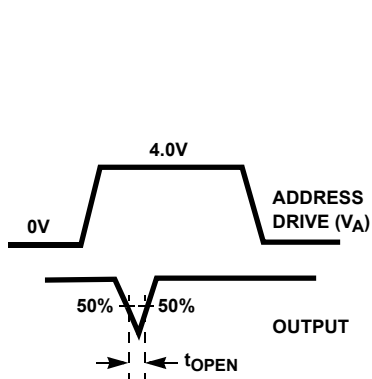


FIGURE 2A. MEASUREMENT POINTS

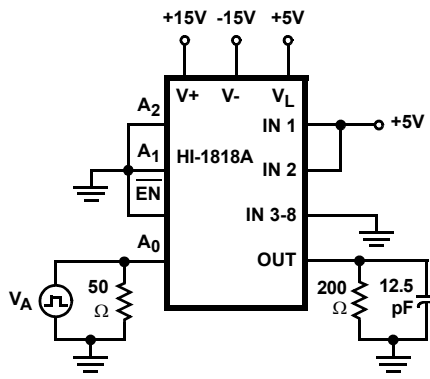


FIGURE 2B. TEST CIRCUIT

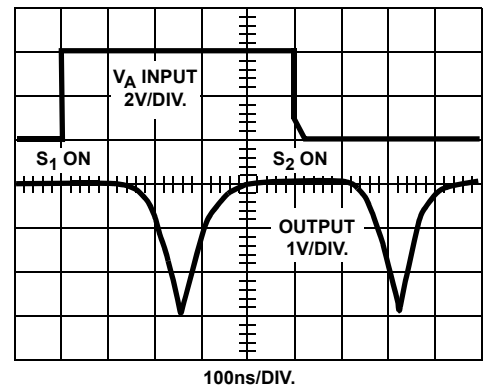


FIGURE 2C. WAVEFORMS

FIGURE 2. BREAK-BEFORE-MAKE DELAY

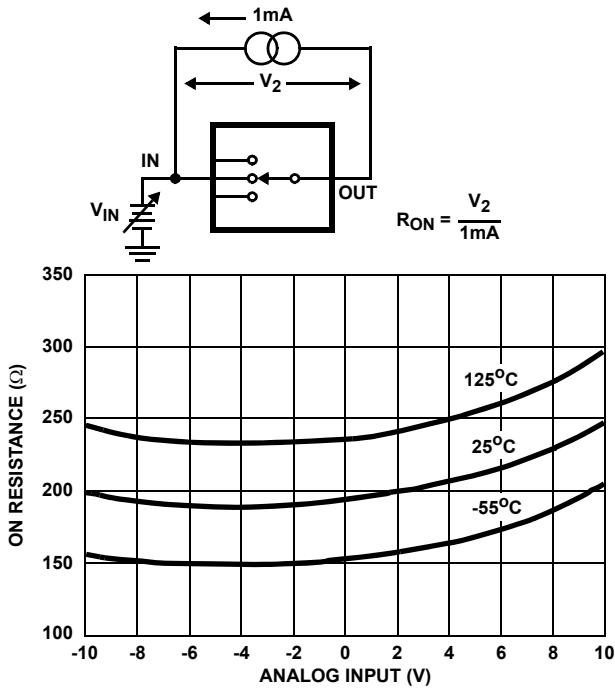


FIGURE 3. ON RESISTANCE vs ANALOG INPUT VOLTAGE

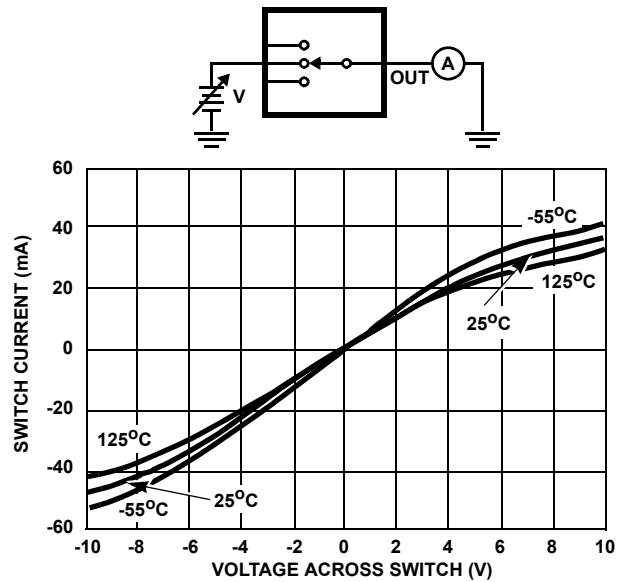
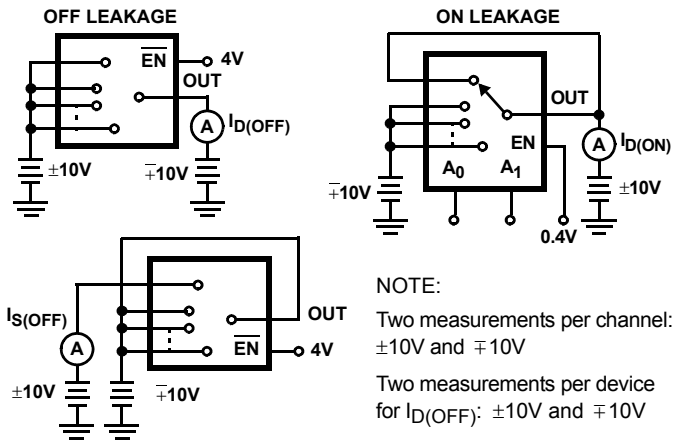


FIGURE 4. ON CHANNEL CURRENT vs VOLTAGE



NOTE:  
Two measurements per channel:  
±10V and ∓10V  
Two measurements per device  
for  $I_{D(OFF)}$ : ±10V and ∓10V

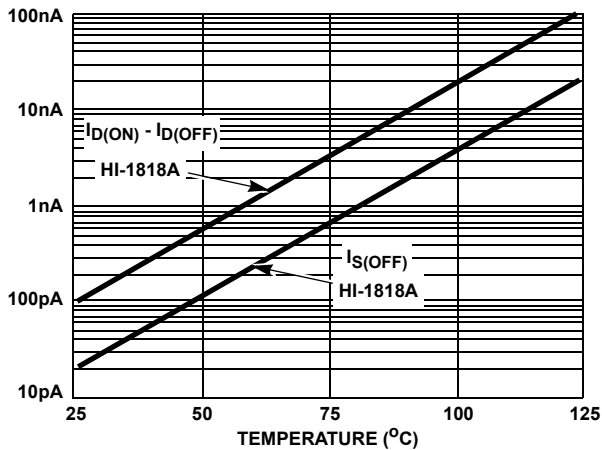


FIGURE 5. LEAKAGE CURRENTS vs TEMPERATURE

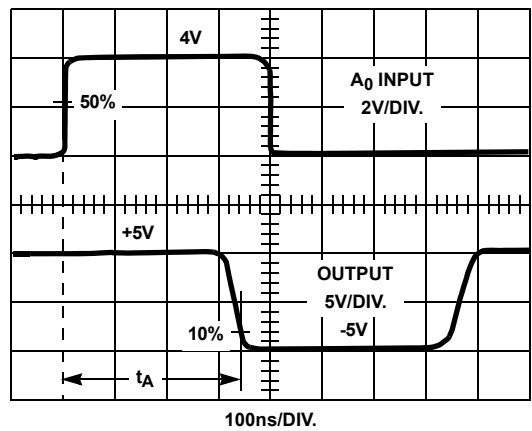
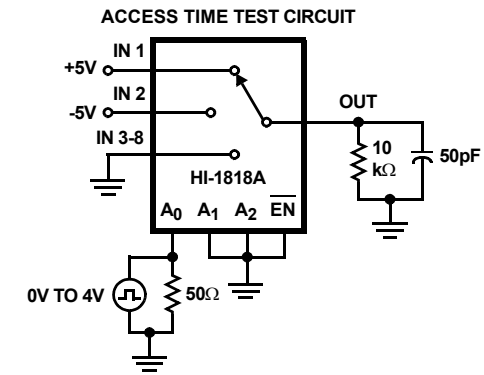


FIGURE 6. ACCESS TIME

## Die Characteristics

### METALLIZATION:

Type: CuAl  
Thickness:  $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

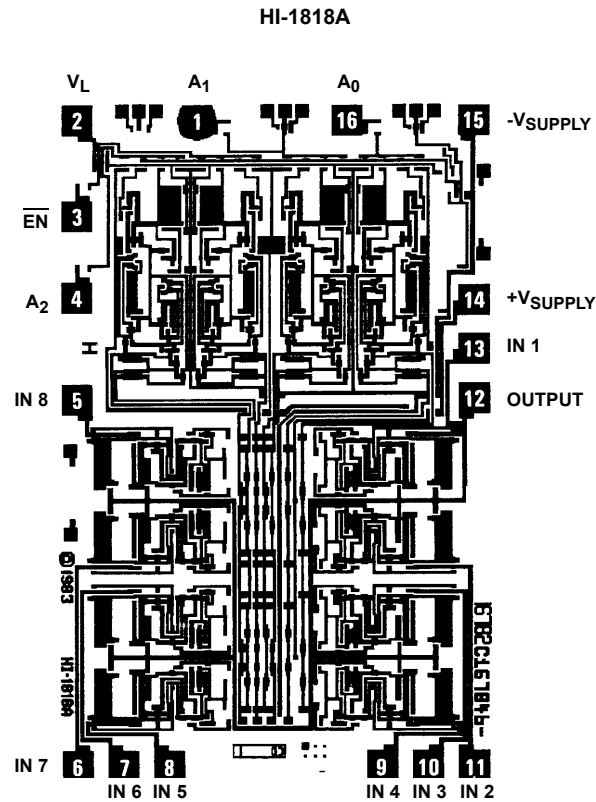
### PASSIVATION:

Type: Nitride/Silox  
Thickness: Silox:  $12\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$ , Nitride:  $3.5\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

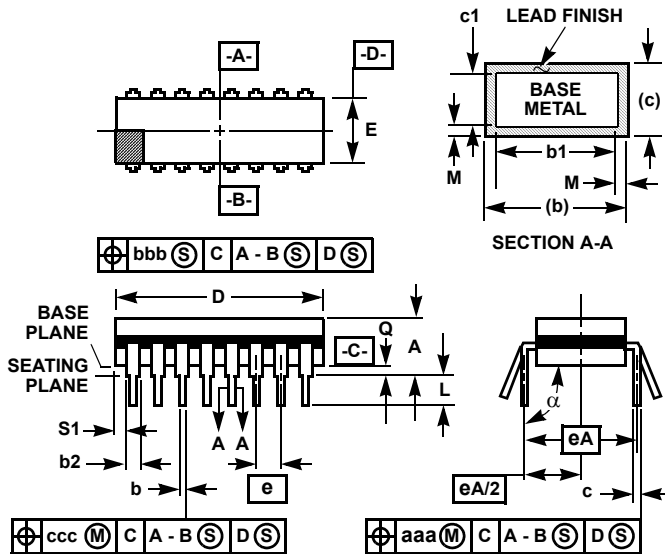
### WORST CASE CURRENT DENSITY:

$1.43 \times 10^5 \text{ A/cm}^2$  at 25mA

## Metallization Mask Layout



**Ceramic Dual-In-Line Frit Seal Packages (CERDIP)**



**F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)  
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
$\alpha$	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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