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April 1st, 2010
Renesas Electronics Corporation

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HAF2027(L), HAF2027(S)

Silicon N Channel Power MOS FET
Power Switching

REJ03G1674-0100

Rev.1.00

May 19, 2008

Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

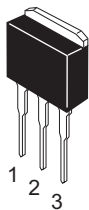
Features

- Logic level operation (4 V Gate drive)
- Built-in the over temperature shut-down circuit
- High endurance capability against to the shut-down circuit
- Latch type shut down operation (need 0 voltage recovery)

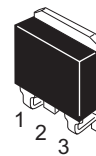
Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDKPAK (L))

RENESAS Package code: PRSS0004AE-B
(Package name: LDKPAK (S)-(1))

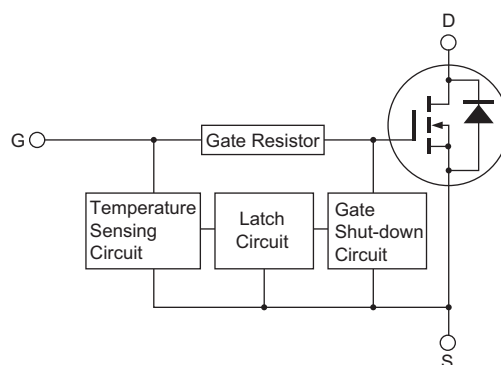


HAF2027(L)



HAF2027(S)

1. Gate
2. Drain (Flange)
3. Source



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	60	V
Gate to source voltage	V _{GSS}	16	V
Gate to source voltage	V _{GSS}	-2.5	V
Drain current	I _D	50	A
Drain peak current	I _D (pulse) ^{Note1}	100	A
Body-drain diode reverse drain current	I _{DR}	50	A
Channel dissipation	P _{ch} ^{Note2}	100	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10ms, duty cycle ≤ 1 %

2. Value at Tc = 25°C

Typical Operation Characteristics

(Ta=25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	3.5	—	—	V	
	V _{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I _{IH1}	—	—	100	μA	V _i = 6 V, V _{DS} = 0
	I _{IH2}	—	—	50	μA	V _i = 3.5 V, V _{DS} = 0
	I _{IL}	—	—	1	μA	V _i = 1.2 V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sd)1}	—	0.6	—	mA	V _i = 6 V, V _{DS} = 0
	I _{IH(sd)2}	—	0.35	—	mA	V _i = 3.5 V, V _{DS} = 0
Shut down temperature	T _{sd}	—	175	—	°C	Channel temperature
Gate operation voltage	V _{op}	3.5	—	12	V	

Electrical Characteristics

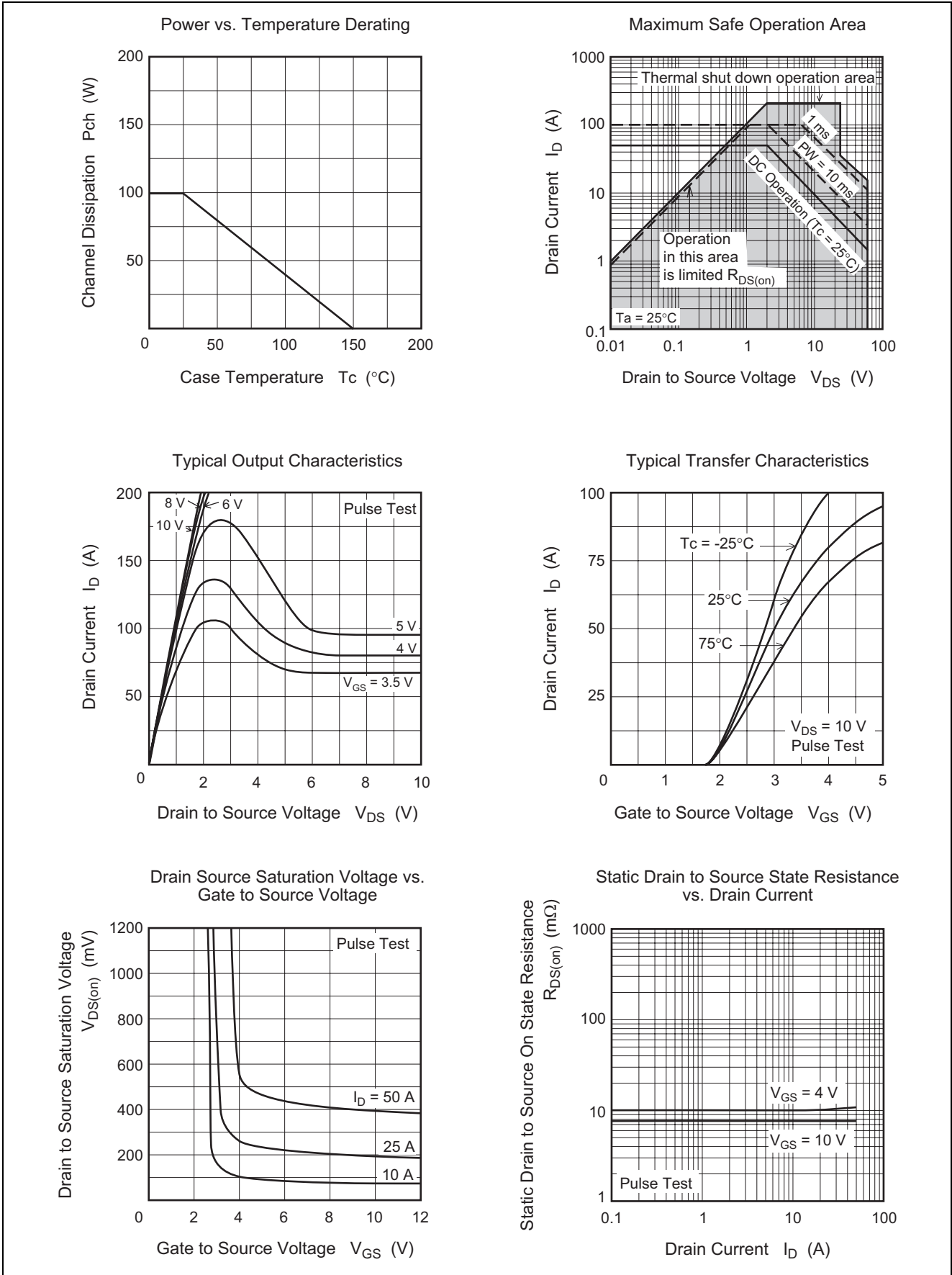
(Ta = 25°C)

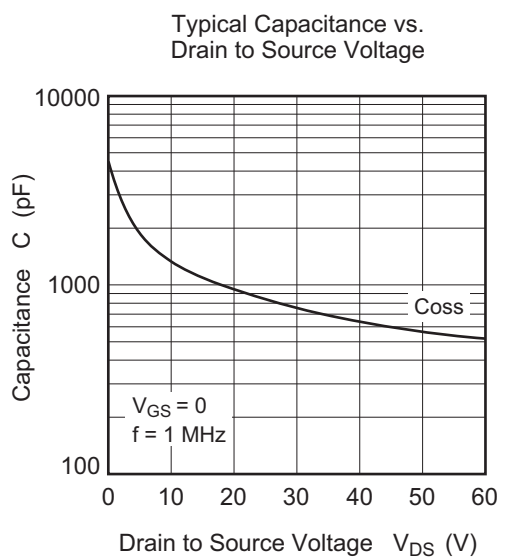
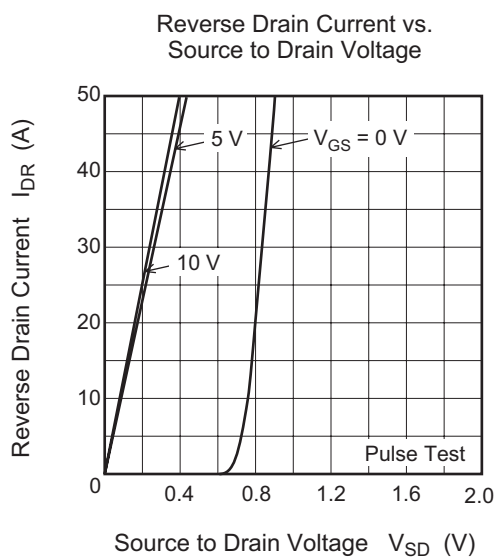
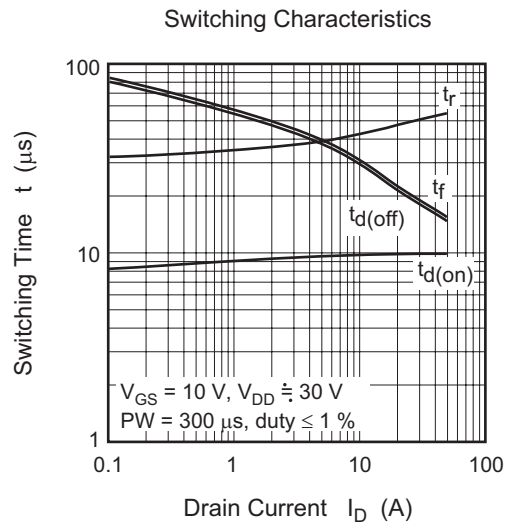
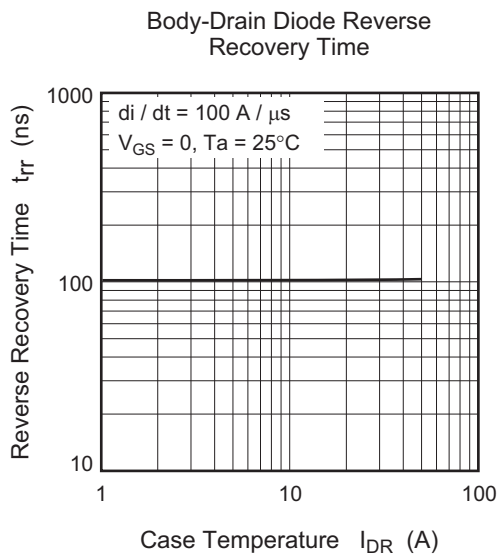
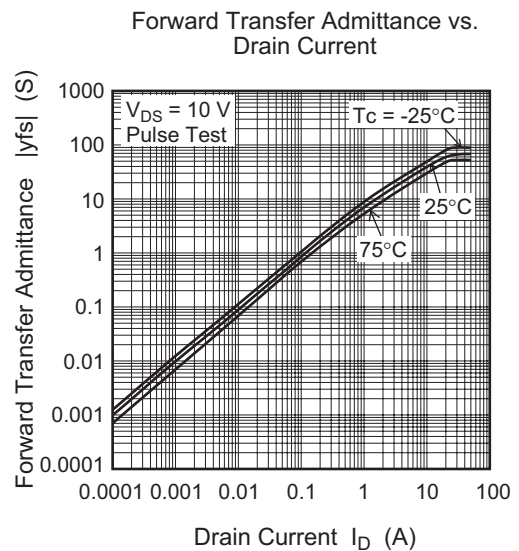
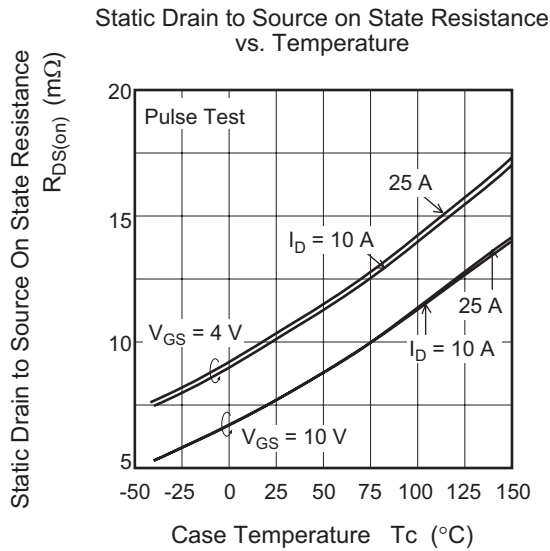
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I _{D1}	80	—	—	A	V _{GS} = 6 V, V _{DS} = 10 V ^{Note3}
	I _{D2}	15	—	—	A	V _{GS} = 3.5 V, V _{DS} = 10 V ^{Note3}
	I _{D3}	—	—	10	mA	V _{GS} = 1.2 V, V _{DS} = 10 V ^{Note3}
Drain to source breakdown voltage	V _{(BR)DSS}	60	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	16	—	—	V	I _G = 300 μA, V _{DS} = 0
	V _{(BR)GSS}	-2.5	—	—	V	I _G = -100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS1}	—	—	100	μA	V _{GS} = 6 V, V _{DS} = 0
	I _{GSS2}	—	—	50	μA	V _{GS} = 3.5 V, V _{DS} = 0
	I _{GSS3}	—	—	1	μA	V _{GS} = 1.2 V, V _{DS} = 0
	I _{GSS4}	—	—	-100	μA	V _{GS} = -2.4 V, V _{DS} = 0
Input current (shut down)	I _{GS(OP)1}	—	0.6	—	mA	V _{GS} = 6 V, V _{DS} = 0
	I _{GS(OP)2}	—	0.35	—	mA	V _{GS} = 3.5 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	10	μA	V _{DS} = 60 V, V _{GS} = 0
Gate to source cut off voltage	V _{GS(off)}	1.0	—	2.25	V	V _{DS} = 10 V, I _D = 1 mA
Forward transfer admittance	y _{fs}	15	65	—	S	I _D = 25 A, V _{DS} = 10 V ^{Note3}
Static drain to source on state resistance	R _{DS(on)}	—	7.7	10	mΩ	I _D = 25 A, V _{GS} = 10 V ^{Note3}
	R _{DS(on)}	—	10.3	15	mΩ	I _D = 25 A, V _{GS} = 4 V ^{Note3}
Output capacitance	C _{oss}	—	1423	—	pF	V _{DS} = 10 V, V _{GS} = 0, f = 1MHz
Turn-on delay time	t _{d(on)}	—	10	—	μs	V _{GS} = 10 V, I _D = 25 A, R _L = 1.2 Ω
Rise time	t _r	—	48	—	μs	
Turn off delay time	t _{d(off)}	—	22	—	μs	
Fall time	t _f	—	23	—	μs	
Body-drain diode forward voltage	V _{DF}	—	0.9	—	V	I _F = 50 A, V _{GS} = 0
Body-drain diode reverse recovery time	t _{rr}	—	102	—	ns	I _F = 50 A, V _{GS} = 0, di _F /dt = 100 A/μs
Over load shut down operation time ^{Note4}	t _{os1}	—	0.7	—	ms	V _{GS} = 5 V, V _{DD} = 16 V
	t _{os2}	—	0.43	—	ms	V _{GS} = 5 V, V _{DD} = 24 V

Notes: 3. Pulse test

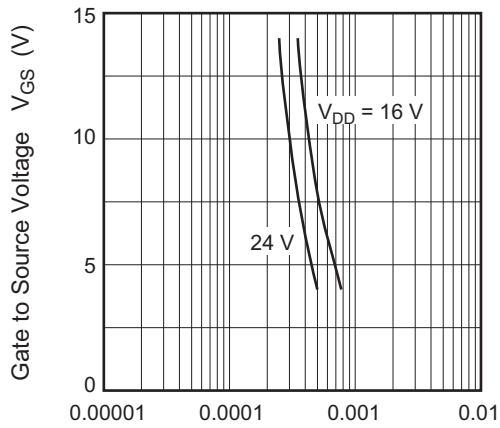
4. Including the junction temperature rise of the over loded condition.

Main Characteristics



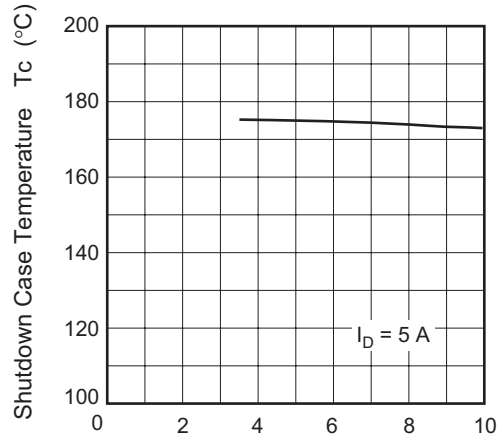


Gate to Source Voltage vs. Shutdown Time of Load-Short Test



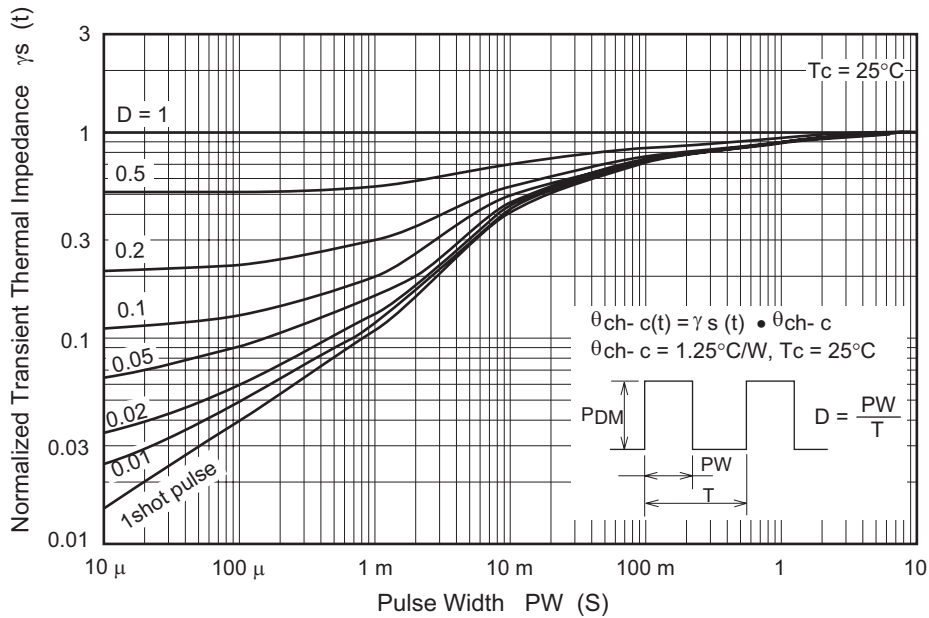
Shutdown Time of Load-Short Test Pw (S)

Shutdown Case Temperature vs. Gate to Source Voltage

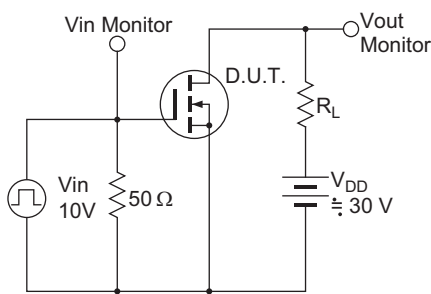


Gate to Source Voltage VGS (V)

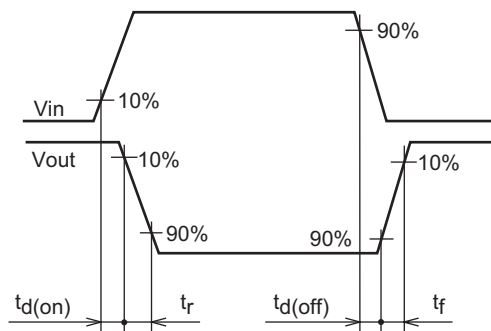
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



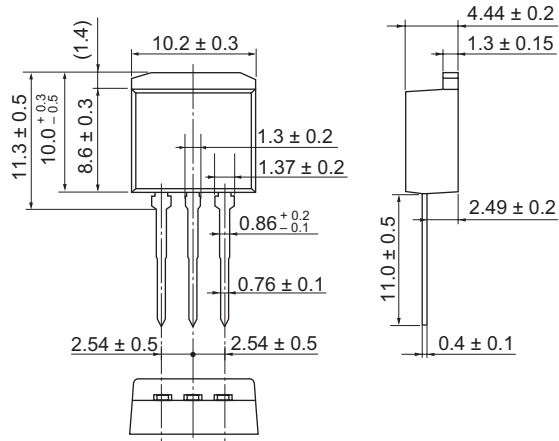
Waveform



Package Dimensions

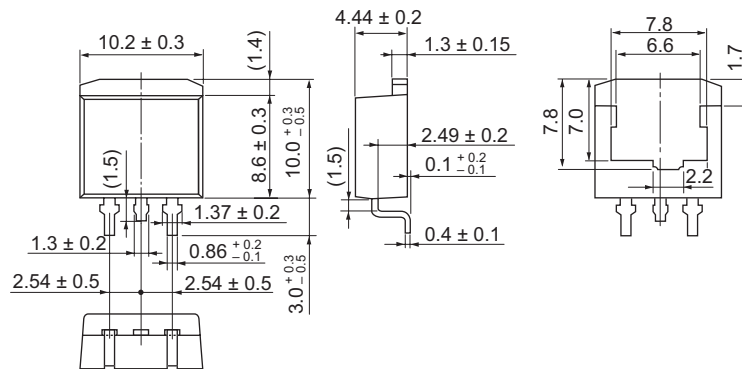
Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBPAK(L)	—	PRSS0004AE-A	LDBPAK(L) / LDBPAK(L)V	1.40g

Unit: mm



Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBPAK(S)-(1)	SC-83	PRSS0004AE-B	LDBPAK(S)-(1) / LDBPAK(S)-(1)V	1.30g

Unit: mm



Ordering Information

Part No.	Quantity	Shipping Container
HAF2027-90STL-E	1000 pcs/Reel	Taping (Reel)
HAF2027-90STR-E	1000 pcs/Reel	Taping (Reel)

Notes:

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