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Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
for new design

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FS7VS-12A

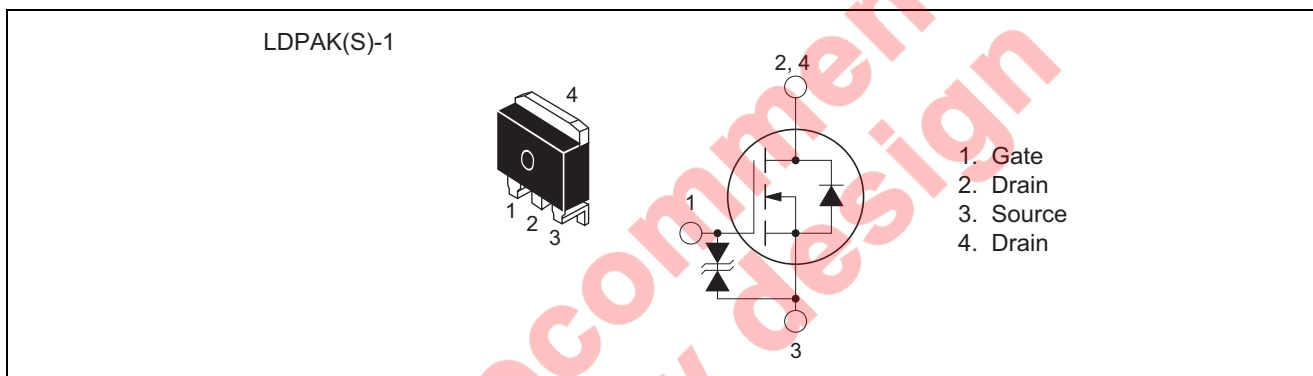
High-Speed Switching Use
Nch Power MOS FET

REJ03G0271-0100
Under development
Rev.1.00
Aug.20.2004

Features

- Drive voltage : 10 V
- V_{DSS} : 600 V
- $r_{DS(ON)(max)}$: 1.3 Ω
- I_D : 7 A

Outline



Applications

SMPS, lamp ballast, etc.

Maximum Ratings

($T_c = 25^\circ\text{C}$)

Parameter	Symbol	Ratings	Unit	Conditions
Drain-source voltage	V_{DSS}	600	V	$V_{GS} = 0\text{ V}$
Gate-source voltage	V_{GSS}	± 30	V	$V_{DS} = 0\text{ V}$
Drain current	I_D	7	A	
Drain current (Pulsed)	I_{DM}	21	A	
Avalanche current (Pulsed)	I_{DA}	7	A	$L = 200\ \mu\text{H}$
Maximum power dissipation	P_D	100	W	
Channel temperature	T_{ch}	- 55 to +150	$^\circ\text{C}$	
Storage temperature	T_{stg}	- 55 to +150	$^\circ\text{C}$	
Mass	—	1.2	g	Typical value

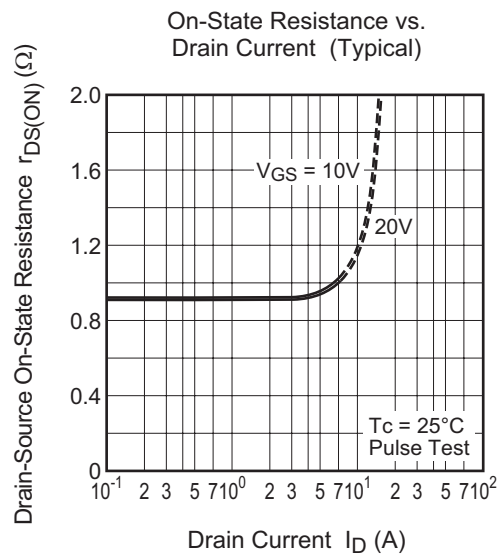
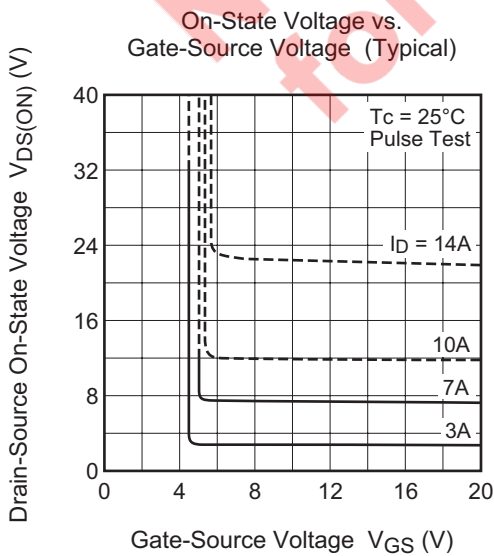
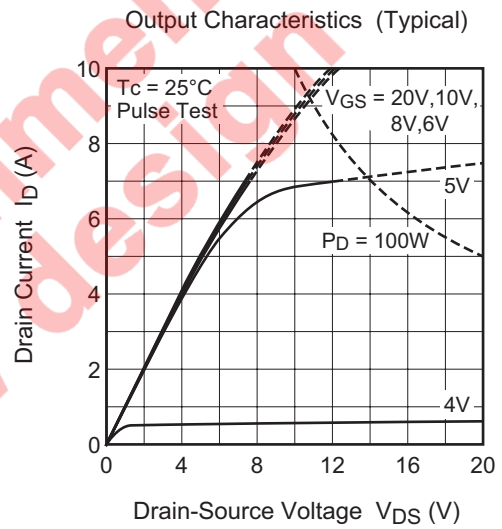
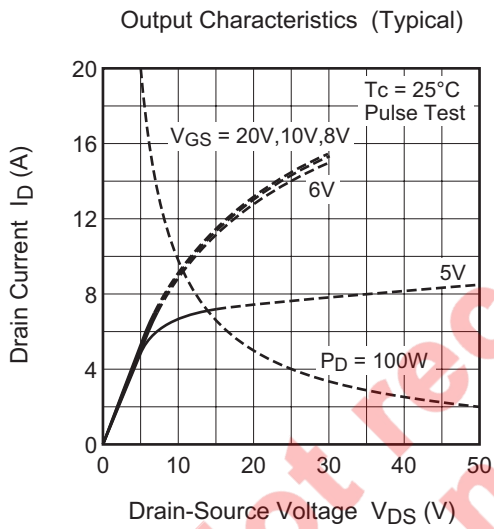
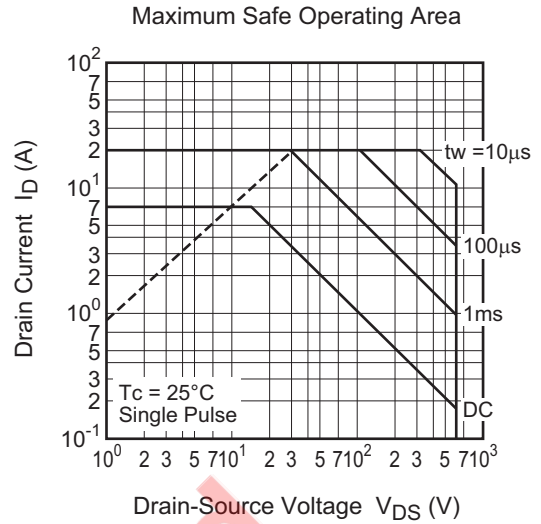
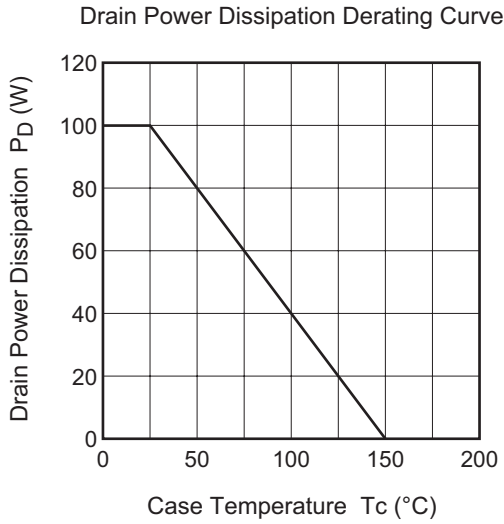
Electrical Characteristics

(T_{ch} = 25°C)

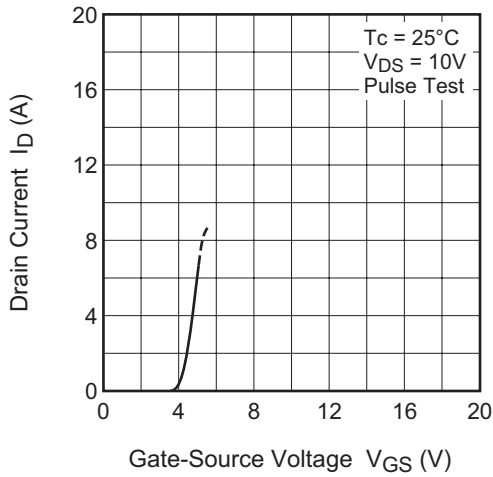
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	—	—	V	$I_D = 1 \text{ mA}$, $V_{GS} = 0 \text{ V}$
Gate-source breakdown voltage	$V_{(BR)GSS}$	± 30	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0 \text{ V}$
Gate-source leakage current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 25 \text{ V}$, $V_{DS} = 0 \text{ V}$
Drain-source leakage current	I_{DSS}	—	—	1	mA	$V_{DS} = 600 \text{ V}$, $V_{GS} = 0 \text{ V}$
Gate-source threshold voltage	$V_{GS(th)}$	2.5	3.0	3.5	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$
Drain-source on-state resistance	$r_{DS(ON)}$	—	1.0	1.3	Ω	$I_D = 3 \text{ A}$, $V_{GS} = 10 \text{ V}$
Drain-source on-state voltage	$V_{DS(ON)}$	—	3.0	3.9	V	$I_D = 3 \text{ A}$, $V_{GS} = 10 \text{ V}$
Forward transfer admittance	$ y_{fs} $	4.2	7.0	—	S	$I_D = 3 \text{ A}$, $V_{DS} = 10 \text{ V}$
Input capacitance	C_{iss}	—	1100	—	pF	$V_{DS} = 25 \text{ V}$, $V_{GS} = 10 \text{ V}$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	100	—	pF	
Reverse transfer capacitance	C_{rss}	—	25	—	pF	
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{DD} = 200 \text{ V}$, $I_D = 3 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_{GEN} = R_{GS} = 50 \text{ }\Omega$
Rise time	t_r	—	25	—	ns	
Turn-off delay time	$t_{d(off)}$	—	150	—	ns	
Fall time	t_f	—	35	—	ns	
Source-drain voltage	V_{SD}	—	1.5	2.0	V	$I_S = 3 \text{ A}$, $V_{GS} = 0 \text{ V}$
Thermal resistance	$R_{th(ch-c)}$	—	—	1.25	$^{\circ}\text{C/W}$	Channel to case

Not recommended
for new designs

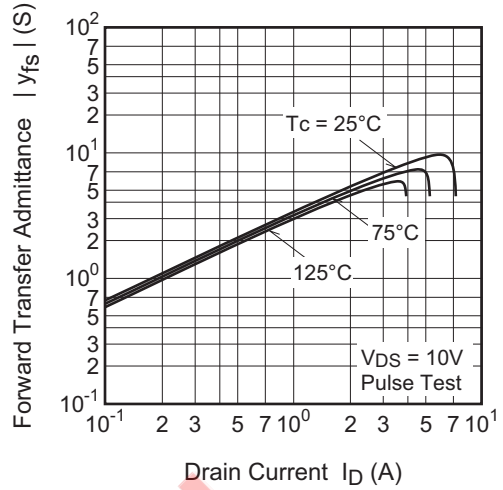
Performance Curves



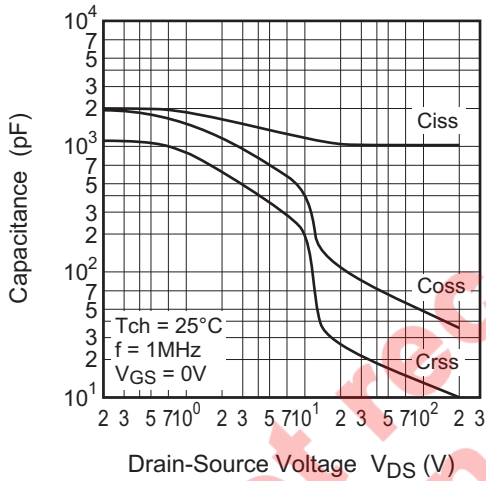
Transfer Characteristics (Typical)



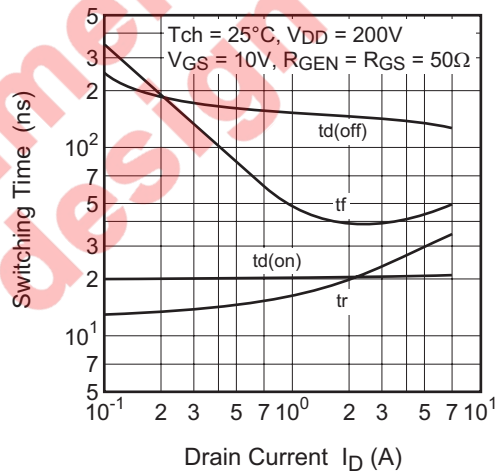
Forward Transfer Admittance vs. Drain Current (Typical)



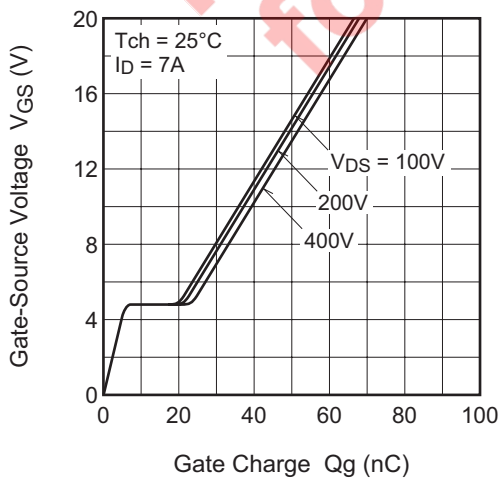
Capacitance vs. Drain-Source Voltage (Typical)



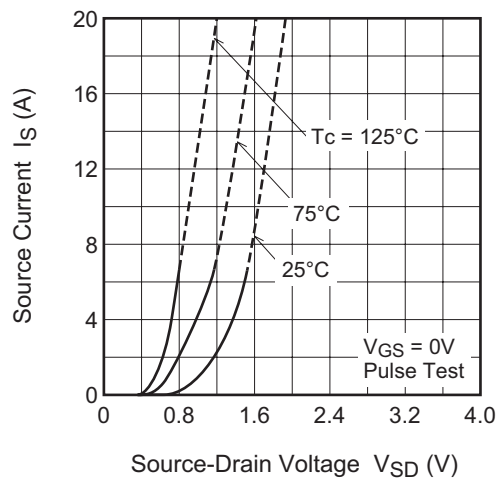
Switching Characteristics (Typical)

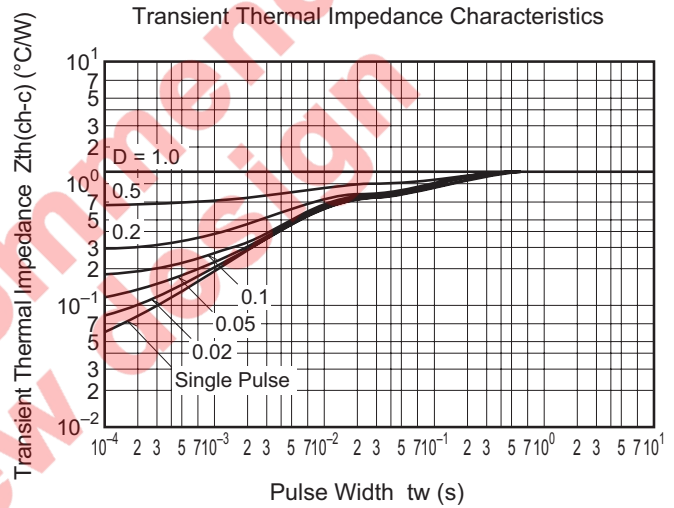
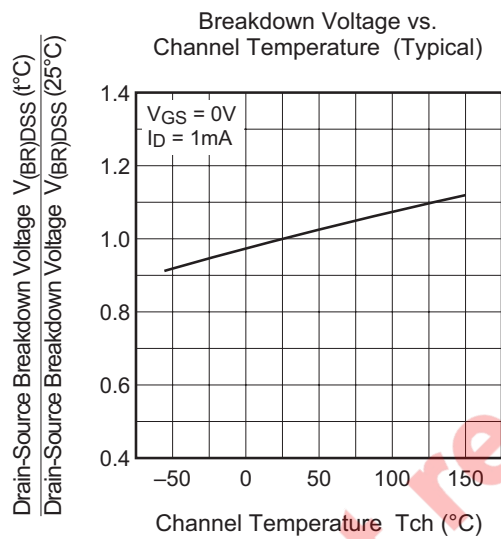
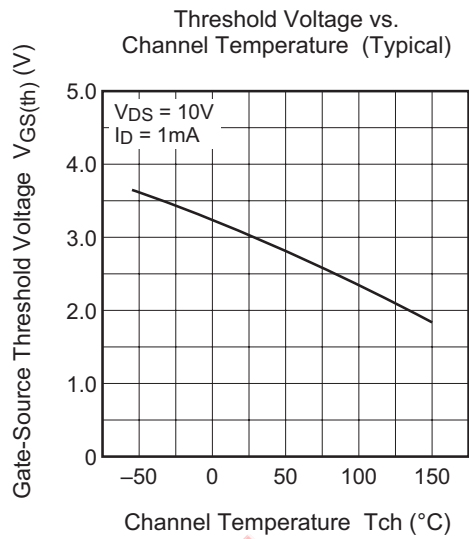
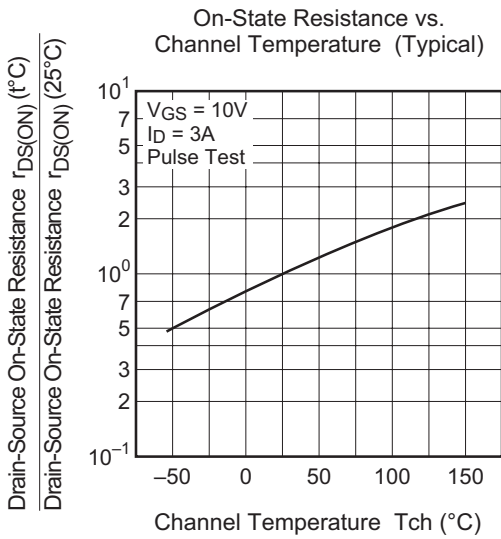


Gate-Source Voltage vs. Gate Charge (Typical)

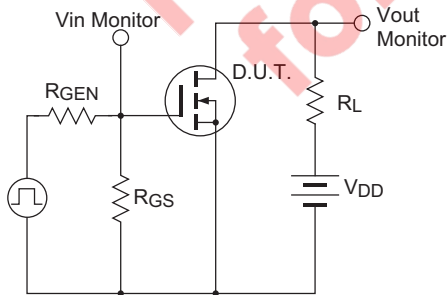


Source-Drain Diode Forward Characteristics (Typical)

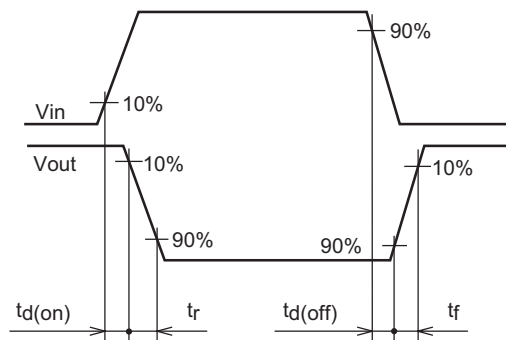




Switching Time Measurement Circuit

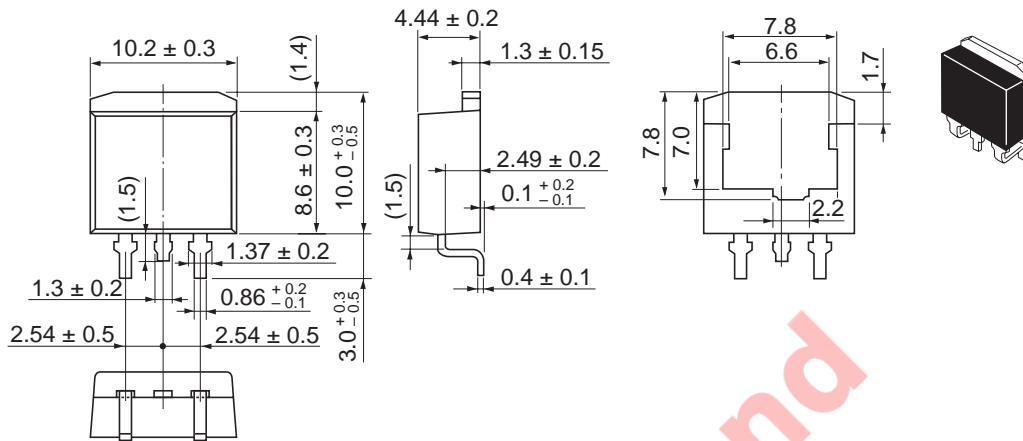


Switching Waveform



Package Dimensions

As of January, 2003
Unit: mm



Package Code	LDBAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.30 g

Order Code

Lead form	Standard packing	Quantity	Standard order code	Standard order code example
Surface-mounted type	Taping	1000	Type name – T +Direction (1 or 2) +1	FS7VS-12A-T11

Note : Please confirm the specification about the shipping in detail.

Not recommended for new design

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