EC-1

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150 MHz, MCU with Arm® Cortex®-R4, on-chip FPU, 249 DMIPS, EtherCAT, USB 2.0 high-speed, CAN, various communications interfaces such as an SPI multi-I/O bus controller, and safety functions

Features

■ On-chip 32-bit Arm Cortex-R4 processor

- High-speed realtime control with maximum operating frequency of 150 MHz
  Capable of 249 DMIPS
- On-chip 32-bit Arm Cortex-R4 (revision r1p4)
- Tightly coupled memory (TCM) with ECC: 512 Kbytes/32 Kbytes
- Instruction cache/data cache with ECC: 8 Kbytes per cache
- High-speed interrupt
- The FPU supports addition, subtraction, multiplication, division, multiply-and-accumulate, and square-root operations at single-precision and double-precision.
- Harvard architecture with 8-stage pipeline
- Supports the memory protection unit (MPU)
- Arm CoreSight architecture, includes support for debugging through JTAG and SWD interfaces

■ Low power consumption

- Standby mode, and module stop function

■ Data transfer

- DMACAa: 16 channels × 2 units

■ Event link controller

- Module operations can be started by event signals rather than by interrupt handlers.
- Linked operation of modules is available even while the CPU is in the sleep state.

■ Reset and power supply voltage control

- Three reset sources including a pin reset
- Dual power-voltage configuration: 3.3 V (I/O unit), 1.2 V (internal)

■ Clock functions

- Oscillator input frequency: 25 MHz
- CPU clock frequency: 150 MHz
- Low-speed on-chip oscillator (LOCO): 240 kHz

■ Independent watchdog timer

- Operated by a clock signal obtained by frequency-dividing the clock signal from the low-speed on-chip oscillator: Up to 120 kHz

■ Safety functions

- Register write protection, input clock oscillation stop detection, CRC, and IWDTa
- An error control module is incorporated to generate a pin signal output, interrupt, or internal reset in response to errors originating in the various modules.

PLBG0196GA-B 12x12mm, 0.8-mm pitch

■ Various communications interfaces

- EtherCAT slave controller: 2 ports
- USB 2.0 high-speed host/function : 1 channel
- CAN (compliant with ISO11898-1): 1 channel
- SCIFA with 16-byte transmission and reception FIFOs: 5 channels
- I^2C bus interface: 1 channel for transfer at up to 400 kbps
- RSPIa: 2 channels
- SPIBSC: Provides a single interface for multi-I/O compatible serial flash memory

■ 8 extended-function timers

- 16-bit CMT (6 channels), 32-bit CMTW (2 channels)

■ General-purpose I/O ports

- 5-V tolerance, open drain, input pull-up

■ Multi-function pin controller

- The locations of input/output functions for peripheral modules are selectable from among multiple pins.

■ Operating temperature range*1

- Tj = -40°C to +125°C
  Tj: Junction temperature

Note 1. When the operating temperature (junction temperature) is 110°C or higher, refer to the precautions regarding the high-temperature operation on the EC-1 (R01AN3998).

1. Overview

1.1 Outline of Specifications

This LSI circuit is a high-performance industrial MCU equipped with the Arm® Cortex®-R4 processor with FPU, and incorporating integrated peripheral functions necessary for system configuration. Table 1.1 lists the specifications in outline, and Table 1.2 gives a list of functions.

Table 1.1 Outline of Specifications (1 / 3)

Classification	Module/Function	Description
CPU	Central processing unit (Cortex-R4)	• Operating frequency 196-pin FBGA:150 MHz • 32-bit CPU Cortex-R4 designed by Arm (core revision r1p4) • Address space: 4 Gbytes • Instruction cache: 8 Kbytes (with ECC) • Data cache: 8 Kbytes (with ECC) • Tightly coupled memory (TCM) ATCM: 512 Kbytes (with ECC) BTCM: 32 Kbytes (with ECC) • Instruction set: Arm v7-R architecture, so support includes Thumb® and Thumb-2 • Data arrangement Instructions: Little endian Data: Little endian • Memory protection unit (MPU)
	FPU (Cortex-R4)	• Supports addition, subtraction, multiplication, division, multiply-and-accumulate, and square-root operations at single- and double-precision. • Registers 32-bit single-word registers: 32 bits × 32 (can be used as 16 double-word registers: 64 bits × 16)
Operating modes		• SPI boot mode (for booting up from serial flash memory)
Clock	Clock generation circuit	• The input clock can be selected from an external resonator. • Detection of input clock oscillation stopping • The following clocks are generated. CPU clock:150 MHz (fixed) System clock: 150 MHz (fixed) High-speed peripheral module clock: 150 MHz (fixed) Low-speed peripheral module clock: 75 MHz (fixed) Low-speed on-chip oscillator: 240 kHz (fixed)
Reset		RES# pin reset, error control module (ECM) reset, software reset
Low power	Low power consumption	• Standby mode (Cortex-R4) • Module stop function
Interrupt	Cortex-R4 vector interrupt controller (VIC)	• Peripheral function interrupts: 87 • External interrupts: 15 sources (NMI, IRQ0 to IRQ4, IRQ6, IRQ7, IRQ9, IRQ11 to IRQ14, ETH0_INT, ETH1_INT) • Non-maskable interrupts: 2 sources • Sixteen levels specifiable for the order of priority
Data transfer	Direct memory access controller (DMACAa)	• 2 units (16 channels for unit 0, 16 channels for unit 1) • Transfer modes: Single transfer mode and block transfer mode • Transfer size Unit 0: 1/2/4/16/32/64 bytes Unit 1: 1/2/4/16 bytes • Activation sources: External interrupts, on-chip peripheral module requests, and software requests
I/O ports	General-purpose I/O ports	• 196-pin FBGA I/O pins: 115 Input pins: 8 Pull-up/pull-down resistors: 115 5-V tolerance: 5
Event link controller (ELC)		• Event signals can be interlinked with the operation of modules. • In particular, the operation of timer modules can be started by input event signals. • Event-linked operation of signals of ports B and E is to be possible.

Table 1.1 Outline of Specifications (2 / 3)

Classification	Module/Function	Description
Multi-function pin controller (MPC)		The locations of input/output functions are selectable from among multiple pins.
Timer	Compare match timer (CMT)	• (16 bits × 2 channels) × 3 units • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 75 MHz) • Event linking by the ELC (channel 1 of unit 0 only)
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 75 MHz) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Digital noise filter function for signals on the input capture pins • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among six counter-input clock signals for each channel (with maximum operating frequency of 75 MHz)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: Low-speed on-chip oscillator (LOCO)/2 Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 (with maximum operating frequency of 120 kHz)
Communication function	EtherCAT Slave Controller (ESC)*1	• 1 channel (2 ports) • EtherCAT Slave Controller IP core (made by Beckhoff Automation GmbH) implemented
	USB 2.0 HS host/ function module	• 1 port • Compliance with the USB 2.0 specification • Transfer rate High speed (480 Mbps), full speed (12 Mbps) • Communications buffer Incorporates 1 Kbyte of RAM for host mode Incorporates 8 Kbytes of RAM for function mode
	Serial communication interface with FIFO (SCIFA)	• 5 channels • Serial communications modes: Asynchronous, clock synchronous*2 • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Both the transmission and reception sections are equipped with 16-byte FIFO buffers, allowing continuous transmission and reception. • Bit rate modulation
	I^2C bus interface (RIICa)	• 1 channel • Supports I^2C bus format • Supports the multi-master • Max. transfer rate: 400 kbps
	CAN module (RSCAN)	• 1 channel • Compliance with the ISO11898-1 specification (standard frame and extended frame) • Message buffers Max. 64 × 1 channel of receive message buffers 16 transmit message buffers per channel • Max. transfer rate: 1 Mbps

Table 1.1 Outline of Specifications (3 / 3)

Classification	Module/Function	Description
Communication function	Serial peripheral interface (RSPIa)	• 2 channels • RSPI transfer facility Using the MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped automatically with the receive buffer full for master reception • Event linking by the ELC
	SPI multi I/O bus controller (SPIBSC)	• 1 channel • One serial flash memory with multiple I/O bus sizes (single/dual/quad) can be connected. • External address space read mode (built-in read cache) • SPI operating mode • Clock polarity and clock phase can be selected. • Maximum transfer rate: 300 Mbps (for quad)
Safety	Register write protection function	Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRC)	• CRC code generation for arbitrary amounts of data in 8-, 16-, or 32-bit units • Select any of four generating polynomials: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (32-Ethernet), $X^{16} + X^{12} + X^5 + 1$ (16-CCITT), $X^8 + X^4 + X^3 + X^2 + 1$ (8-SAEJ1850), $X^8 + X^5 + X^3 + X^2 + X + 1$ (8-0x2F)
	Input clock oscillation stop function	Input clock oscillation stop detection: Available
	Clock monitor circuit (CLMA)	Monitors the abnormal output clock frequency from the PLL circuit or low-speed on-chip oscillator.
	Error control module (ECM)	• Generates an interrupt, internal reset, or error output for the error signal input from each module. • Time-out function • The error control is duplicated in the master and the checker.
Power supply voltage		VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V VCCQ33 = VDD33_USB = 3.0 to 3.6 V
Operating temperature*3		Tj = -40 to +125°C
Package		196-pin FBGA: 12 × 12 mm, 0.8-mm pitch PLBG0196GA-B
Debugging interface		• CoreSight architecture designed by Arm • Debugging function by the JTAG/SWD interface, and trace function by the trace port/ SWV interface

Note 1. EtherCAT is a registered trademark of Beckhoff Automation GmbH, Germany.
Note 2. Channels 3 and 4 are used only in asynchronous mode.
Note 3. When the operating temperature (junction temperature) is 110°C or higher, refer to the precautions regarding the high-temperature operation on the EC-1(R01AN3998).

Table 1.2 List of Functions

Module/Function		EC-1 196 Pins
Interrupt	External interrupt	NMI, IRQ0 to 4, IRQ6, IRQ7, IRQ9, IRQ11 to IRQ14, ETH0_INT, ETH1_INT
DMA	DMA controller (DMACAa)	ch0 to ch31
Timers	Compare match timer (CMT)	ch0 to ch5
	Compare match timer W (CMTW)	ch0, ch1
	Watchdog timer (WDTA)	ch0
	Independent watchdog timer (IWDTa)	Available
Communication function	EtherCAT slave controller (ESC)	2 ports
	USB 2.0 HS host/function module (USB)	ch0
	Serial communications interface with FIFO (SCIFA)	ch0 to ch4*1
	I^2C bus interface (RIICa)	ch1
	Serial peripheral interface (RSPIa)	ch0, ch1
	CAN module (RSCAN)	ch1
	SPI multi I/O bus controller (SPIBSC)	ch0
CRC calculator (CRC)		Available
Clock monitor circuit (CLMA)		Available
Event link controller (ELC)		Available

Note 1. Channels 3 and 4 are used only in asynchronous mode.

1.2 List of Products

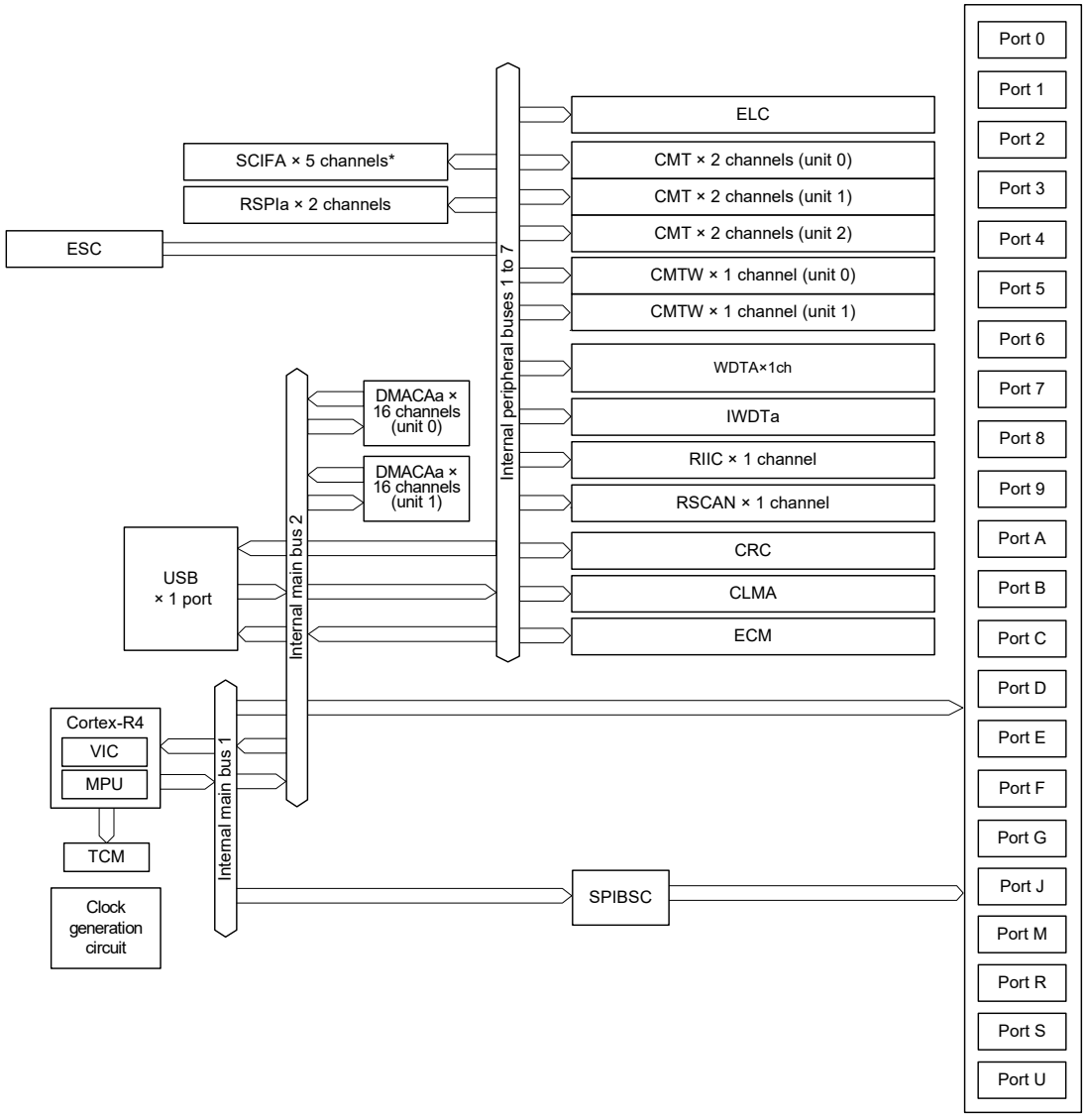
Table 1.3 is a list of products.

Table 1.3 List of Products

Part No.	Package	CPU	Operating Frequency (max.)
R9A06G043GBG	196 pins (PLBG0196GA-B)	Cortex-R4	150 MHz

1.3 Block Diagram

Figure 1.1 shows a block diagram of a 196-pin device.



ESC:	EtherCAT slave controller	CMT:	Compare match timer
DMACAa:	DMA controller	CMTW:	Compare match timer W
SPIBSC:	SPI multi I/O bus controller	RIICa:	I^2C bus interface
WDTA:	Watchdog timer	RSCAN:	CAN module
IWDTa:	Independent watchdog timer	CRC:	CRC (cyclic redundancy check) calculator
SCIFA:	Serial communication interface with FIFO	CLMA:	Clock monitor circuit
RSPIa:	Serial peripheral interface	ECM:	Error control module
USB:	USB 2.0 HS host/function module		
VIC:	Vector interrupt controller		
MPU:	Memory protection unit		
ELC:	Event link controller		

Note: Channels 3 and 4 are used only in asynchronous mode.

Figure 1.1 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1 / 3)

Classifications	Pin Name	I/O	Description
Power supply	VDD	Input	Power supply pin. Connect this pin to the system power supply.
	VSS	Input	Ground pin. Connect this pin to the system power supply (0 V).
	VCCQ33	Input	Power supply pin for I/O pin
	PLLVDD0, PLLVDD1	Input	Power supply pins for the on-chip PLL oscillator
	PLLVSS0, PLLVSS1	Input	Ground pins for the on-chip PLL oscillator. Connect these pins to the system power supply (0 V).
Clock	XTAL	Output	Connected to a crystal resonator.
	EXTAL	Input	
	CLKOUT25M0, CLKOUT25M1	Output	Output the external clock for EtherCAT PHY.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	BSCANP	Input	Inputs the boundary scan enable signal. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
	ERROROUT#	Output	Outputs the error signal from the error control module (ECM).
	RSTOUT#	Output	Outputs the reset signal externally.
Debugging interface	TRST#	Input	Test reset pin for on-chip emulator
	TMS	I/O	Test mode select pin for on-chip emulator
	TDI	Input	Test data input pin for on-chip emulator
	TDO	Output	Test data output pin for on-chip emulator
	TCK	Input	Test clock pin for on-chip emulator
	TRACECLK	Output	Outputs the clock for synchronization with the trace data.
	TRACECTL	Output	Outputs the enable signal for trace control.
	TRACEDATA0 to TRACEDATA7	Output	Output the trace data.
Interrupt	NMI	Input	Inputs the non-maskable interrupt request signal.
	IRQ0 to IRQ4, IRQ6, IRQ7, IRQ9, IRQ11 to IRQ14	Input	Input the external interrupt request signal.
	ETH0_INT, ETH1_INT	Input	Input the EtherCAT PHY interrupt request signal.
Compare match timer W (CMTW)	TIC0 to TIC3	Input	CMTW input capture input pins
	TOC0 to TOC3	Output	CMTW output compare output pins
Serial communication interface with FIFO (SCIFA)	SCK0 to SCK2	I/O	Clock I/O pins
	RXD0 to RXD4	Input	Input the receive data.
	TXD0 to TXD4	Output	Output the transmit data.
	CTS0# to CTS2#	I/O	Hardware flow control input (transmission enable signal)/general output
	RTS0# to RTS2#	Output	Hardware flow control output (transmission request signal)/general output
I^2C bus interface (RIICa)	SCL1	I/O	Clock I/O pin. The bus can be directly driven by the N-channel open drain.
	SDA1	I/O	Data I/O pin. The bus can be directly driven by the N-channel open drain.

Table 1.4 Pin Functions (2 / 3)

Classifications	Pin Name	I/O	Description
EtherCAT slave controller (ESC)	ETH0_TXC, ETH1_TXC	Input	Transmission clock input pins
	ETH0_TXEN, ETH1_TXEN	Output	Output the transmission enable signal.
	ETH0_TXD0 to 3, ETH1_TXD0 to 3	Output	Output the transmission data signal.
	ETH0_RXC, ETH1_RXC	Input	Receive clock input pins
	ETH0_RXDV, ETH1_RXDV	Input	Input the receive data enable signal.
	ETH0_RXER, ETH1_RXER	Input	Input the receive data error signal.
	ETH0_RXD0 to 3, ETH1_RXD0 to 3	Input	Input the receive data signal.
	ETH_MDC	Output	Output the management interface clock.
	ETH_MDIO	I/O	Management data signal I/O pin
	PHYLINK0, PHYLINK1	Input	Input the PHY Link signal.
	PHYRESETOUT#	Output	Output the PHY RESET signal
	CATLEDRUN	Output	Outputs the EtherCAT RUN LED signal.
	CATIRQ	Output	Outputs the EtherCAT IRQ signal.
	CATLEDSTER	Output	Outputs the EtherCAT Dual-color state LED signal.
	CATLEDERR	Output	Outputs the EtherCAT error LED signal.
	CATLINKACT0, CATLINKACT1	Output	Output the EtherCAT link/activity LED signal.
	CATSYNC0, CATSYNC1	Output	Output the EtherCAT SYNC signal.
	CATLATCH0	Input	Input the EtherCAT LATCH signal.
	CATLATCH1	Input	Input the EtherCAT LATCH signal.
	CATI2CCLK	Output	Outputs the EtherCAT EEPROM I^2C clock signal.
	CATI2CDATA	I/O	Inputs/outputs the EtherCAT EEPROM I^2C data signal.
USB 2.0 host/function module	VDD33_USB	Input	Power supply input pin for USB
	VSS_USB	Input	Ground input pin for USB
	DVDD_USB	Input	Digital power supply input pin for USB
	USB_RREF	Input	Reference current input pin for USB. Connect this pin to the VSS_USB pin via 200Ω (±1%).
	USB_DP	I/O	USB bus D+ data I/O pin
	USB_DM	I/O	USB bus D- data I/O pin
	USB_VBUSEN	Output	Outputs the VBUS power enable signal for USB.
	USB_OVRCUR	Input	Inputs the overcurrent signal for USB.
	USB_VBUSIN	Input	USB cable connection/disconnection detection input pin
CAN module (RSCAN)	CRXD1	Input	Receive data input pin
	CTXD1	Output	Transmit data output pin
Serial peripheral interface (RSPIa)	RSPCK0, RSPCK1	I/O	Clock I/O pins
	MOSI0, MOSI1	I/O	Master transmit data I/O pins
	MISO0, MISO1	I/O	Slave transmit data I/O pins
	SSL00, SSL10	I/O	Slave select signal I/O pins
	SSL01, SSL02, SSL03, SSL11	Output	Slave select signal output pins

Table 1.4 Pin Functions (3 / 3)

Classifications	Pin Name	I/O	Description
SPI multi I/O bus controller (SPIBSC)	SPBCLK	Output	Clock output pin
	SPBSSL	Output	Slave select signal output pin
	SPBMO/SPBIO0	I/O	Master transmit data/data 0 I/O pin
	SPBMI/SPBIO1	I/O	Master input data/data 1 I/O pin
	SPBIO2, SPBIO3	I/O	Data 2, data 3 I/O pins
I/O ports	P00	I/O	1-bit I/O pin
	P10, P12, P16, P17	I/O	4-bit I/O pins
	P20 to P23, P25 to P27	I/O	7-bit I/O pins
	P33 to P35	I/O	3-bit I/O pins
	P40, P42, P44	I/O	3-bit I/O pins
	P50 to P54, P56	I/O	6-bit I/O pins
	P60 to P66	I/O	7-bit I/O pins
	P70 to P77	I/O	8-bit I/O pins
	P80 to P87	I/O	8-bit I/O pins
	P90 to P97	I/O	8-bit I/O pins
	PA0 to PA7	I/O	8-bit I/O pins
	PB0 to PB7	I/O	8-bit I/O pins
	PC0 to PC7	Input	8-bit input pins
	PD5 to PD7	I/O	3-bit I/O pins
	PF5 to PF7	I/O	3-bit I/O pins
	PG2 to PG6	I/O	5-bit I/O pins
	PJ0 to PJ7	I/O	8-bit I/O pins
	PM1 to PM7	I/O	7-bit I/O pins
	PR1	I/O	1-bit I/O pin
	PS0 to PS7	I/O	8-bit I/O pins
	PU7	I/O	1-bit I/O pin
Others	IC0	Input	Connect to VSS via a resistor (pull-down)

1.5 Pin Assignments

Figure 1.2 show the pin arrangement. Table 1.5 show the pin assignments. Table 1.6 show the lists of pin functions.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	PC2	PJ2	PF7	PB5	PB2	PC1	PF5	PD6	P56	P51	IC0	IC0	VSS	A
B	PJ7	PJ4	PJ3	PJ1	PB6	PB1	PB7	P87	PD5	P53	IC0	IC0	P16	P97	B
C	P83	PJ5	PC3	PJ0	PB4	PB0	PF6	PD7	P54	VCCQ33	VCCQ33	P17	P96	P95	C
D	P84	P81	PJ6	VCCQ33	PB3	PC0	P86	P52	P50	VSS	VSS	PA7	P94	P12	D
E	TRST#	P85	P82	P80	VCCQ33	VDD	VDD	VDD	VDD	VCCQ33	VCCQ33	P90	P92	P93	E
F	P34	P33	ERROROUT#	P35	PLLVDD1	VDD	VSS	VSS	VSS	VDD	P91	PA4	PA5	PA6	F
G	PC4	PC5	TCK	TMS	PLLVSS1	VSS	VSS	VSS	VSS	VDD	PA3	P77	PA2	PA1	G
H	VCCQ33	BSCANP	PU7	IC0	PLLVDD0	VSS	VSS	VSS	VSS	VDD	P74	P75	P76	PA0	H
J	EXTAL	VSS	PM1	RES#	PLLVSS0	VDD	VSS	VSS	VSS	VDD	PE7	P71	P72	P73	J
K	XTAL	VSS	PM4	RSTOUT#	VDD33_USB	VDD	VDD	VDD	VDD	VCCQ33	PE1	PE5	PE6	P70	K
L	VSS	PM3	USB_REF	P62	VCCQ33	PG2	VDD	PR1	P27	VDD	VCCQ33	PS6	PE3	PE4	L
M	PM2	PM6	VSS_USB	P60	P64	PG3	PG5	P21	P26	P44	PS0	P00	PS7	PE2	M
N	PM7	PM5	DVDD_USB	P61	P63	PG4	PG6	P22	P20	P42	PS1	PS3	PS5	PE0	N
P	VSS_USB	USB_DM	USB_DP	P66	P65	PC6	PC7	P23	P25	P40	P10	PS2	PS4	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 1.2 Pin Arrangement (196-Pin FBGA) (Top View)

Table 1.5 Pin Assignments (196-Pin FBGA) (1 / 5)

Pin Number	Pin Name
A1	VSS
A2	PC2 / ETH0_TXC
A3	PJ2 / ETH0_TXD1
A4	PF7 / IRQ7
A5	PB5 / ETH_MDIO
A6	PB2 / ETH1_RXC
A7	PC1 / ETH1_RXD3
A8	PF5 / ETH1_TXEN
A9	PD6 / ETH1_TXD2
A10	P56
A11	P51 / PHYLINK1
A12	IC0
A13	IC0
A14	VSS
B1	PJ7 / ETH0_RXD3
B2	PJ4 / ETH0_RXD0
B3	PJ3 / ETH0_TXD0
B4	PJ1 / ETH0_TXD2
B5	PB6 / ETH_MDC
B6	PB1 / ETH1_RXER
B7	PB7 / ETH1_RXD1
B8	P87 / ETH1_TXC
B9	PD5 / ETH1_TXD3
B10	P53 / ETH1_INT
B11	IC0
B12	IC0
B13	P16
B14	P97 / IRQ7
C1	P83 / IRQ11 / CATLINKACT0 / TXD4
C2	PJ5 / ETH0_RXD1
C3	PC3 / ETH0_RXC
C4	PJ0 / ETH0_TXD3
C5	PB4 / ETH0_RXER / CATSYNC0 / CATLATCH0 / RXD3
C6	PB0 / ETH1_RXDV
C7	PF6 / ETH1_RXD0
C8	PD7 / ETH1_TXD1
C9	P54 / CLKOUT25M1
C10	VCCQ33
C11	VCCQ33
C12	P17 / PHYRESETOUT#
C13	P96
C14	P95 / IRQ13 / CTS2#
D1	P84 / CATLINKACT1 / RXD4
D2	P81 / ETH0_RXER

Table 1.5 Pin Assignments (196-Pin FBGA) (2 / 5)

Pin Number	Pin Name
D3	PJ6 / ETH0_RXD2
D4	VCCQ33
D5	PB3 / IRQ3 / PHYRESETOUT# / TXD3 / CTXD1
D6	PC0 / ETH1_RXD2
D7	P86 / ETH1_TXD0
D8	P52 / ETH0_INT
D9	P50 / PHYLINK0
D10	VSS
D11	VSS
D12	PA7 / IRQ7 / RTS2#
D13	P94 / IRQ4 / RTS2#
D14	P12
E1	TRST#
E2	P85 / CLKOUT25M0
E3	P82 / ETH0_TXEN
E4	P80 / ETH0_RXDV
E5	VCCQ33
E6	VDD
E7	VDD
E8	VDD
E9	VDD
E10	VCCQ33
E11	VCCQ33
E12	P90 / TXD4
E13	P92 / TOC3 / RXD2
E14	P93 / TIC3 / SCK2
F1	P34 / TDI
F2	P33 / TDO
F3	ERROROUT#
F4	P35 / NMI
F5	PLLVDD1
F6	VDD
F7	VSS
F8	VSS
F9	VSS
F10	VDD
F11	P91 / TXD2
F12	PA4 / ETH1_INT / RXD2
F13	PA5 / ETH0_INT / TXD2
F14	PA6 / IRQ6 / CTS2#
G1	PC4 / CATI2CCLK
G2	PC5 / CATI2CDATA
G3	TCK
G4	TMS
G5	PLLVSS1

Table 1.5 Pin Assignments (196-Pin FBGA) (3 / 5)

Pin Number	Pin Name
G6	VSS
G7	VSS
G8	VSS
G9	VSS
G10	VDD
G11	PA3 / SCK2
G12	P77 / RSPCK0 / TRACEDATA5
G13	PA2 / SSL02
G14	PA1 / MISO0 / TRACEDATA7
H1	VCCQ33
H2	BSCANP
H3	PU7 / CATIRQ
H4	IC0
H5	PLLVDD0
H6	VSS
H7	VSS
H8	VSS
H9	VSS
H10	VDD
H11	P74 / CTS1# / SSL03 / TRACEDATA2
H12	P75 / IRQ13 / SSL00 / TRACEDATA3
H13	P76 / SSL01 / TRACEDATA4
H14	PA0 / MOSI0 / TRACEDATA6
J1	EXTAL
J2	VSS
J3	PM1 / CATLEDERR
J4	RES#
J5	PLLVSS0
J6	VDD
J7	VSS
J8	VSS
J9	VSS
J10	VDD
J11	PE7 / SCK1 / RSPCK0 / TRACEDATA7
J12	P71 / TOC2 / SCK1 / TRACECTL
J13	P72 / TIC2 / TXD1 / TRACEDATA0
J14	P73 / IRQ3 / RXD1 / TRACEDATA1
K1	XTAL
K2	VSS
K3	PM4 / CATLEDRUN
K4	RSTOUT#
K5	VDD33_USB
K6	VDD
K7	VDD
K8	VDD

Table 1.5 Pin Assignments (196-Pin FBGA) (4 / 5)

Pin Number	Pin Name
K9	VDD
K10	VCCQ33
K11	PE1 / SSL03 / TRACEDATA1
K12	PE5 / TXD1 / MOSI0 / TRACEDATA5
K13	PE6 / IRQ6 / RXD1 / MISO0 / TRACEDATA6
K14	P70 / IRQ0 / RTS1# / USB_OVRCUR / TRACECLK
L1	VSS
L2	PM3 / CATSYNC0 / CATLATCH0
L3	USB_RREF
L4	P62 / SPBCLK
L5	VCCQ33
L6	PG2 / TOC0 / RSPCK1
L7	VDD
L8	PR1 / IRQ9 / CTS1#
L9	P27 / RTS0#
L10	VDD
L11	VCCQ33
L12	PS6 / IRQ14 / RXD2
L13	PE3 / IRQ3 / CTS1# / SSL01 / TRACEDATA3
L14	PE4 / RTS1# / SSL00 / TRACEDATA4
M1	PM2 / CATSYNC1 / CATLATCH1
M2	PM6 / IRQ6 / CATLINKACT0
M3	VSS_USB
M4	P60 / SPBSSL
M5	P64 / SPBMI/SPBIO1
M6	PG3 / TIC1 / MISO1
M7	PG5 / SSL10
M8	P21 / IRQ1 / CTS0#
M9	P26
M10	P44 / IRQ12 / CTS0#
M11	PS0
M12	P00 / TRACECTL
M13	PS7 / TXD2
M14	PE2 / IRQ2 / SSL02 / TRACEDATA2
N1	PM7 / CATLINKACT1
N2	PM5 / CATLEDSTER
N3	DVDD_USB
N4	P61 / SPBIO3 / CTXD1
N5	P63 / SPBMO/SPBIO0
N6	PG4 / TOC1 / MOSI1
N7	PG6 / SSL11
N8	P22 / IRQ2 / SCK0
N9	P20
N10	P42 / RXD0
N11	PS1 / IRQ1

Table 1.5 Pin Assignments (196-Pin FBGA) (5 / 5)

Pin Number	Pin Name
N12	PS3
N13	PS5
N14	PE0 / TRACEDATA0
P1	VSS_USB
P2	USB_DM
P3	USB_DP
P4	P66 / IRQ14 / CTXD1 / USB_VBUSEN
P5	P65 / SPBIO2
P6	PC6 / SCL1 / USB_VBUSIN
P7	PC7 / TIC0 / SDA1 / CRXD1
P8	P23 / TXD0
P9	P25
P10	P40 / TXD0
P11	P10 / IRQ0 / TRACECLK
P12	PS2
P13	PS4
P14	VSS

Table 1.6 List of Pin and Pin Functions (196-Pin FBGA) (1 / 5)

Pin Number	Power Supply Clock System Control	I/O Port	Timer (CMTW)	Communication (ESC)	Communication (SPIBSC)	Communication (SCIFA, RSPIa, RIICa, RSCAN, USB)	Interrupt	Others (Connect to VSS via a resistor)
A1	VSS							
A2		PC2		ETH0_TXC				
A3		PJ2		ETH0_TXD1				
A4		PF7					IRQ7	
A5		PB5		ETH_MDIO				
A6		PB2		ETH1_RXC				
A7		PC1		ETH1_RXD3				
A8		PF5		ETH1_TXEN				
A9		PD6		ETH1_TXD2				
A10		P56						
A11		P51		PHYLINK1				
A12								IC0
A13								IC0
A14	VSS							
B1		PJ7		ETH0_RXD3				
B2		PJ4		ETH0_RXD0				
B3		PJ3		ETH0_TXD0				
B4		PJ1		ETH0_TXD2				
B5		PB6		ETH_MDC				
B6		PB1		ETH1_RXER				
B7		PB7		ETH1_RXD1				
B8		P87		ETH1_TXC				
B9		PD5		ETH1_TXD3				
B10		P53		ETH1_INT				
B11								IC0
B12								IC0
B13		P16						
B14		P97					IRQ7	
C1		P83		CATLINKACT0		TXD4	IRQ11	
C2		PJ5		ETH0_RXD1				
C3		PC3		ETH0_RXC				
C4		PJ0		ETH0_TXD3				
C5		PB4		ETH0_RXER / CATSYNC0 / CATLATCH0		RXD3		
C6		PB0		ETH1_RXDV				
C7		PF6		ETH1_RXD0				
C8		PD7		ETH1_TXD1				
C9		P54		CLKOUT25M1				
C10	VCCQ33							
C11	VCCQ33							

Table 1.6 List of Pin and Pin Functions (196-Pin FBGA) (2 / 5)

Pin Number	Power Supply Clock System Control	I/O Port	Timer (CMTW)	Communication (ESC)	Communication (SPIBSC)	Communication (SCIFA, RSPIa, RIICa, RSCAN, USB)	Interrupt	Others (Connect to VSS via a resistor)
C12		P17		PHYRESETOUT#				
C13		P96						
C14		P95				CTS2#	IRQ13	
D1		P84		CATLINKACT1		RXD4		
D2		P81		ETH0_RXER				
D3		PJ6		ETH0_RXD2				
D4	VCCQ33							
D5		PB3		PHYRESETOUT#		TXD3 / CTXD1	IRQ3	
D6		PC0		ETH1_RXD2				
D7		P86		ETH1_TXD0				
D8		P52		ETH0_INT				
D9		P50		PHYLINK0				
D10	VSS							
D11	VSS							
D12		PA7				RTS2#	IRQ7	
D13		P94				RTS2#	IRQ4	
D14		P12						
E1	TRST#							
E2		P85		CLKOUT25M0				
E3		P82		ETH0_TXEN				
E4		P80		ETH0_RXDV				
E5	VCCQ33							
E6	VDD							
E7	VDD							
E8	VDD							
E9	VDD							
E10	VCCQ33							
E11	VCCQ33							
E12		P90				TXD4		
E13		P92	TOC3			RXD2		
E14		P93	TIC3			SCK2		
F1	TDI	P34						
F2	TDO	P33						
F3	ERROROUT#							
F4		P35					NMI	
F5	PLLVDD1							
F6	VDD							
F7	VSS							
F8	VSS							
F9	VSS							
F10	VDD							

Table 1.6 List of Pin and Pin Functions (196-Pin FBGA) (3 / 5)

Pin Number	Power Supply Clock System Control	I/O Port	Timer (CMTW)	Communication (ESC)	Communication (SPIBSC)	Communication (SCIFA, RSPIa, RIICa, RSCAN, USB)	Interrupt	Others (Connect to VSS via a resistor)
F11		P91				TXD2		
F12		PA4		ETH1_INT		RXD2		
F13		PA5		ETH0_INT		TXD2		
F14		PA6				CTS2#	IRQ6	
G1		PC4		CATI2CCLK				
G2		PC5		CATI2CDATA				
G3	TCK							
G4	TMS							
G5	PLLVSS1							
G6	VSS							
G7	VSS							
G8	VSS							
G9	VSS							
G10	VDD							
G11		PA3				SCK2		
G12	TRACEDATA5	P77				RSPCK0		
G13		PA2				SSL02		
G14	TRACEDATA7	PA1				MISO0		
H1	VCCQ33							
H2	BSCANP							
H3		PU7		CATIRQ				
H4								IC0
H5	PLLVDD0							
H6	VSS							
H7	VSS							
H8	VSS							
H9	VSS							
H10	VDD							
H11	TRACEDATA2	P74				CTS1# / SSL03		
H12	TRACEDATA3	P75				SSL00	IRQ13	
H13	TRACEDATA4	P76				SSL01		
H14	TRACEDATA6	PA0				MOSI0		
J1	EXTAL							
J2	VSS							
J3		PM1		CATLEDERR				
J4	RES#							
J5	PLLVSS0							
J6	VDD							
J7	VSS							
J8	VSS							
J9	VSS							

Table 1.6 List of Pin and Pin Functions (196-Pin FBGA) (4 / 5)

Pin Number	Power Supply Clock System Control	I/O Port	Timer (CMTW)	Communication (ESC)	Communication (SPIBSC)	Communication (SCIFA, RSPIa, RIICa, RSCAN, USB)	Interrupt	Others (Connect to VSS via a resistor)
J10	VDD							
J11	TRACEDATA7	PE7				SCK1 / RSPCK0		
J12	TRACECTL	P71	TOC2			SCK1		
J13	TRACEDATA0	P72	TIC2			TXD1		
J14	TRACEDATA1	P73				RXD1	IRQ3	
K1	XTAL							
K2	VSS							
K3		PM4		CATLEDRUN				
K4	RSTOUT#							
K5	VDD33_USB							
K6	VDD							
K7	VDD							
K8	VDD							
K9	VDD							
K10	VCCQ33							
K11	TRACEDATA1	PE1				SSL03		
K12	TRACEDATA5	PE5				TXD1 / MOSI0		
K13	TRACEDATA6	PE6				RXD1 / MISO0	IRQ6	
K14	TRACECLK	P70				RTS1# / USB_OVRCUR	IRQ0	
L1	VSS							
L2		PM3		CATSYNC0 / CATLATCH0				
L3	USB_RREF							
L4		P62			SPBCLK			
L5	VCCQ33							
L6		PG2	TOC0			RSPCK1		
L7	VDD							
L8		PR1				CTS1#	IRQ9	
L9		P27				RTS0#		
L10	VDD							
L11	VCCQ33							
L12		PS6				RXD2	IRQ14	
L13	TRACEDATA3	PE3				CTS1# / SSL01	IRQ3	
L14	TRACEDATA4	PE4				RTS1# / SSL00		
M1		PM2		CATSYNC1 / CATLATCH1				
M2		PM6		CATLINKACT0			IRQ6	

Table 1.6 List of Pin and Pin Functions (196-Pin FBGA) (5 / 5)

Pin Number	Power Supply Clock System Control	I/O Port	Timer (CMTW)	Communication (ESC)	Communication (SPIBSC)	Communication (SCIFA, RSPIa, RIICa, RSCAN, USB)	Interrupt	Others (Connect to VSS via a resistor)
M3	VSS_USB							
M4		P60			SPBSSL			
M5		P64			SPBMI/SPBIO1			
M6		PG3	TIC1			MISO1		
M7		PG5				SSL10		
M8		P21				CTS0#	IRQ1	
M9		P26						
M10		P44				CTS0#	IRQ12	
M11		PS0						
M12	TRACECTL	P00						
M13		PS7				TXD2		
M14	TRACEDATA2	PE2				SSL02	IRQ2	
N1		PM7		CATLINKACT1				
N2		PM5		CATLEDSTER				
N3	DVDD_USB							
N4		P61		CTXD1	SPBIO3			
N5		P63			SPBMO/SPBIO0			
N6		PG4	TOC1			MOSI1		
N7		PG6				SSL11		
N8		P22				SCK0	IRQ2	
N9		P20						
N10		P42				RXD0		
N11		PS1					IRQ1	
N12		PS3						
N13		PS5						
N14	TRACEDATA0	PE0						
P1	VSS_USB							
P2	USB_DM							
P3	USB_DP							
P4		P66		CTXD1		USB_VBUSEN	IRQ14	
P5		P65			SPBIO2			
P6		PC6		USB_VBUSIN		SCL1		
P7		PC7	TIC0			SDA1 / CRXD1		
P8		P23				TXD0		
P9		P25						
P10		P40				TXD0		
P11	TRACECLK	P10					IRQ0	
P12		PS2						
P13		PS4						
P14	VSS							

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Rating

Conditions: VSS = PLLVSS0 = PLLVSS1 = VSS_USB = 0 V

Item	Symbol	Value	Unit
Power supply voltage (I/O)	VCCQ33	–0.3 to +4.2	V
Power supply voltage (internal)	VDD	–0.3 to +1.6	V
PLL power supply voltage	PLLVDD0, PLLVDD1	–0.3 to +1.6	V
Input voltage (except for ports for 5-V tolerant*1)	V_{in1}	–0.3 to VCCQ33 + 0.3*5	V
Input voltage (ports for 5-V tolerant*1)	V_{in2}	–0.3 to +5.5*3	V
USB digital power supply voltage	DVDD_USB	–0.3 to +1.6	V
USB power supply voltage	VDD33_USB*2	–0.3 to +4.2	V
Operating temperature (junction temperature)	Tj*4	–40 to +125	°C
Storage temperature	T_{stg}	–55 to +125	°C

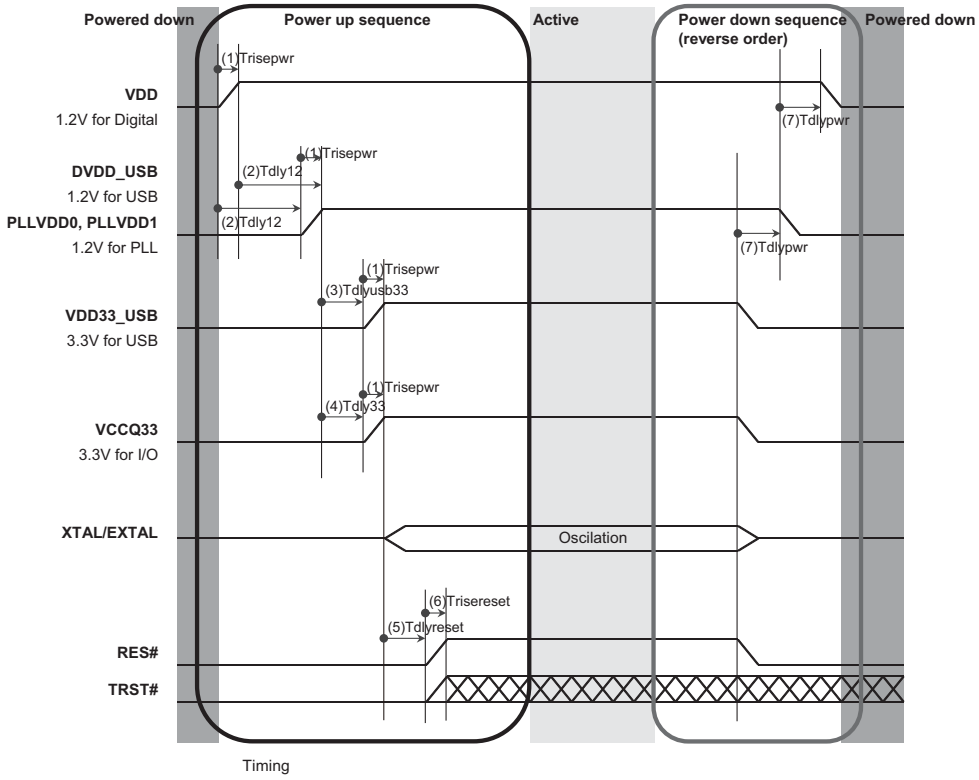
[Usage Notes]

1. Do not directly connect output pins (I/O pins in output state) of IC products to other output pins (including I/O pins in output state) , power pins, or GND pins. However, output pins are directly connectable in an external circuit where timing design is provided to avoid conflict of outputs of high-impedance pins such as I/O pins.
2. If even a single item exceeds the absolute maximum rating for even a moment, it may degrade the product's quality. In other words, the absolute maximum rating is a rated value that potentially causes physical damage to products. Use products with a margin of the absolute maximum rating.
   Specified values and conditions shown in DC characteristics and AC characteristics are the range of normal operation and quality assurance of products.

Note 1. Ports PC0 to PC7 are 5-V tolerant.
Note 2. When the USB is not to be used, connect the VDD33_USB pin to VCCQ33, the VSS_USB pin to VSS, and the DVDD_USB pin to VDD, respectively. Do not leave these pins open.
Note 3. When VCCQ33 is less than 3.0 V, the rated value of ports for 5-V tolerant is 3.6 V.
Note 4. For operations at the temperatures over 110 °C (junction temperature), refer to the “Precautions for High-Temperature Operations with the EC-1 Group (R01AN3998).
Note 5. Do not exceed the absolute maximum rating, 4.2 V.

2.2 Power On/Off Sequence

Turn on and off each power supply voltage according to the procedure shown in the figure below.
When turning on the power, be sure to fix TRST# pins and RES# pins to the low level. Otherwise, initialization is not performed successfully.



Timing

		Value		
No.	**Item**	**min**	**typ**	**max**
(1)	Trisepwr	100 us	—	50 ms
(2)	Tdly12	0 ms	—	100 ms
(3)	Tdlyusb33	0 ms	—	100 ms
(4)	Tdly33	0 ms	—	100 ms
(5)	Tdlyreset	10 ms	—	—
(6)	Trisereset	—	—	150 µs
(7)	Tdlypwr	0 ms	—	—

Note 1. Turn on all power supply voltages and reset signals with a monotonic increase and turn off with a monotonic decrease.
Note 2. Do not apply a negative voltage to power supply voltages.
Note 3. Before turning on the power, be sure to make reset pins (TRST# and RES#) active (low). Otherwise, inputs and outputs on the pins may be unstable. If this may also be a problem when turning off the power, make reset pins (TRST# and RES#) active (low.)

Note: If the power on/off sequence is not met (out of operation guarantee range), the pin input state and output state may be undefined.

Figure 2.1 Power On/Off Sequence

2.3 DC Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = VSS_USB = 0 V,
  Tj = –40 to 125°C

Table 2.2 DC Characteristics (1)

Item	Symbol	min	typ	max	Unit	Test Conditions
Power supply voltage (I/O)	VCCQ33	3.0	3.3	3.6	V	
Power supply voltage (internal)	VDD	1.14	1.2	1.26	V	
PLL power supply voltage	PLLVDD0, PLLVDD1	1.14	1.2	1.26	V	
USB digital power supply voltage	DVDD_USB	1.14	1.2	1.26	V	
USB power supply voltage	VDD33_USB	3.0	3.3	3.6	V	

Table 2.3 DC Characteristics (2) [Power Supply]

Item	Type	Symbol	typ	max	Unit	Test Conditions
Normal operation	VDD 150MHz	VIcc	107	555	mA	Tj = -40 to 125°C
	PLLVDD0 + PLLVDD1	PLLIcc	3.2	5	mA	
	VCCQ33	V33Icc	19*1, *2	—	mA	
	DVDD_USB	V12UIcc	5.1	9	mA	USB high-speed communication
			3.5	9	mA	USB full-speed communication
	VDD33_USB	V33UIcc	15*1	—	mA	USB high-speed communication
			10*1	—	mA	USB full-speed communication
Standby mode with all modules inactive (reference value)	VDD	VIcc	41	—	mA	
	PLLVDD0 + PLLVDD1	PLLIcc	3.2	—	mA	
	VCCQ33	V33Icc	0.35*1, *2	—	mA	
	DVDD_USB	V12UIcc	3.5	—	mA	UTMI suspend mode
	VDD33_USB	V33UIcc	9.6*1	—	mA	UTMI suspend mode

Note 1. These values are reference values. The actual operating current greatly depends on the system (such as unsharpened waveforms due to I/O load and toggle frequency). Be sure to measure these current values in the system.
Note 2. V33Icc must be 80 mA or less. (ΣI_{OH} in Table 2.9)

Table 2.4 DC Characteristics (3) [Except for USB2.0 Host/Function-Related Pins]

Item		Symbol	min	typ	max	Unit	Test Conditions
Schmitt trigger Input voltage	Other than 5-V tolerant pins	V_{IH1}	2.4	—	VCCQ33 + 0.3	V	
		V_{IL1}	–0.3	—	0.8	V	
		ΔV_{T1}	VCCQ33 × 0.05	—	—	V	
	5-V tolerant pins*1	V_{IH2}	VCCQ33 × 0.7	—	5.3*2	V	
		V_{IL2}	–0.3	—	VCCQ33 × 0.3	V	
		ΔV_{T2}	VCCQ33 × 0.05	—	—	V	
Input high level voltage (except for schmitt trigger input pins)		V_{IH3}	2.4	—	VCCQ33 + 0.3	V	
Input low level voltage (except for schmitt trigger input pins)		V_{IL3}	–0.3	—	0.8	V	
Output high level voltage	Other than 5-V tolerant pins	V_{OH}	VCCQ33 – 0.5	—	—	V	I_{OH} = –2 mA
Output low level voltage	Other than 5-V tolerant pins	V_{OL1}	—	—	0.4	V	I_{OL1} = 2 mA
	5-V tolerant pins*1	V_{OL2}	—	—	0.4	V	I_{OL2} = 3 mA
			—	—	0.6	V	I_{OL2} = 6 mA
Input leakage current		$\lvert I_{in} \rvert$	—	—	1.0	µA	$V_{in1} = V_{in2}$ = 0 V $V_{in1} = V_{in2}$ = VCCQ33
Three-state leakage current (off state)	Input/output and output pins excluding 5-V tolerant pins	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in1} = 0 V V_{in1} = VCCQ33
	5-V tolerant pins*1		—	—	5.0	µA	V_{in2} = 0 V V_{in2} = VCCQ33
Input pull-up MOS current/ resistance	Ports P50 to P54, P56, P86, P87, P90 to P97, PD5 to PD7	I_{pu1}	–300	—	–30	µA	VCCQ33 = 3.0 to 3.6 V $V_{in1} = V_{in2}$ = 0 V
		R_{pu1}	10	—	120	kΩ	
	Pins other than the above*3	I_{pu2}	–120	—	–7	µA	VCCQ33 = 3.0 to 3.6 V $V_{in1} = V_{in2}$ = 0 V
		R_{pu2}	25	—	515	kΩ	
Input pull-down MOS current/ resistance	Ports P50 to P54, P56, P86, P87, P90 to P97, PD5 to PD7	I_{pd1}	30	—	300	µA	VCCQ33 = 3.0 to 3.6 V $V_{in1} = V_{in2}$ = VCCQ33
		R_{pd1}	10	—	120	kΩ	
	Pins other than the above*3	I_{pd2}	7	—	120	µA	VCCQ33 = 3.0 to 3.6 V $V_{in1} = V_{in2}$ = VCCQ33
		R_{pd2}	25	—	515	kΩ	
Pin capacity	All input/output and input pins	C_{in}	—	—	10	pF	

Note 1. Ports PC0 to PC7 are 5-V tolerant.
Note 2. When VCCQ33 is less than 3.0 V, do not apply voltage of 3.6 V or higher to 5-V tolerant pins.
Note 3. 5-V tolerant pins are not included.

Table 2.5 DC Characteristics (4) [USB2.0 USB_RREF Pin]

Item	Symbol	min	typ	max	Unit	Test Conditions
Reference resistor	R_{REF}	200 ±1%			Ω	

Table 2.6 DC Characteristics (5) [USB2.0 Host/Function-Related Pins (Items for Both Full Speed and High Speed)*1]

Item	Symbol	min	typ	max	Unit	Test Conditions
DP pull-up resistor (when the function controller operation is selected)	R_{PU}	0.900	—	1.575	kΩ	Idle
		1.425	—	3.090	kΩ	Transmission/ reception
DP/DM pull-down resistors (when the host function is selected)	R_{PD}	14.25	—	24.80	kΩ	

Note 1. USB_DP and USB_DM pins

Table 2.7 DC Characteristics (6) [USB2.0 Host/Function-Related Pins (Full Speed)*1]

Item	Symbol	min	typ	max	Unit	Measuring Condition
Input high level voltage	V_{FSIH}	2.0	—	—	V	
Input low level voltage	V_{FSIL}	—	—	0.8	V	
Differential input sensitivity	V_{FSDI}	0.2	—	—	V	| (USB_DP) – (USB_DM) |
Differential common mode range	V_{FSCM}	0.8	—	2.5	V	
Output high level voltage	V_{FSOH}	2.8	—	3.6	V	I_{FSOH} = –200 µA
Output low level voltage	V_{FSOL}	0.0	—	0.3	V	I_{FSOL} = 2 mA
Output signal crossover voltage	V_{FSCRS}	1.3	—	2.0	V	CL = 50 pF (full-speed)

Note 1. USB_DP and USB_DM pins

Table 2.8 DC Characteristics (7) [USB2.0 Host/Function-Related Pins (High Speed)*1]

Item	Symbol	min	typ	max	Unit	Test Conditions
Squelch detection threshold voltage (differential voltage)	V_{HSSQ}	100	—	150	mV	
Common mode voltage range	V_{HSCM}	–50	—	500	mV	
Idle state	V_{HSOI}	–10.0	—	10.0	mV	
Output high level voltage	V_{HSOH}	360	—	440	mV	
Output low level voltage	V_{HSOL}	–10.0	—	10.0	mV	
Chirp J output voltage (differential)	V_{CHIRPJ}	700	—	1100	mV	
Chirp K output voltage (differential)	V_{CHIRPK}	–900	—	–500	mV	

Note 1. USB_DP and USB_DM pins

Table 2.9 Permissible Output Currents

Item		Symbol	min	typ	max	Unit
Permissible output low current (average value per pin)	Other than 5-V tolerant pins	I_{OL1}	—	—	2.0	mA
	5-V tolerant pins	I_{OL2}	—	—	3.0	mA
Permissible output low current (maximum value per pin)	Other than 5-V tolerant pins	I_{OL1}	—	—	4.0	mA
	5-V tolerant pins	I_{OL2}	—	—	6.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins	I_{OH}	—	—	–2.0	mA
Permissible output high current (maximum value per pin)	All output pins	I_{OH}	—	—	–4.0	mA
Permissible output high current (total)	Total of all output pins	ΣI_{OH}	—	—	–80	mA

[Usage Note] All output current values shall be within the values in Table 2.9 to ensure the reliability of this LSI.

2.4 AC Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = VSS_USB = 0 V,
  Tj = –40 to 125 °C

Table 2.10 Operating Frequency

Item		Symbol	min	max	Unit
Operating frequency	CPU clock (CPUCLK)	f	150		MHz
	System clock (ICLK)		150		
	Peripheral module clock (PCLKA)		150		
	Peripheral module clock (PCLKB)		75		
	Peripheral module clock (PCLKD)		75		
	Peripheral module clock (PCLKE)		18.75	75	
	High-speed serial clock (SERICLK)		120	150	
	External clock output for EtherCAT PHY (CLKOUT25Mn)		25		

n = 0, 1

2.4.1 Clock Timing

Table 2.11 CLKOUT25Mn Timing

Output load conditions: V_{OH} = VCCQ33 – 0.5 V, V_{OL1} = 0.4 V, C = 30 pF

Item		Symbol	min	max	Unit	Test Conditions
CLKOUT25Mn (MII)	CLKOUT25Mn cycle time	T_{ck}	40	—	ns	Figure 2.2
	CLKOUT25Mn frequency Typ. 25 MHz	—	25 ± 50 ppm		MHz	
	CLKOUT25Mn duty ratio	—	35	65	%	
	CLKOUT25Mn output low pulse width	T_{ckl}	$T_{ck}/2 - T_{ckf}$	$T_{ck}/2 + T_{ckf}$	ns	
	CLKOUT25Mn output high pulse width	T_{ckh}	$T_{ck}/2 - T_{ckr}$	$T_{ck}/2 + T_{ckr}$	ns	
	CLKOUT25Mn rising/falling time	$T_{ckr2/ckf}$	0.5	9	ns	

n = 0, 1

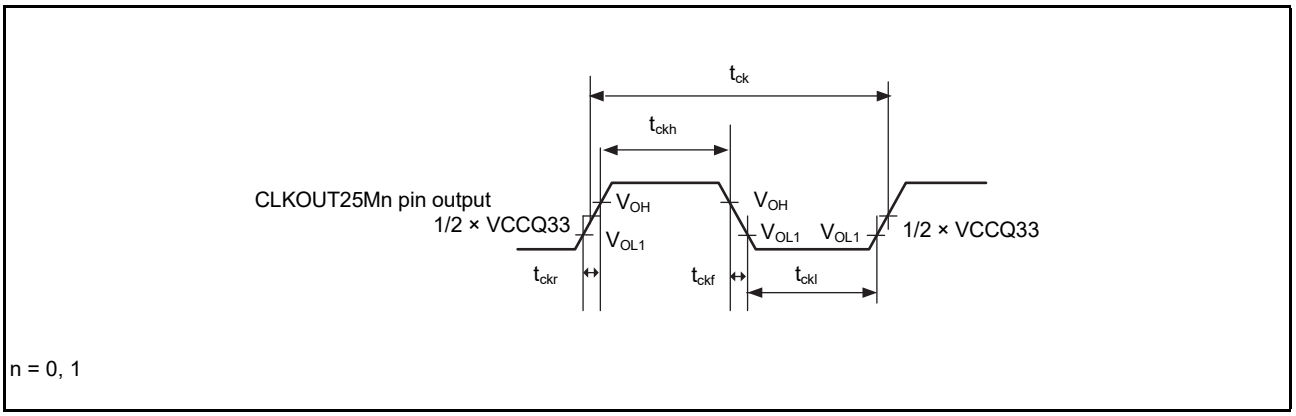


Figure 2.2 CLKOUT25Mn Pin Output Timing 2

Table 2.12 XTAL Clock Timing

Item	Symbol	min	typ	max	Unit
XTAL clock oscillator output cycle*1	$t_{XTALcyc}$	40.00 ± 50 ppm*2			ns

Note 1. When using the XTAL clock, ask the oscillator manufacturer to evaluate oscillation of the oscillator. For the oscillation stabilization time, see the evaluation result provided by the oscillator manufacturer.
Note 2. When using the EtherCAT slave controller, make sure that the clock timing satisfies 25.00 MHz ± 25 ppm.

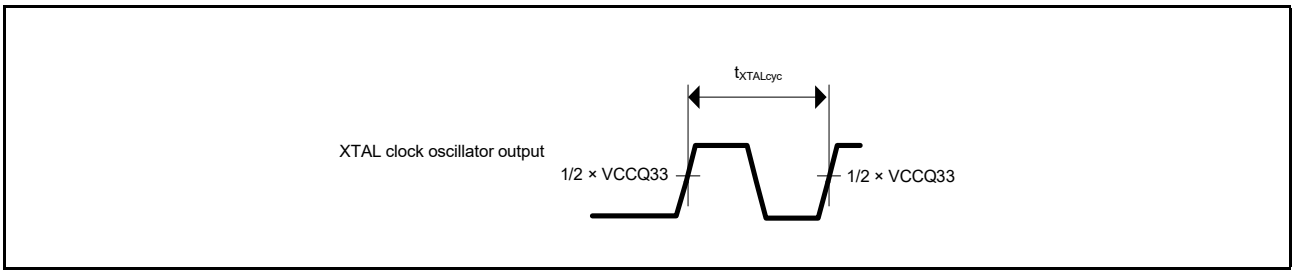


Figure 2.3 XTAL Clock Oscillator Output Timing

Table 2.13 LOCO Clock Timing

Item	Symbol	min	typ	max	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	4.62	4.17	3.79	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	40	µs	Figure 2.4

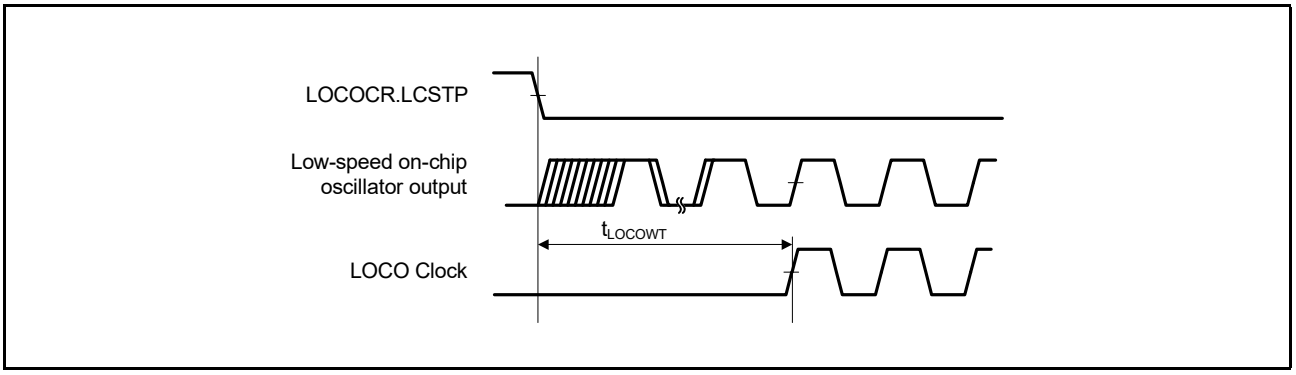


Figure 2.4 LOCO Clock Oscillation Start Timing

2.4.2 Reset Timing and Interrupt Timing

Table 2.14 Reset Timing and Interrupt Timing

Item		Symbol	Min*1	typ	max	Unit	Test Conditions
RES# pulse width	At power on	$T_{dlyreset}$	10	—	—	ms	Figure 2.5
	Other than above	$T_{dlyreset2}$	1	—	—	ms	
RES# rising time		$T_{risereset}$	—	—	150	µs	
TRST# pulse width	At power on	$T_{dlyreset}$	10	—	—	ms	
	Other than above	$T_{dlyreset2}$	1	—	—	ms	
TRST# rising time		$T_{risereset}$	—	—	150	µs	
NMI pulse width		t_{NMIW}	t_{Icyc} × 2	—	—	ns	Figure 2.6
IRQ pulse width		t_{IRQW}	t_{Icyc} × 2	—	—	ns	Figure 2.7
ETH_INT pulse width		t_{EINTW}	t_{Icyc} × 2	—	—	ns	Figure 2.8

Note 1. t_{Icyc}: ICLK cycle

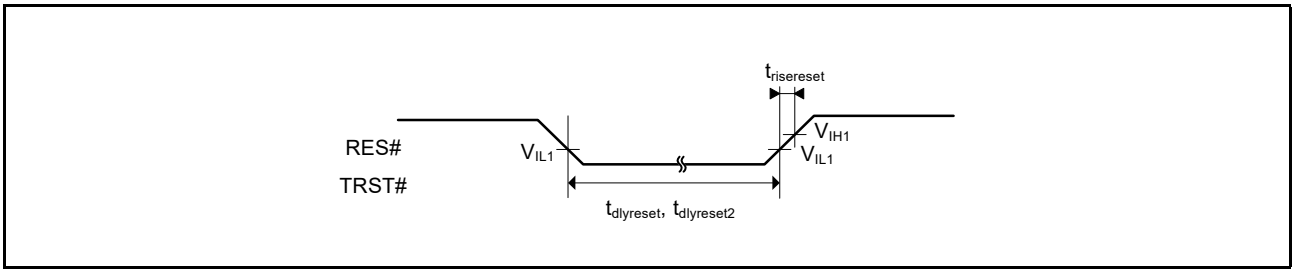


Figure 2.5 Reset Input Timing

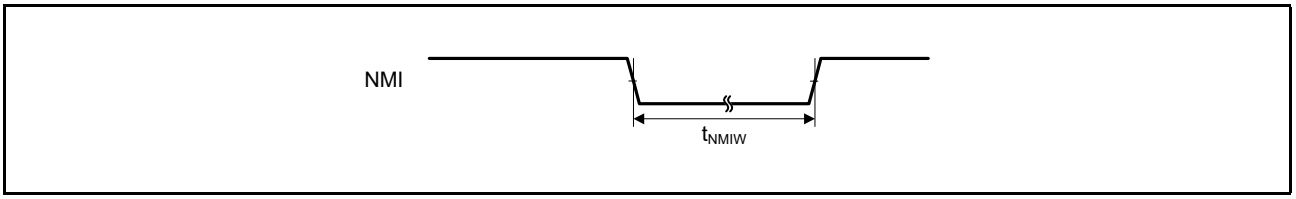


Figure 2.6 NMI Interrupt Input Timing

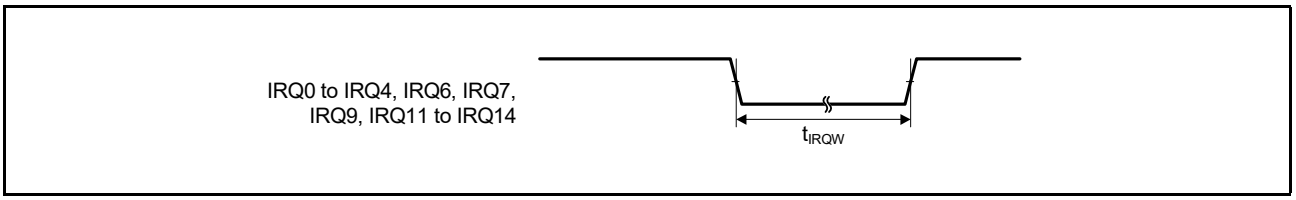


Figure 2.7 IRQ Interrupt Input Timing

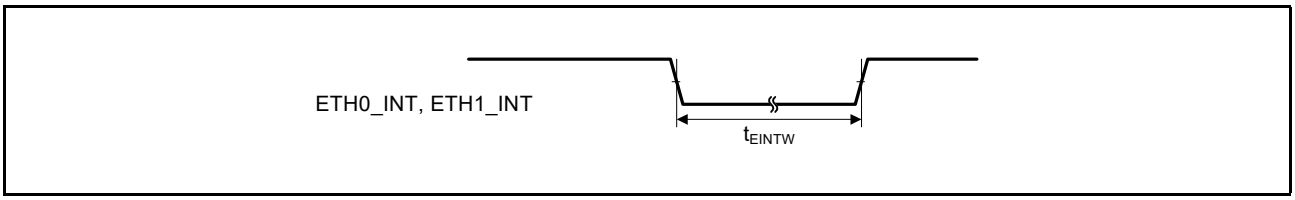


Figure 2.8 ETH_INT Interrupt Input Timing

2.4.3 On-Chip Peripheral Module Timing

2.4.3.1 I/O Port Timing

Table 2.15 I/O Port Timing

Item		Symbol	min	max	Unit*1	Test Conditions
I/O port	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 2.9

Note 1. t_{PBcyc}: PCLKB cycle

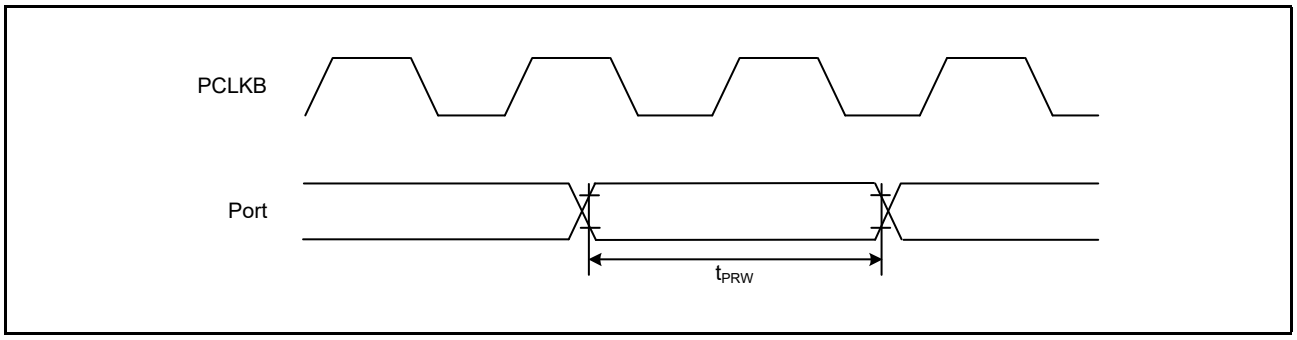


Figure 2.9 I/O Port Input Timing

2.4.3.2 CMTW Timing

Table 2.16 CMTW Timing

Item			Symbol	min	max	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWICW}$	1.5	—	t_{PDcyc}	Figure 2.10
		Both-edge setting		2.5	—		

Note 1. t_{PDcyc}: PCLKD cycle

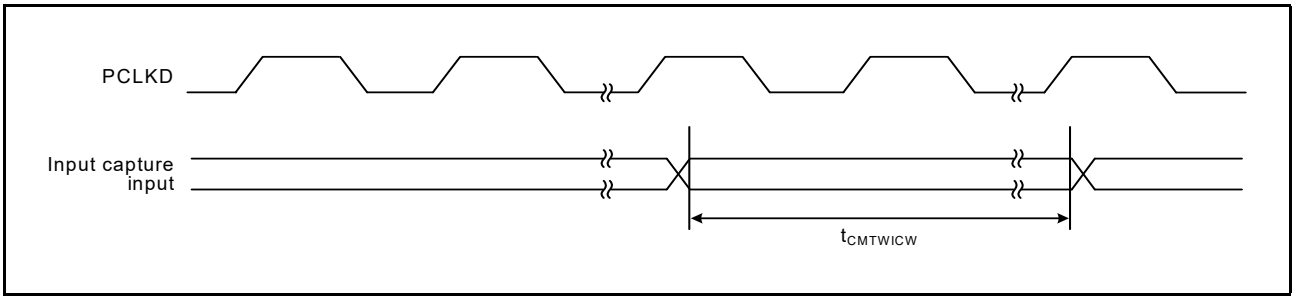


Figure 2.10 CMTW Input Capture Input Timing

2.4.3.3 SCIFA Timing

Table 2.17 SCIFA Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item			Symbol	min*1	max*1	Unit*1	Test Conditions
SCIFA	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{SEcyc}	Figure 2.11
		Clock synchronous		12	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rising time		t_{SCKr}	—	5	ns	
	Input clock falling time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{SEcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rising time		t_{SCKr}	—	9	ns	
	Output clock falling time		t_{SCKf}	—	9	ns	
	Transmit data delay time	Internal clock	t_{TXD}	– 10	10	ns	Figure 2.12
		External clock		3 × t_{SEcyc}	4 × t_{SEcyc} + 20		
	Receive data setup time	Internal clock	t_{RXS}	3 × t_{SEcyc} + 20	—	ns	
		External clock		t_{SEcyc} + 10	—		
	Receive data hold time	Internal clock	t_{RXH}	– 3 × t_{SEcyc}	—	ns	
		External clock		2 × t_{SEcyc} + 10	—		

Note 1. t_{SEcyc}: SERICLK cycle
Note 2. When the SEMR.ABCS0 bit = 1 and the SEMR.BGDM bit = 1

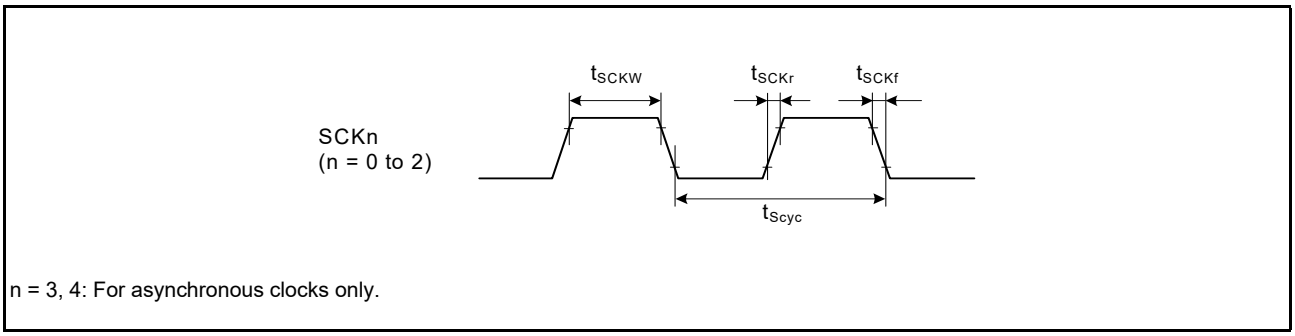


Figure 2.11 SCK Clock Input Timing

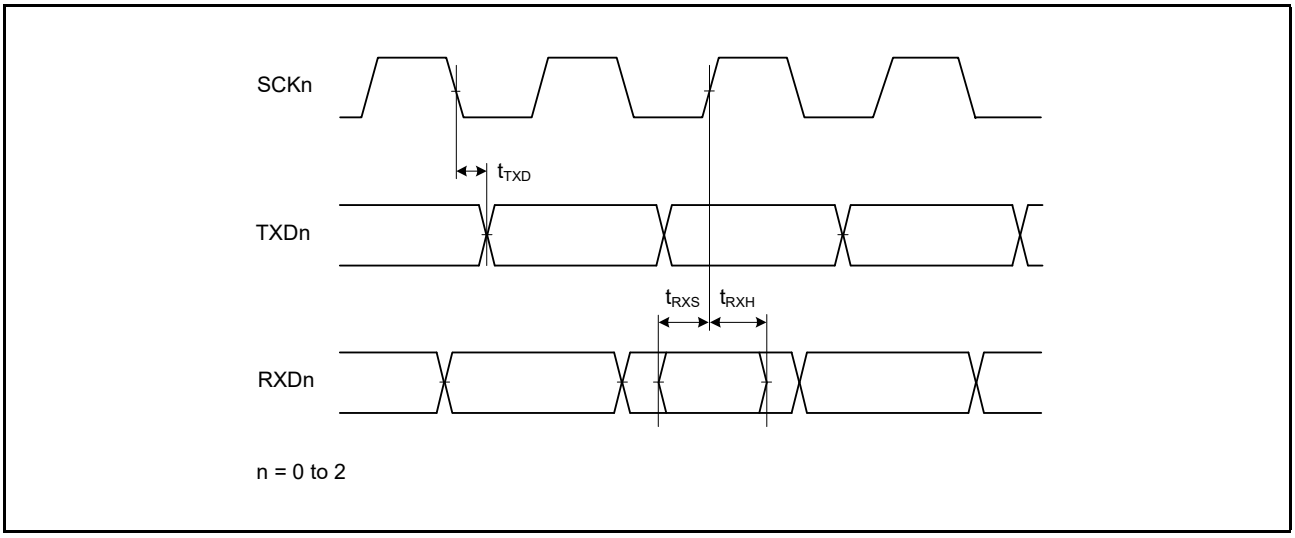


Figure 2.12 SCIFA Input/Output Timing/Clock Synchronous Mode

2.4.3.4 RSPIa Timing

Table 2.18 RSPIa Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item			Symbol*1	Min*1	Max*1	Unit*1	Test Conditions
RSPIa	RSPCK clock cycle	Master	t_{SPcyc}	4	4096	t_{SEcyc}	Figure 2.13
		Slave*4		8	4096		
	RSPCK clock high level pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		0.4	—	t_{SPcyc}	
	RSPCK clock low level pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		0.4	—	t_{SPcyc}	
	RSPCK clock rising/ falling time	Output	t_{SPCKr}, t_{SPCKf}	—	9	ns	
		Input		—	10	ns	
	Data input setup time	Master	t_{SU}	6	—	ns	Figure 2.14 to Figure 2.17
		Slave		$8 - t_{SEcyc}$	—		
	Data input hold time	Master	t_H	t_{SEcyc}	—	ns	
		Slave		$8 + 2 \times t_{SEcyc}$	—		
	SSL setup time	Master	t_{LEAD}	$N \times t_{Spcyc} - 3$*2	$N \times t_{Spcyc} + 3$*2	ns	
		Slave		4	—	t_{SEcyc}	
	SSL hold time	Master	t_{LAG}	$N \times t_{Spcyc} - 3$*3	$N \times t_{Spcyc} + 3$*3	ns	
		Slave		4	—	t_{SEcyc}	
	Data output delay time	Master	t_{OD}	—	6	ns	
		Slave		—	$3 \times t_{SEcyc} + 20$*4		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Continuous transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{SEcyc}$	$8 \times t_{SPcyc} + 2 \times t_{SEcyc}$	ns	
		Slave		$4 \times t_{SEcyc}$	—		
	MOSI, MISO rising/ falling time	Output	t_{Dr}, t_{Df}	—	9	ns	
		Input		—	10	ns	
	SSL rising/falling time	Output	t_{SSLr}, t_{SSLf}	—	9	ns	
		Input		—	10	ns	
	Slave access time		t_{SA}	—	4	t_{SEcyc}	Figure 2.16 to Figure 2.17
	Slave output release time		t_{REL}	—	3	t_{SEcyc}	

Note 1. t_{SEcyc}: SERICLK cycle
Note 2. N = SPCKD set value + 1 (1 to 8)
Note 3. N = SSLND set value + 1 (1 to 8)
Note 4. The data output delay time may become longer than half a cycle of the RSPCK clock depending on the bit rate setting. Be sure to satisfy the conditions required for the electrical characteristics of the master device.

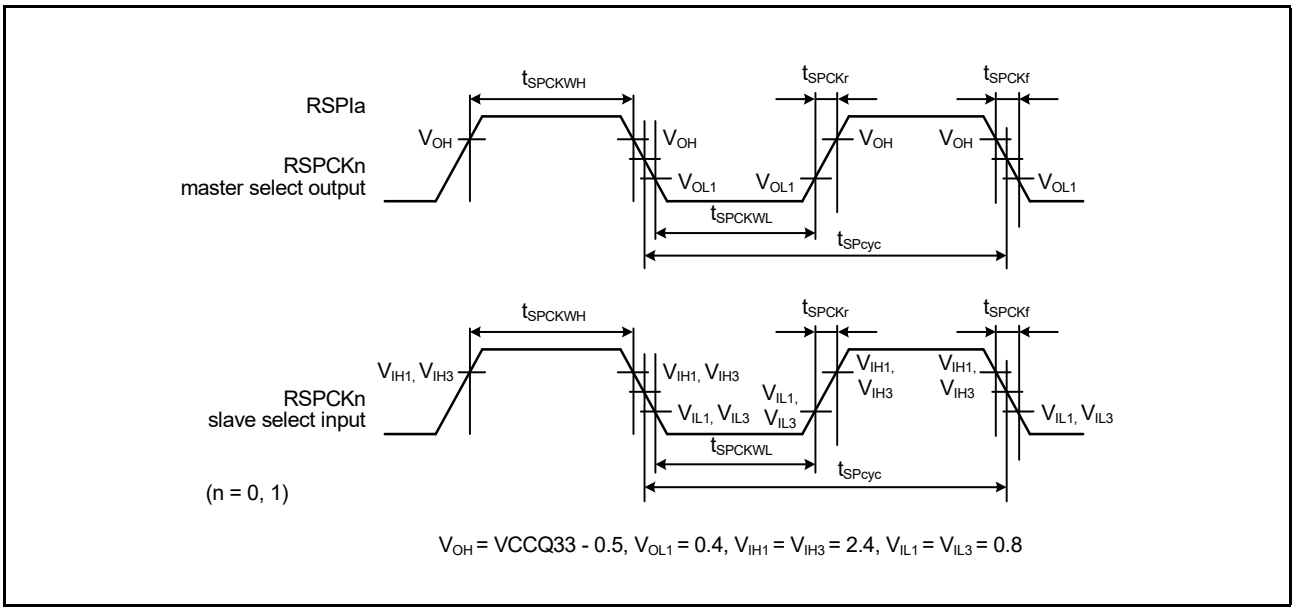


Figure 2.13 RSPIa Clock Timing

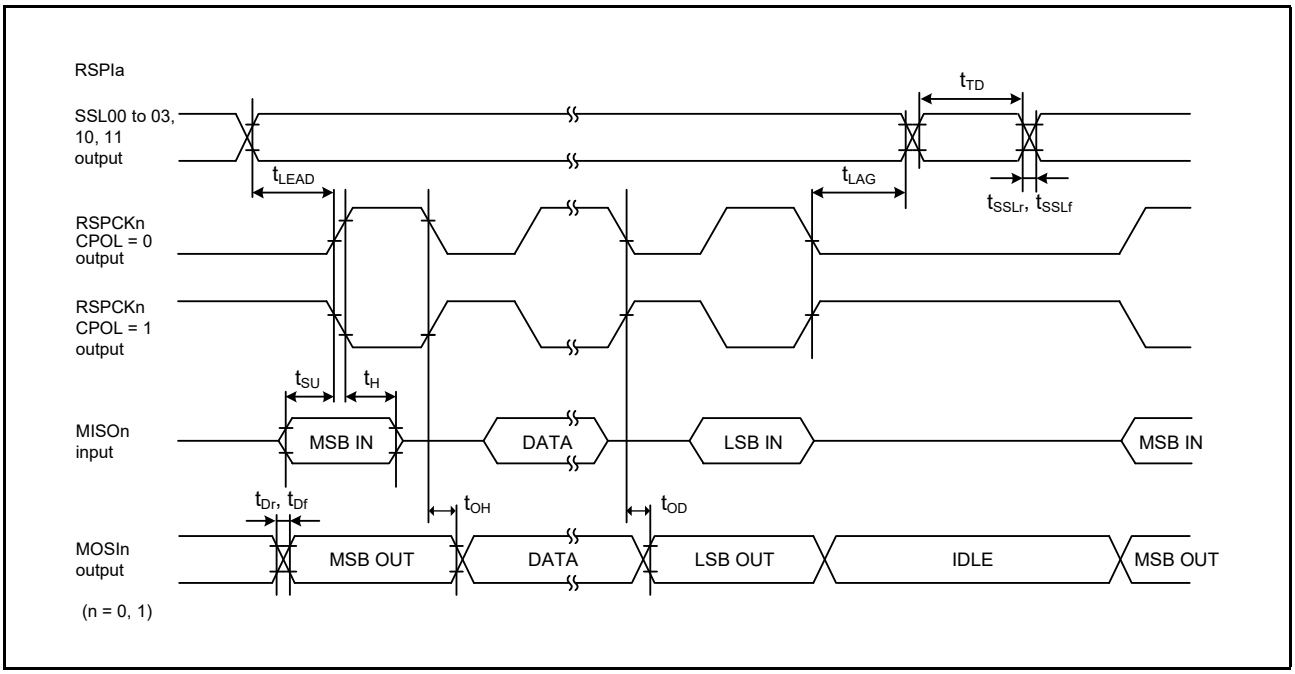


Figure 2.14 RSPIa Timing (Master, CPHA = 0)

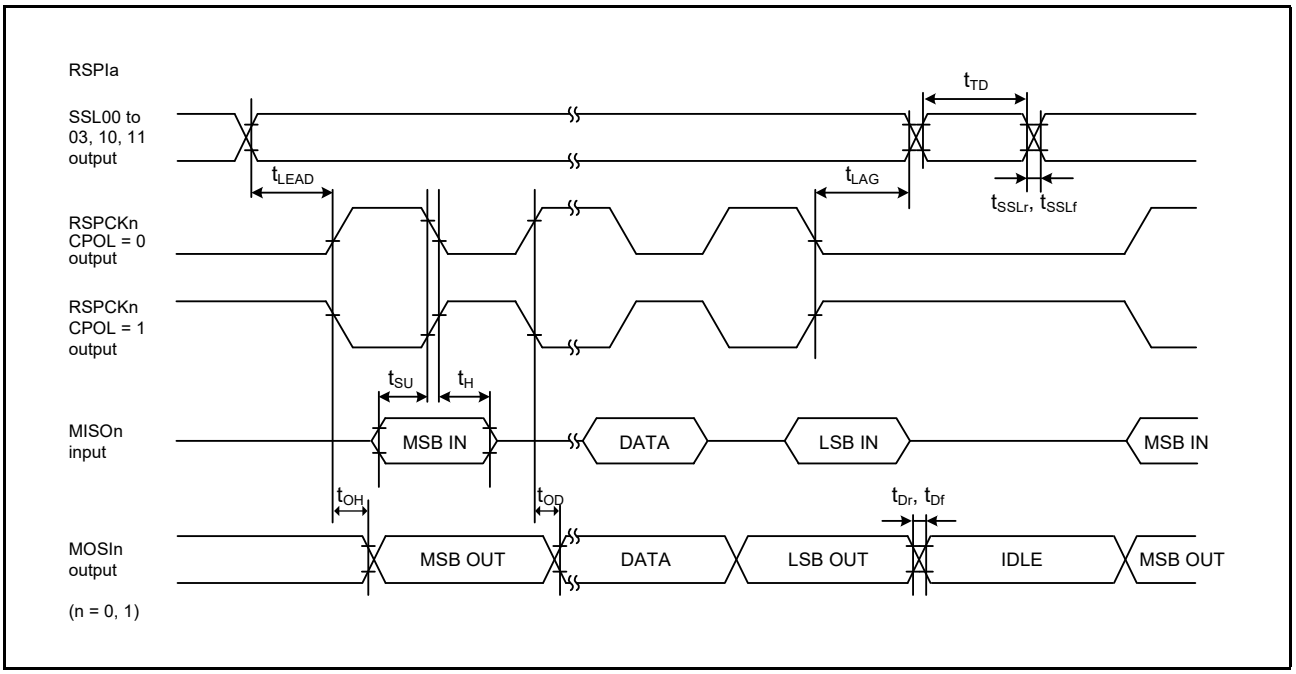


Figure 2.15 RSPIa Timing (Master, CPHA = 1)

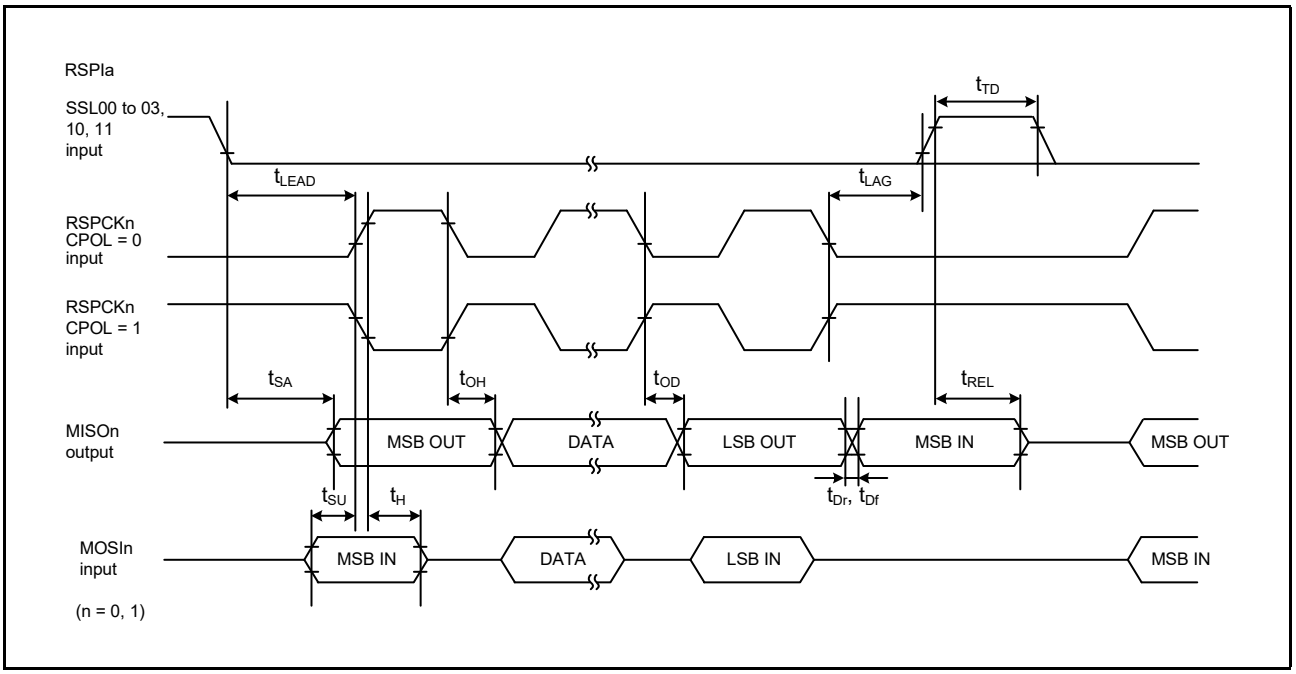


Figure 2.16 RSPI Timing (Slave, CPHA = 0)

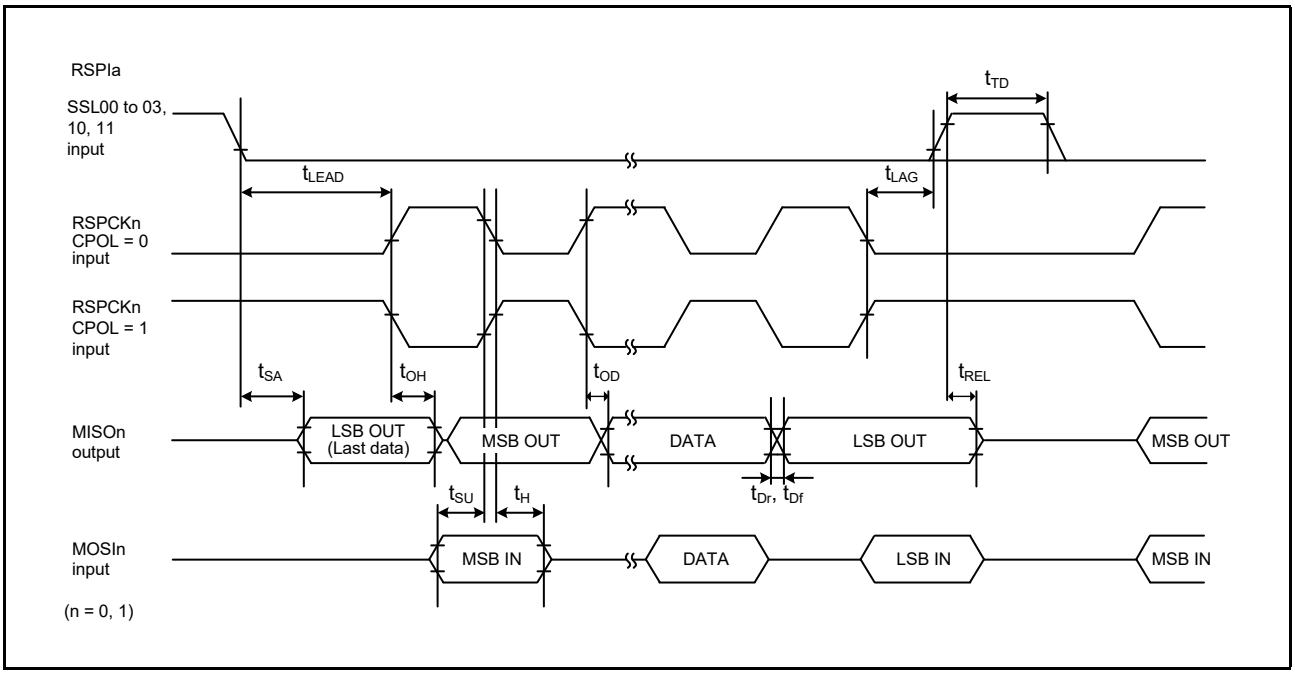


Figure 2.17 RSPI Timing (Slave, CPHA = 1)

2.4.3.5 SPIBSC Timing

Table 2.19 SPIBSC Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item		Symbol	min	max	Unit*1	Test Conditions
SPIBSC	SPBCLK clock cycle	t_{SPBcyc}	2	4080	t_{PAcyc}	Figure 2.18
	SPBCLK high level pulse width	t_{SPBWH}	0.45	0.55	t_{SPBcyc}	
	SPBCLK low level pulse width	t_{SPBWL}	0.45	0.55	t_{SPBcyc}	
	Data input setup time	t_{SU}	3.5	—	ns	Figure 2.19, Figure 2.20, Figure 2.21
	Data input hold time	t_{H}	0.5	—	ns	
	SSL setup time	t_{LEAD}	1 × t_{SPBcyc} – 3	8 × t_{SPBcyc}	ns	
	SSL hold time	t_{LAG}	1.5 × t_{SPBcyc}	8.5 × t_{SPBcyc} + 3	ns	
	Continuous transfer delay time	t_{TD}	1	8	t_{SPBcyc}	
	Data output delay time	t_{OD}	—	3.6	ns	
	Data output hold time	t_{OH}	– 1	—	ns	
	Data output buffer on time	t_{BON}	—	3.6	ns	Figure 2.22, Figure 2.23, Figure 2.24
	Data output buffer off time	t_{BOFF}	– 7	0	ns	

Note 1. t_{PAcyc}: PCLKA cycle

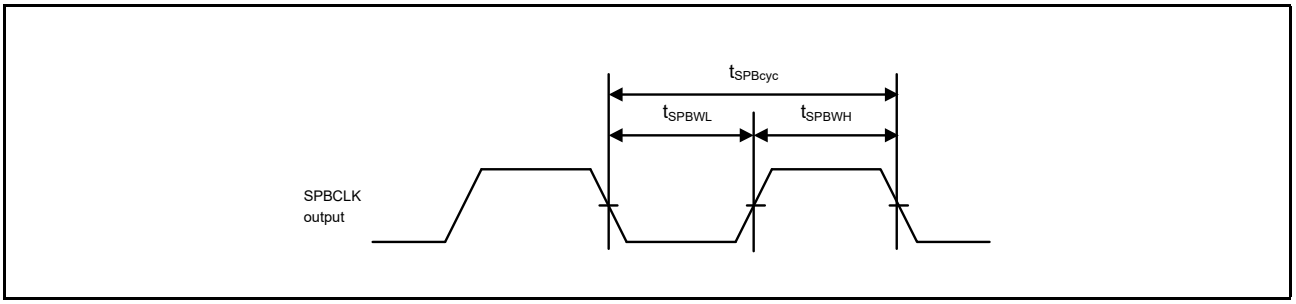


Figure 2.18 SPIBSC Clock Timing

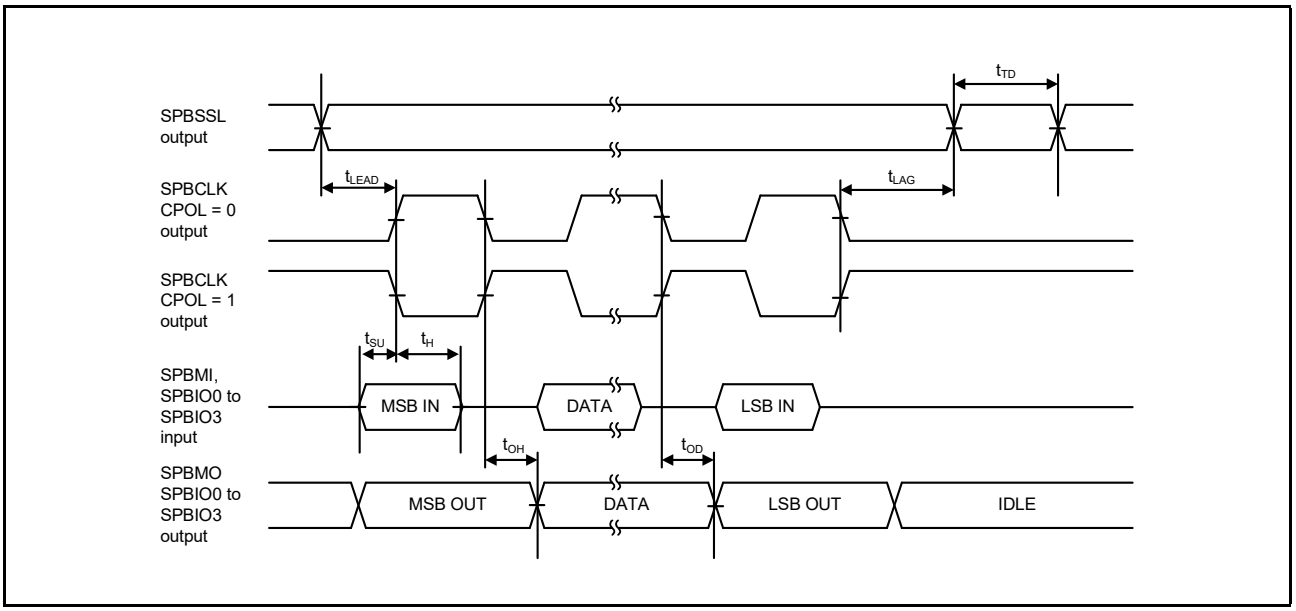


Figure 2.19 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 0)

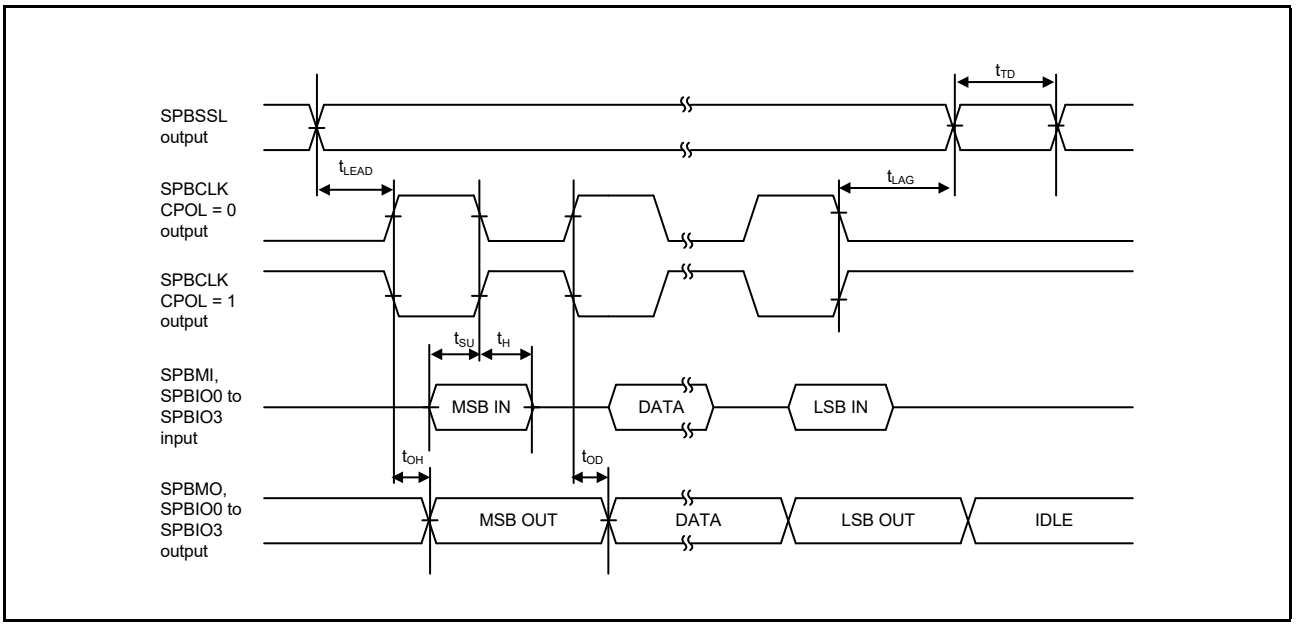


Figure 2.20 SPIBSC Transmit/Receive Timing (CPHAT = 1, CPHAR = 1)

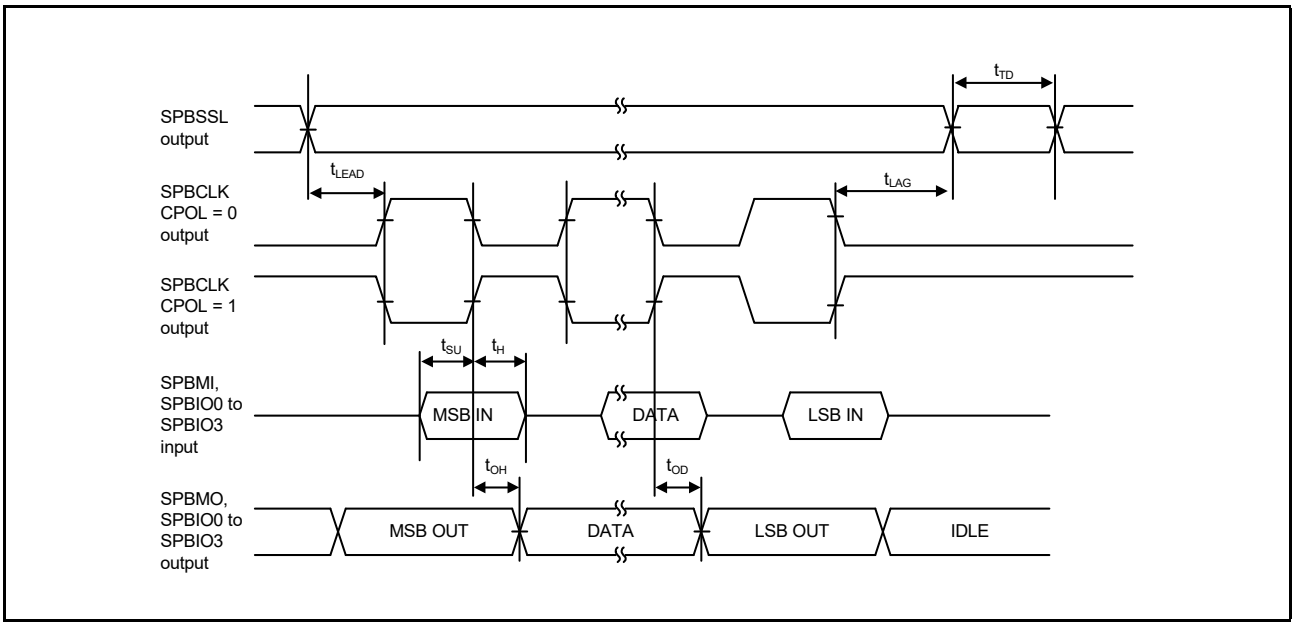


Figure 2.21 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 1)

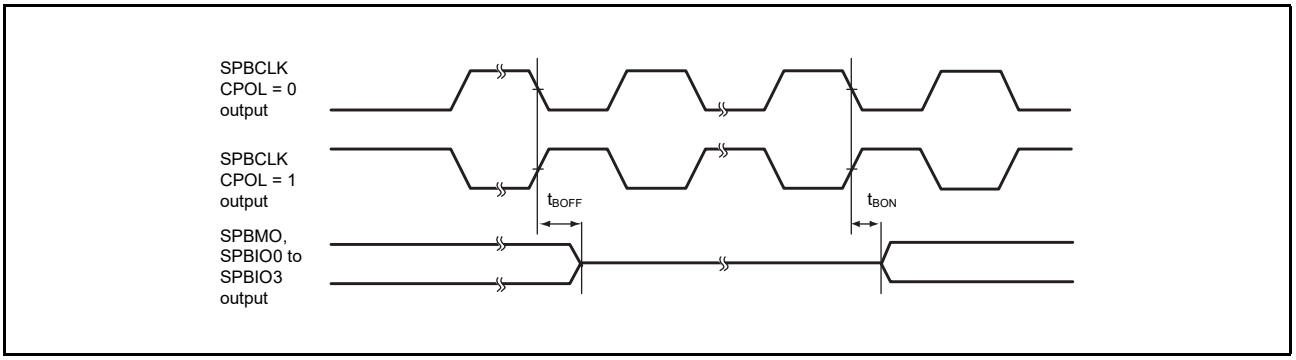


Figure 2.22 SPIBSC Buffer On/Off Timing (CPHAT = 0, CPHAR = 0)

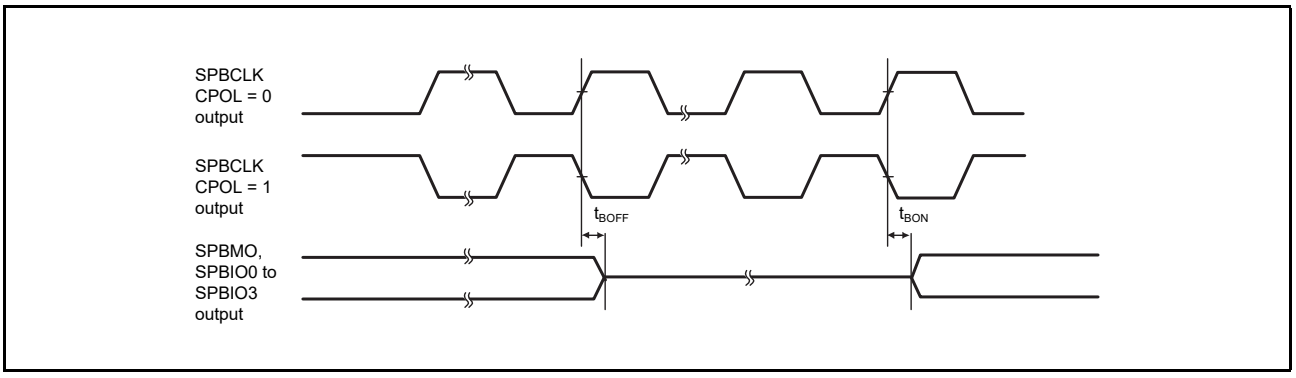


Figure 2.23 SPIBSC Buffer On/Off Timing (CPHAT = 1, CPHAR = 1)

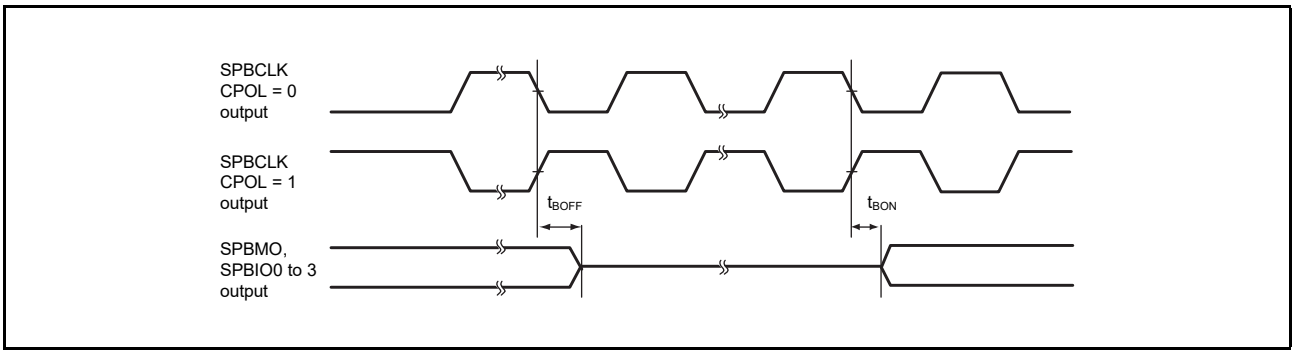


Figure 2.24 SPIBSC Buffer On/Off Timing (CPHAT = 0, CPHAR = 1)

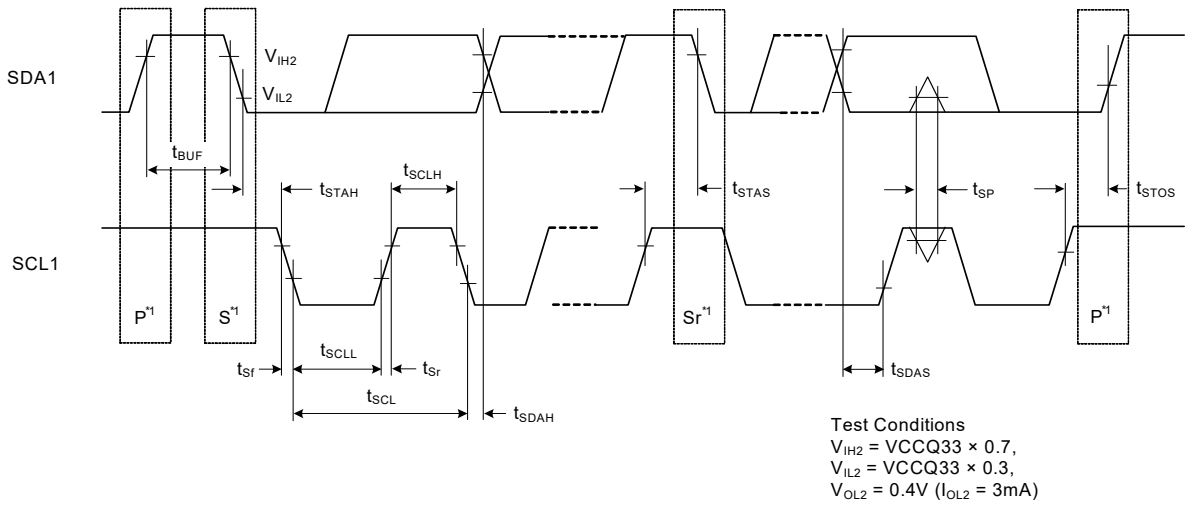
2.4.3.6 RIICa Timing

Table 2.20 RIICa Timing

Output load conditions: V_{OL2} = 0.4 V, I_{OL2} = 3 mA

Item		symbol	min*2	max*2	Unit*1	Test Conditions
RIICa (Standard-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.25
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{sr}	—	1000	ns	
	SCL, SDA input falling time	t_{sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIICa (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{sr}	—*4	300	ns	
	SCL, SDA input falling time	t_{sf}	—*4	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load*3	C_b	—	400	pF	

Note 1. t_{IICcyc}: RIICa internal reference clock (IICφ) cycle
Note 2. The value out of parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 00b while the digital filter is enabled by the setting ICFER.NFE = 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 3. Cb is the total capacitance of the bus lines.
Note 4. The minimum values are not specified for trs and tsf in Fast-mode.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.25 RIICa Bus Interface Input/Output Timing

2.4.3.7 CAN Interface Timing

Table 2.21 CAN Interface Timing

Item	Symbol	min	max	Unit	Test Conditions
Internal delay time	tnode	—	100	ns	Figure 2.26
Transmission rate		—	1	Mbps	

Internal delay time (tnode) = Internal transmission delay time (toutput) + Internal reception delay time (tinput)

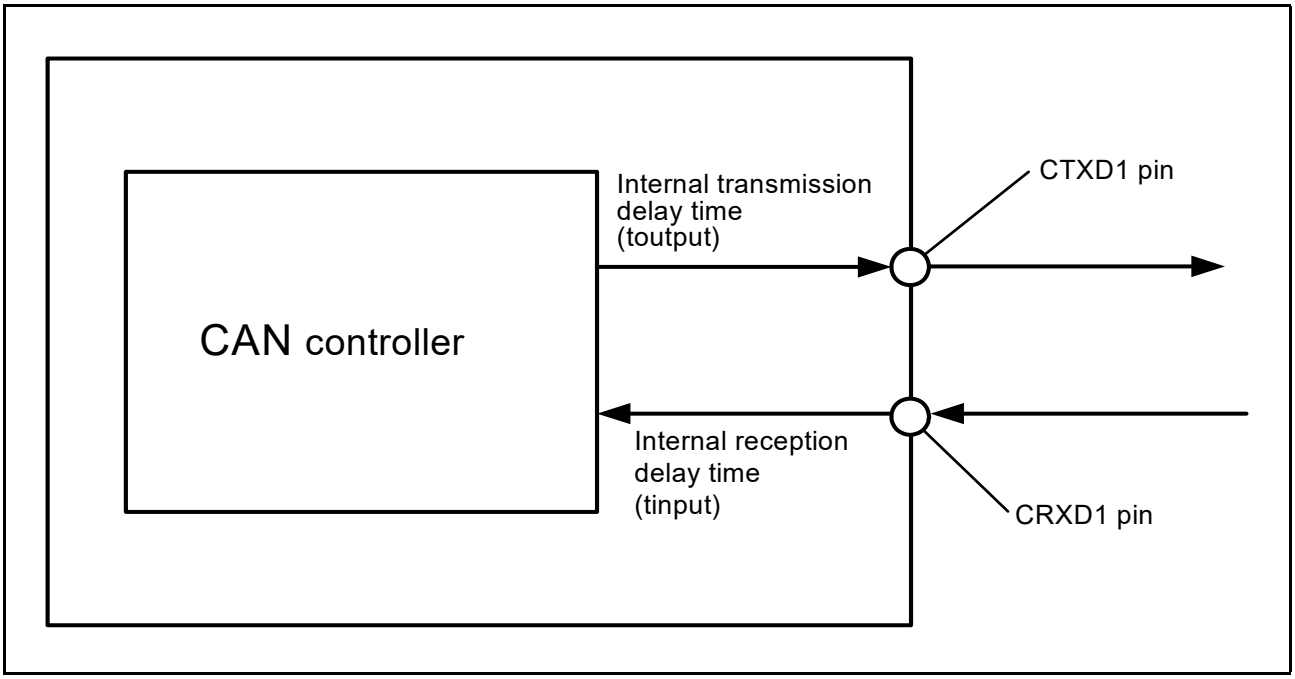


Figure 2.26 CAN Interface Conditions

2.4.3.8 ESC Timing

Table 2.22 ESC Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item		Symbol	min	max	Unit	Test Conditions
ESC (MII)	ETHn_TXC cycle time	t_{Tcyc}	40	—	ns	—
	ETHn_TXEN output delay time	t_{TENd}	0	25	ns	Figure 2.27
	ETHn_TXD0 to ETHn_TXD3 output delay time	t_{MTDd}	0	25	ns	
	ETHn_RXC cycle time	t_{TRcyc}	40	—	ns	—
	ETHn_RXDV setup time	t_{RDVs}	10	—	ns	Figure 2.28
	ETHn_RXDV hold time	t_{RDVh}	10	—	ns	
	ETHn_RXD0 to ETHn_RXD3 setup time	t_{MRDs}	10	—	ns	
	ETHn_RXD0 to ETHn_RXD3 hold time	t_{MRDh}	10	—	ns	
	ETHn_RXER setup time	t_{RERs}	10	—	ns	Figure 2.29
	ETHn_RXER hold time	t_{RERh}	10	—	ns	

n = 0, 1

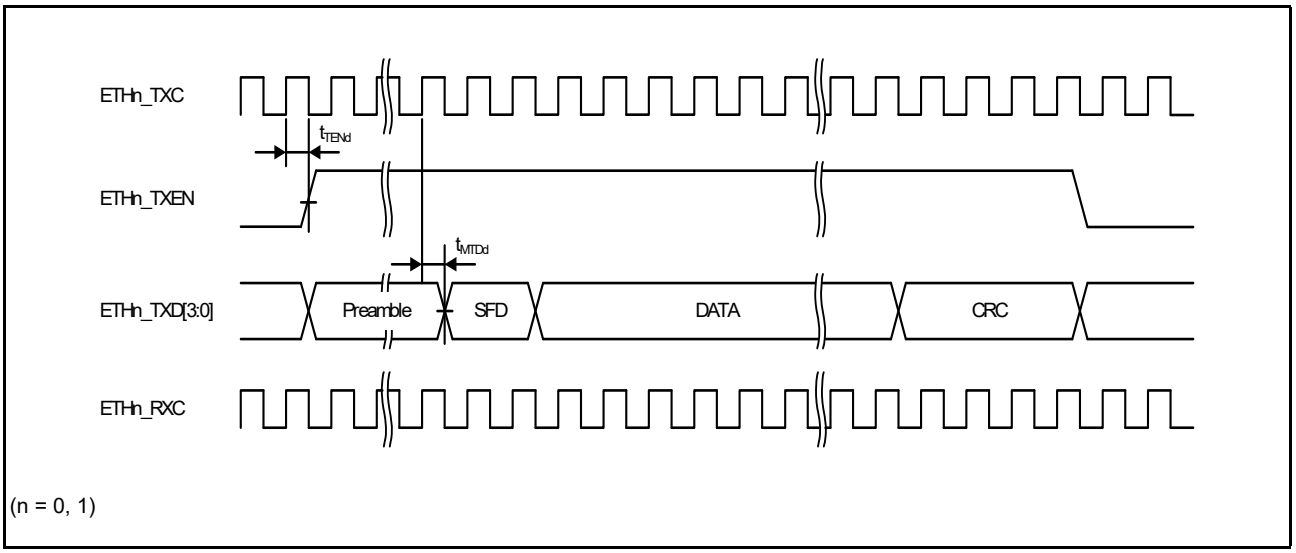


Figure 2.27 MII Transmission Timing

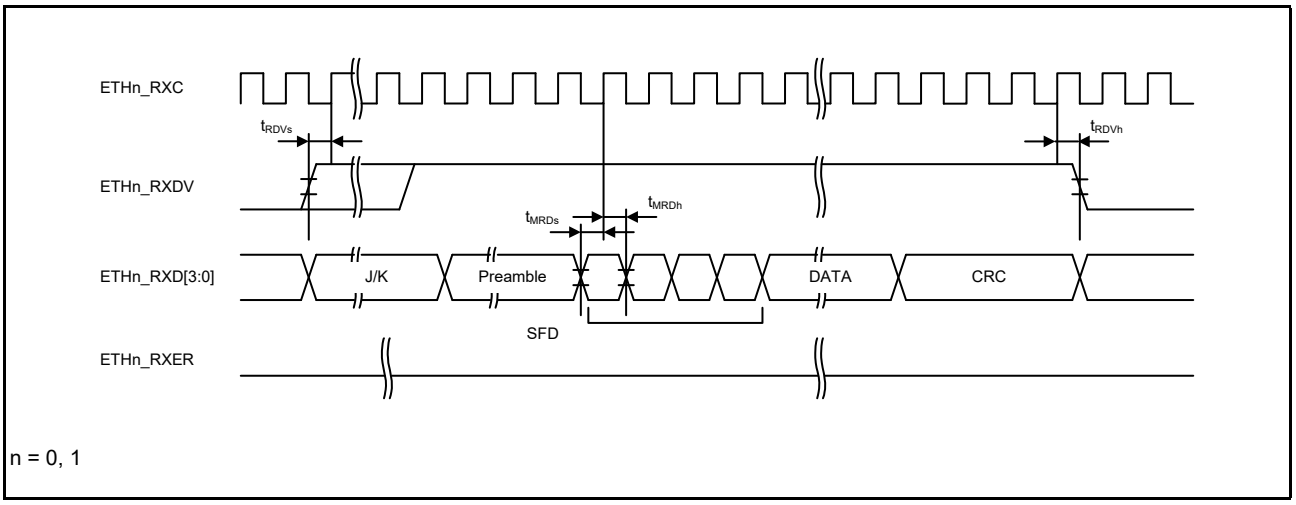


Figure 2.28 MII Reception Timing (Normal Operation)

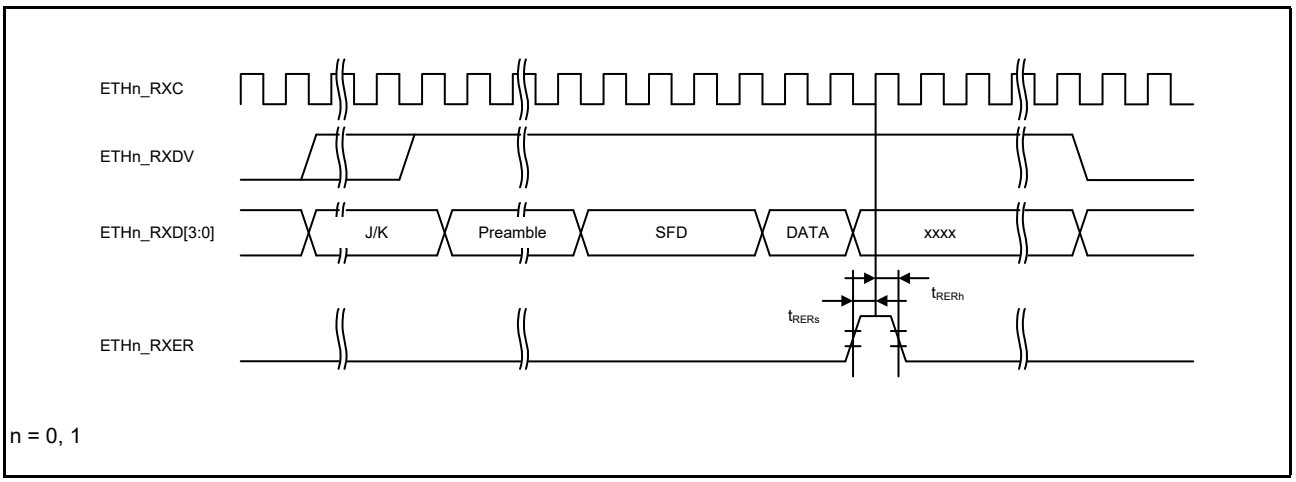


Figure 2.29 MII Reception Timing (Error Occurrence)

2.4.3.9 Serial Management Interface

Table 2.23 Serial Management Interface

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item		Symbol	min	max	Unit	Test Conditions
MDIO	ETH_MDC output cycle	t_{MDC}	80	—	ns	Figure 2.30
	ETH_MDIO input setting time (to ETH_MDC↑)	t_{SMDIO}	10	—	ns	
	ETH_MDIO input hold time (to ETH_MDC↑)	t_{HMDIO}	0	—	ns	
	ETH_MDIO output delay time (to ETH_MDC↓)	t_{DMDIO}	—	20	ns	

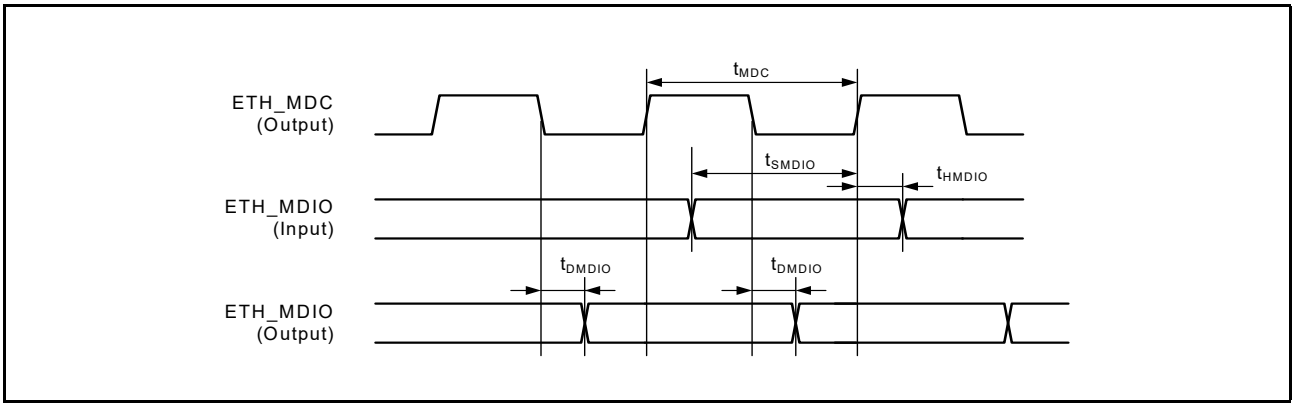


Figure 2.30 Serial Management Access Timing

2.5 USB Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = VSS_USB = 0 V,
  Tj = –40 to 125 °C

Table 2.24 On-chip USB Full-Speed Characteristics (USB_DP, USB_DM Pin Characteristics)

Item	Symbol	min	typ	max	Unit	Test Conditions
Rising time	t_{FR}	4	—	20	ns	Figure 2.31
Falling time	t_{FF}	4	—	20	ns	
Rising/falling time ratio	t_{FR} / t_{FF}	90	—	111.11	%	t_{FR} / t_{FF}

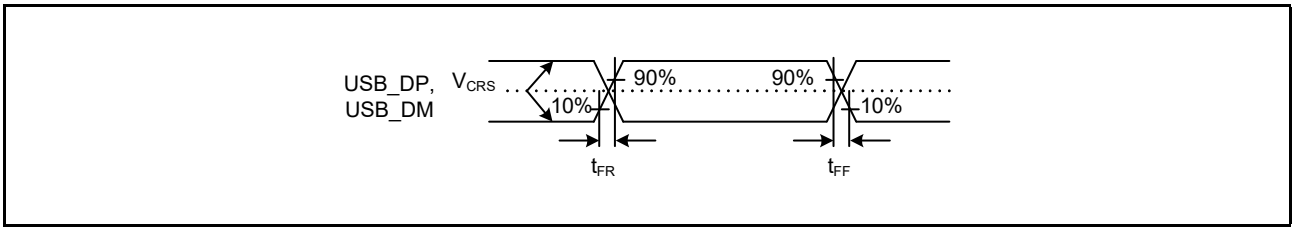


Figure 2.31 USB_DP, USB_DM Output Timing (Full Speed)

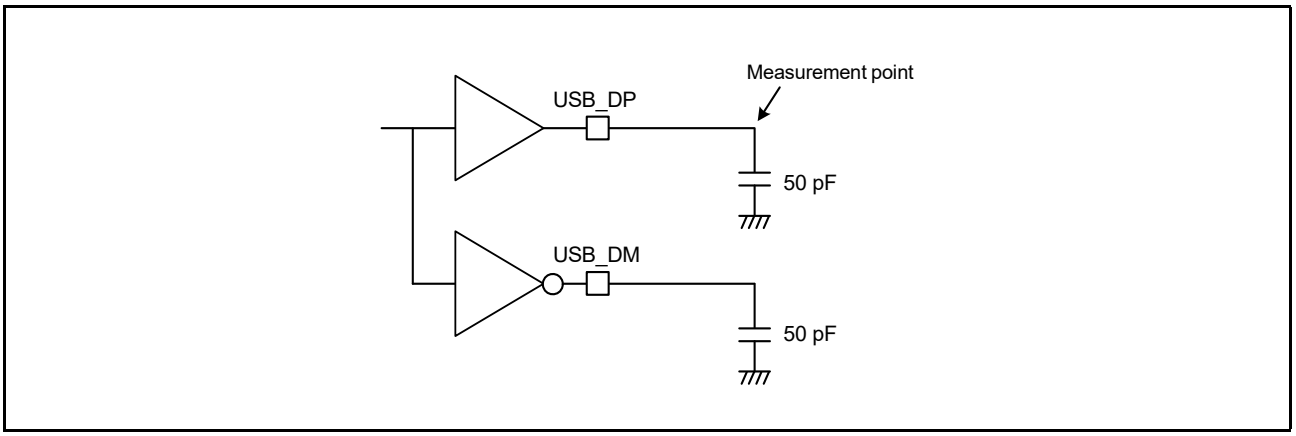


Figure 2.32 Measurement Circuit (Full Speed)

Table 2.25 On-chip USB High-Speed Characteristics (USB_DP, USB_DM Pin Characteristics)

Item		Symbol	min	typ	max	Unit	Test Conditions
AC characteristics	Rising time	t_{HSR}	500	—	—	ps	Figure 2.33
	Falling time	t_{HSF}	500	—	—	ps	
	Output resistance	Z_{HSDRV}	40.5	—	49.5	Ω	

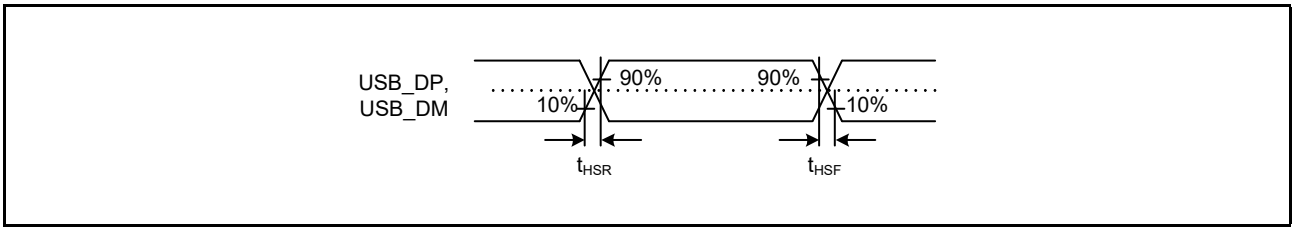


Figure 2.33 USB_DP, USB_DM Output Timing (High Speed)

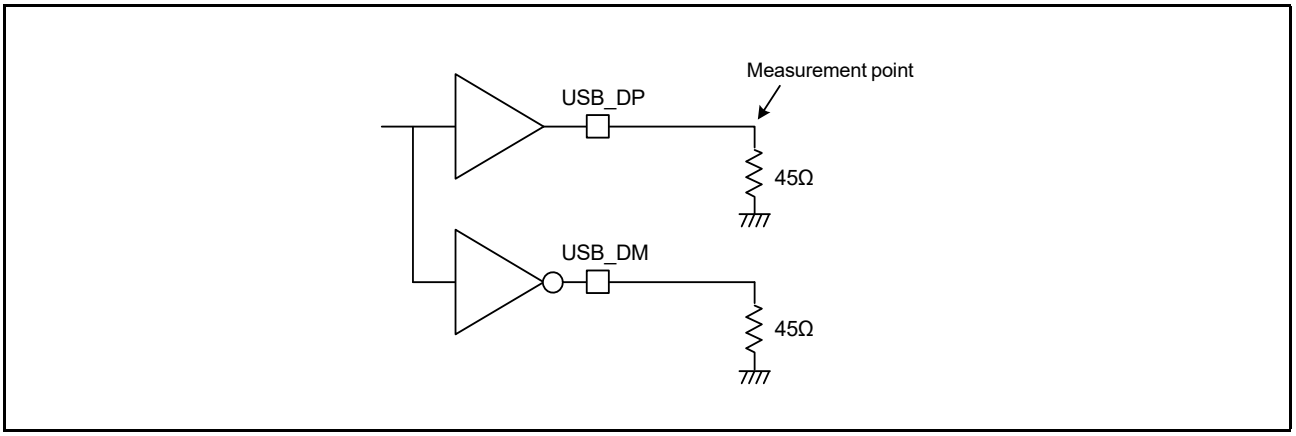


Figure 2.34 Measurement Circuit (High Speed)

2.6 Oscillation Stop Detection Timing

Table 2.26 Oscillation Stop Detection Circuit Characteristics

Item	Symbol	min	typ	max	Unit	Test Conditions
Clock switching time	t_{dr}	—	—	1	ms	Figure 2.35

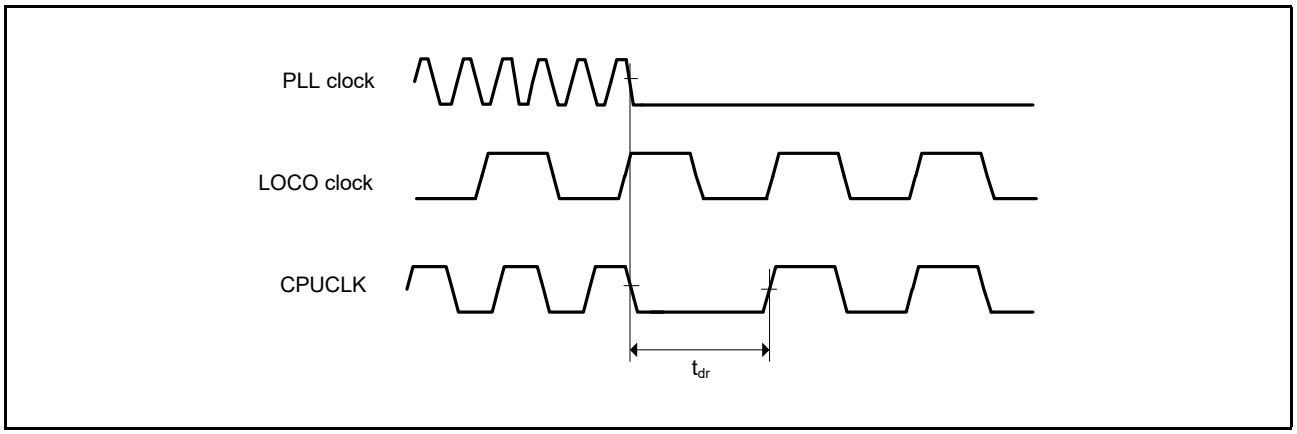


Figure 2.35 Oscillation Stop Detection Timing

2.7 Debug Interface Timing

Table 2.27 Debug Interface Timing

Output load conditions: V_{OH} = VCCQ33 – 0.5 V, V_{OL1} = 0.4 V

Item	Symbol	Min.	Max.	Unit	Reference Figure
TCK cycle time	t_{TCKcyc}	30	—	ns	Figure 2.36
TCK high pulse width	t_{TCKH}	0.4	0.6	t_{TCKcyc}	
TCK low pulse width	t_{TCKL}	0.4	0.6	t_{TCKcyc}	
TDI setup time	t_{TDIS}	5	—	ns	Figure 2.37 Output load: 30 pF
TDI hold time	t_{TDIH}	5	—	ns	
TMS/SWDIO setup time	t_{TMSS}	5	—	ns	
TMS/SWDIO hold time	t_{TMSH}	5	—	ns	
SWDIO delay time	t_{SWDO}	—	15	ns	
TDO delay time	t_{TDOD}	—	15	ns	
Capture register setup time	t_{CAPTS}	5	—	ns	Figure 2.38
Capture register hold time	t_{CAPTH}	5	—	ns	
Update register delay time	$t_{UPDATED}$	—	15	ns	
Trace clock cycle	t_{TCYC}	26.6	—	ns	Figure 2.39 Output load: 15 pF
Trace data delay time	t_{TDT}	0.25 × t_{TCYC} – 2	0.25 × t_{TCYC} + 2	ns	

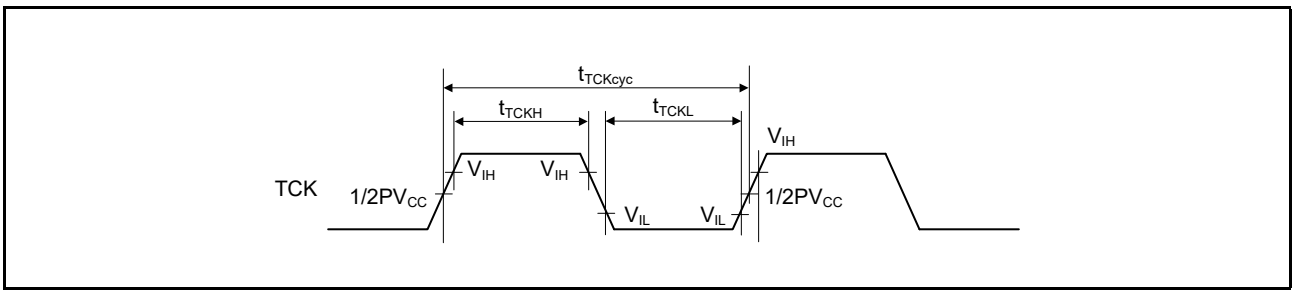


Figure 2.36 TCK Input Timing

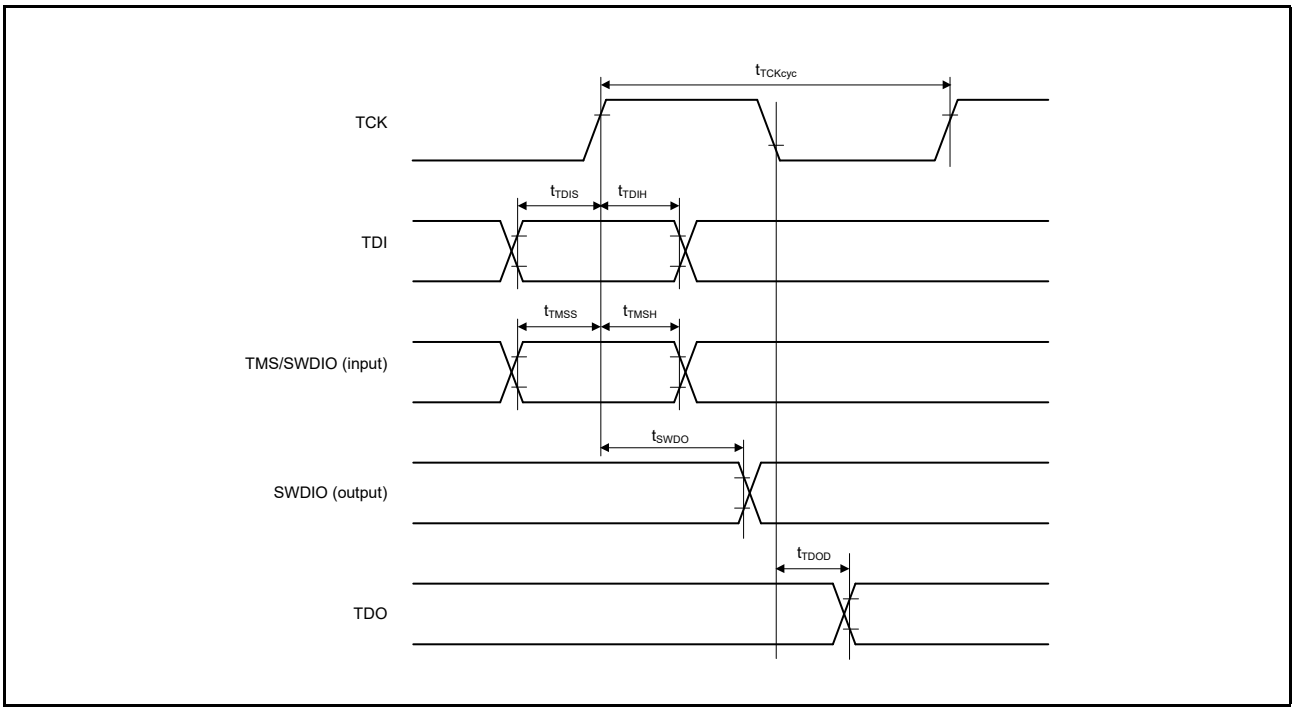


Figure 2.37 Data Transfer Timing

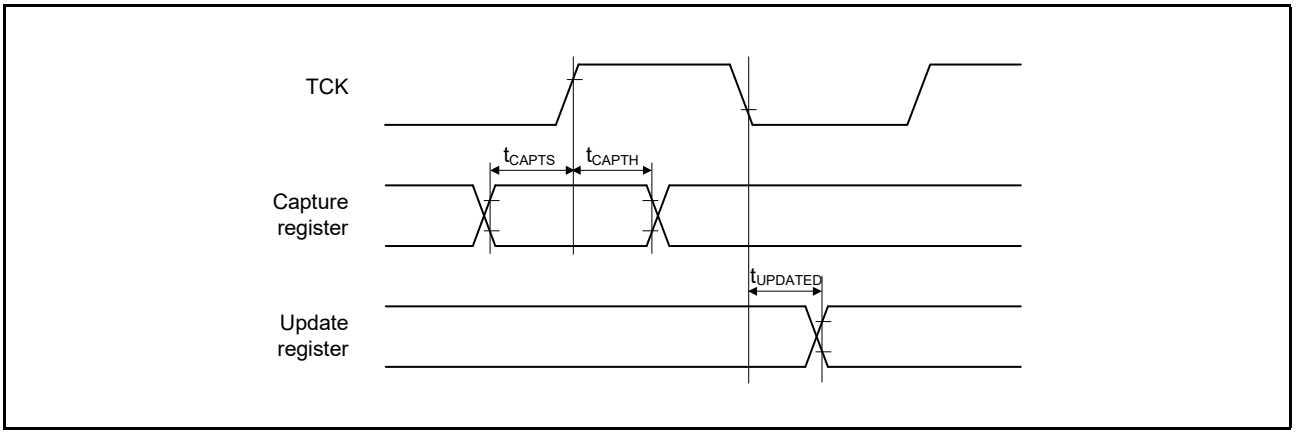


Figure 2.38 Boundary Scan Input/Output Timing

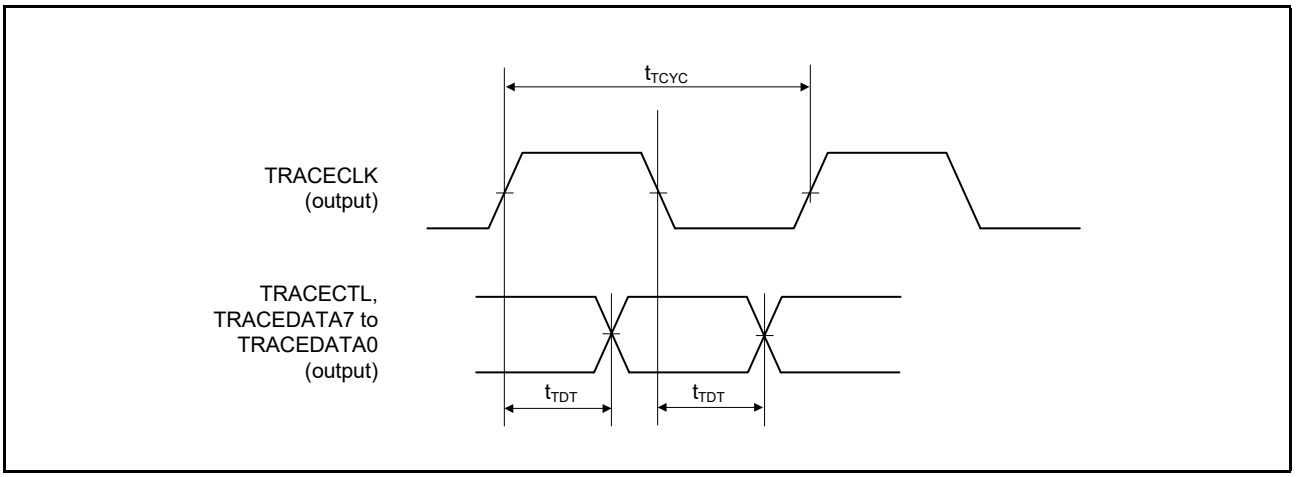


Figure 2.39 Trace Interface Timing

REVISION HISTORY — EC-1 Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Jun. 23, 2016	—	First edition, issued
1.00	Sep. 30, 2016	1. Overview	
		3	Table 1.1 Outline of Specifications (2 / 3), Communication function, CAN module (RSCAN), Message buffers: Number of channels changed, description partially deleted.
1.10	Jul. 04, 2017	2. Electrical Characteristics	
		42	Figure 2.21 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 1): Modified
1.20	Apr. 03, 2018	All	"Cortex-R4F" changed to "Cortex-R4"
		1. Overview	
		2	1.1 Outline of Specifications: “ARM Cortex®-R4F processor” changed to “ARM Cortex®-R4 processor with FPU”
		8	Table 1.4 Pin Functions (1 / 3): CTS0# to CTS2# pins: I/O and functional description changed; RTS0# to RTS2# pins: Functional description changed
		2. Electrical Characteristics	
		36	Table 2.18 RSPIa Timing: Note 2 changed, Note 3 added
1.30	Apr. 24, 2019	—	"ARM" was modified to "Arm"
		1. Overview	
		2	Table 1.1 Outline of Specifications (1/3): Central processing unit (Cortex-R4): The architecture type, corrected; Direct memory access controller (DMACAa): Activation sources, modified
		3	Table 1.1 Outline of Specifications (2/3): Compare match timer (CMT): The description of event linking, modified; I²C bus interface (RIICa): The description of event linking, deleted
		2. Electrical Characteristics	
		26	Table 2.5 DC Characteristics (4) [USB2.0 USB_RREF Pin]: Unit: Ω, added
		29	Table 2.12 XTAL Clock Timing: The rated value, modified
		36	Table 2.18 RSPIa Timing: Note 4, added
		40	Table 2.19 SPIBSC Timing: Test conditions, added (Figure 2.21, Figure 2.24)
1.40	Oct. 30, 2020	All	Registered trademark symbol added (Arm → Arm®)
		1. Overview	
		3	Table 1.1 Outline of Specifications (2 / 3): IWDTa: The unit of frequency, modified
		2. Electrical Characteristics	
		25	Table 2.4 DC Characteristics (3) [Except for USB2.0 Host/Function-Related Pins] The row of "Output high level voltage" modified: Output high level voltage / All output pins/ V_{OH} → Output high level voltage / Other than 5-V tolerant pins / V_{OH} The footnote number added: Three-state leakage current (off state) / 5-V tolerant pins / $\|I_{TSI}\|$ → Three-state leakage current (off state) / 5-V tolerant pins*1 / $\|I_{TSI}\|$ Input pull-down MOS current and resistance: The test conditions of Ipd1 and Rpd1 and of Ipd2 and Rpd2, modified
		29	Table 2.11 CLKOUT25Mn Timing: CLKOUT25Mn (MII) / CLKOUT25Mn frequency: The max. and min. values modified
		44	Table 2.20 RIICa Timing: Note 4 modified
		47	Table 2.22 ESC Timing: Index (n = 0, 1), added
		51	Table 2.25 On-chip USB High-Speed Characteristics (USB_DP, USB_DM Pin Characteristics): The header notation modified (Typ → typ)

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The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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