

Revision History FINAL

## 1 V3.1 (04-Jan-2022)

· Updated logo, disclaimer, copyright.

## 2 V3.0 (04-Nov-2016)

- · Product status changed to Production, datasheet status changed to Final.
- Notes added that DC-DC converter Boost mode is not supported, in section 5 (p.16) and section 7 (p.137).

# 3 V2.0 (25-Aug-2016)

- · Product status changed to Qualification, datasheet status changed to Preliminary.
- DA14583 qualified to Bluetooth Specification 4.2. Datasheet title and document content changed accordingly.
- Bluetooth Smart changed to Bluetooth low energy as per Bluetooth SIG directive.
- Table 3 (Pin Description), p.5/6:
  - Added note that the SPI pins of Port P2 shall not be remapped or used for any other purpose, because they are
    used for accessing the internal Flash memory during booting.
- Section 3.3 (Memories), p.9:
  - · Added text on Advanced Bootloader to OTP description.
- Section 3.6.7 (Input/Output Ports), p.11:
  - · Note text updated: SPI pins cannot be remapped or used for any other purpose.
- Section 3.7.2 (Wake-Up Timer), p.12:
  - · Added minimum pulse width of 2 sleep clock cycles for wake-up via GPIO.
- Table 126 (SPI\_CTRL\_REG), p.92: Definition of SPI\_MINT corrected:
  - ICU changed to Interrupt Controller.
  - Note on shared interrupts (SPI\_INT and AD\_INT) removed: not applicable.
- Figure 9 (QFN40 Package Outline Drawing), p.148:
  - Drawing updated to Rev B. Reason: Min/Nom/Max values added for dimensions A, A1, A2, D and E.
- Template updated to new branding guidelines.
- · Back page:
  - · Definition for datasheet status Final clarified.
  - · Disclaimer updated with trademarks statement.
  - · RoHS statement updated.
  - · Contact information updated.

# 4 V1.1 (March 6, 2015)

- · Order numbers modified (Table1 and Table 2, p.4):
  - DA14583-01AT1 changed to DA14583 01F01AT1
  - DA14583-01AT2 changed to DA14583 01F01AT2
- · Deep Sleep mode removed: not supported. Document updated accordingly in various places.
- Table 3 (Pin Description), p.6: OTP programming voltage on pin VPP corrected to 6.7 V ± 0.1 V.
- Table 276 (Flash memory: DC characteristics), p.141: conditions updated, typical values added.
- · Figure 9 (QFN Package Outline Drawing), p.147: drawing updated.



Revision History FINAL

# 5 V1.0 (February 13, 2015)

- Product status: Development, datasheet status: Target.
- Initial version, derived from DA14580.
- · Changes with respect to DA14580:
  - · Buck mode DC-DC converter only.
  - · Integrated 1 Mbit Flash memory.
  - · Package: QFN40.

### **IMPORTANT NOTICE AND DISCLAIMER**

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### **Corporate Headquarters**

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

### **Trademarks**

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

#### **Contact Information**

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit <a href="https://www.renesas.com/contact-us/">www.renesas.com/contact-us/</a>.