

## 1 V3.5 (07-Jan-2022)

Rebranded datasheet from Dialog to Renesas

## 2 V3.4 (09-Nov-2016)

- Bluetooth Smart changed to Bluetooth low energy as per Bluetooth SIG directive.
- Section 4.3.1 (OTP Header), p.11 and p.12:
  - 0x7FDC to 0x7FF0: Changed to Customer Specific Field (6 32-bit words).
  - 0x7FD4 to 0x7FDB: Bluetooth Device Address corrected from 8 32-bit words to 2 32-bit words.
- Section 13.6.2 (I2C - Master Mode Operation), p.43:
  - Changed section number from 13.7 to 13.6.2.
  - Added missing sub-section 'Master Transmit and Master Receive'.
  - Changed sub-section 'Disabling the I2C Controller' to section 13.6.3.
- Figure 56 (Block Diagram of the Analog Power Block and Internal Interconnections), p.69:
  - Minimum battery voltage for Lithium coin cell corrected from 2.2 V to 2.35 V.
- Language and title capitalization changed to US English.
- Back page:
  - Definition for datasheet status Final clarified.
  - Disclaimer updated with trademarks statement.
  - RoHS statement updated.

## 3 V3.3 (08-Jun-2016)

- DA14580 qualified to Bluetooth Specification 4.2. Datasheet title and document content changed accordingly.
- Section 17 (Wake-up timer), p.55: Added minimum pulse width of 2 sleep clock cycles for wake-up via GPIO.
- Table 196 (SPI\_CTRL\_REG), p.174: Definition of SPI\_MINT corrected:
  - ICU changed to Interrupt Controller.
  - Note on shared interrupts (SPI\_INT and AD\_INT) removed: not applicable.
- Table 326 (Absolute maximum ratings), p.220: Maximum value of  $V_{PIN(LIM)}(VDCDC\_RF)$  changed from  $\min(2, VBAT\_RF+0.2)$  to  $\min(3.3, VBAT\_RF+0.2)$ .
- Table 327 (Recommended operating conditions), p.221: Maximum value of  $V_{PIN}(VDCDC\_RF)$  changed from 2 V to 3.3 V.
- Table 342 (RCX Oscillator: Timing characteristics), p.229: Added parameters  $\Delta T_A/t(RCX)100ms$ ,  $\Delta T_A/t(RCX)4s$ :

$\Delta T_A/\Delta t(RCX)100ms$	ambient temperature gradient	buck mode only; connection interval 100 ms			0.66	°C/s
$\Delta T_A/\Delta t(RCX)4s$	ambient temperature gradient	buck mode only; connection interval 4 s			0.33	°C/s

- Figure 72 (WLSCSP34 Package Outline Drawing), p.233: drawing updated to Rev F (Min and Max values added to body size).

## 4 V3.2 (18-Dec-2015)

- Table 1 (Pin Description), p.8:
  - Programming voltage on pin VPP corrected to 6.7 V  $\pm$  0.1 V.
- Ordering information moved to new section 3 (p.9):

- Table 2: Ordering information (samples).
- Table 3: Ordering information (production).
- Table 4: Ordering information (preprogrammed OTP); previously in separate Addendum document.
- Table 5 (OTP Header), p.4:
  - 0x7F94 to 0x7FCC: Signature length corrected from 16 words to 15 words.
  - 0x7F70: Added value 0x99 for KGD.
  - 0x7F0C: Changed from 'Reserved' to 'CRC for Trim and Calibration values'.
  - 0x7F10 to 0x7F60: Changed from 'Reserved' to 'Customer Specific Field (21 32-bit words)'.
- Figure 71 (p.235): Package outline drawing of QFN40 updated.
- Section 21 (General purpose ADC), p.68:
  - Added section 21.9 (Delay counter).
- Table 291 (P01\_PADPWR\_CTRL\_REG), p.210:
  - Notes 19 and 20 updated with limited output current capability in Boost mode.
- Table 292 (P2\_PADPWR\_CTRL\_REG), p.210:
  - Note 21 updated with limited output current capability in Boost mode.
- Table 293 (P3\_PADPWR\_CTRL\_REG), p.211:
  - Note 22 updated with limited output current capability in Boost mode.
- Table 336 (Digital Input/Output: DC characteristics), p.225:
  - Note 33 added for  $V_{OH}(VBAT3V)$ : In Boost mode the output source current is limited to  $I_{out} = -250 \mu A$ .
  - Note 34 added for  $V_{OL}(VBAT3V)$ : In Boost mode the output sink current is limited to  $I_{out} = 250 \mu A$ .
- Template updated to new branding guidelines.
- Back page: Contact information updated.

## 5 V3.1 (January 29, 2015)

- General description partly rephrased.
- Features (p.1):
  - Corrected nominal package size for WLCSP34 package.
  - Package added: KGD (wafer, dice).
- Ordering information (p.6):
  - Reformatted into separate tables for samples and production orders.
  - Table 1 (samples):
    - Discontinued: DA14580-01UN6 (WLCSP34 samples in waffle pack).
    - Replacement: DA14580-01UNA (WLCSP34 samples on mini-reel).
  - Table 2 (production):
    - Added: DA14580-01WO4 (KGD, wafer)
    - Added: DA14580-01WC4 (KGD, dice)
- Figure 9 (BootROM sequence), p.16: flow corrected to jump back to top after 5 loops in Development mode.
- Figure 17 (Clock generation block diagram) p.31: label 'sys\_clk' added, generation of 'tmr2\_clk' corrected.
- Section 14 (SPI+ interface), p.50: text and figures corrected for single SPI interface (SPIx -> SPI).
- Section 17 (p.56):
  - Section title changed to 'General purpose timers'.
  - Section 17.1 (Timer 0): formulas for output frequency, duty cycle and interrupt time reformatted.

- Section 17.2 (Timer 2), p.58 and p.59:
  - Input clock frequency: corrected from 16 MHz (fixed) to  $\text{sys\_clk}/N$  with  $N = 1, 2, 4$  or  $8$  and  $\text{sys\_clk} = 16 \text{ MHz}$  or  $32 \text{ kHz}$ . Formula reformatted.
  - Output frequency: formula reformatted.
  - Figure 48 and following paragraph: input clock frequency corrected.
  - Figure 49: clock signal corrected to TMR2\_CLK.
- Section 22 (Power management), p.68 to p.70:
  - Feature 'On/off control' removed. Not supported for normal operation.
  - Minimum voltage for Buck mode operation changed from 2.2 V to 2.35 V.
  - Figures 57 and 59 updated accordingly.
- Section 25 (Registers):
  - Table 101 (CLK\_AMBA\_REG), p.110: descriptions of fields PCLK\_DIV and HCLK\_DIV rephrased.
  - Tables 309, 310 and 311 (Px\_PADPWR\_CTRL\_REG), p.212: Note added: "For buck mode the output must be powered by the 3V rail, for boost mode by the 1V rail."
- Section 26 (Specifications), p.220:
  - Definition of MIN/MAX specifications rephrased.
  - Default measurement conditions added.
  - Table 350 (Recommended operating conditions), p.223:
    - $V_{\text{BAT}}(\text{VBAT3V})\text{NO\_OTP}$ : parameter removed.  $V_{\text{BAT}}(\text{VBAT3V})$  also applies when OTP is not programmed.
  - Table 351 (DC characteristics), p.223 and 224:
    - Max value added for:  $I_{\text{BAT}}(\text{DP\_SLP})_{\text{BOOST\_8kB}}$ ,  $I_{\text{BAT}}(\text{EXT\_SLP})_{\text{BOOST\_50kB}}$ ,  $I_{\text{BAT}}(\text{ACT\_RX})_{\text{BOOST}}$ ,  $I_{\text{BAT}}(\text{ACT\_TX})_{\text{BOOST}}$ ,  $I_{\text{BAT}}(\text{DP\_SLP})_{\text{BUCK\_8kB}}$ ,  $I_{\text{BAT}}(\text{EXT\_SLP})_{\text{BUCK\_50kB}}$ ,  $I_{\text{BAT}}(\text{ACT\_RX})_{\text{BUCK}}$ ,  $I_{\text{BAT}}(\text{ACT\_TX})_{\text{BUCK}}$ .
    - Supply voltage condition removed for:  $I_{\text{BAT}}(\text{DP\_SLP})_{\text{BUCK\_1kB}}$ ,  $I_{\text{BAT}}(\text{DP\_SLP})_{\text{BUCK\_2kB}}$ ,  $I_{\text{BAT}}(\text{DP\_SLP})_{\text{BUCK\_8kB}}$ ,  $I_{\text{BAT}}(\text{ACT\_RX})_{\text{BOOST}}$ ,  $I_{\text{BAT}}(\text{ACT\_TX})_{\text{BOOST}}$ ,  $I_{\text{BAT}}(\text{ACT\_RX})_{\text{BUCK}}$ ,  $I_{\text{BAT}}(\text{ACT\_TX})_{\text{BUCK}}$ . Default measurement conditions apply.
  - Table 364 (Radio: AC characteristics), p.229: Note 31 (reference to AN-B-017) removed.

## 6 V3.0 (September 25, 2014)

### 6.1 CRITICAL CHANGES

- Product status changed to Production, datasheet status changed to Final.
- Section 26 (Specifications), p.220: added MIN/MAX definitions and reference diagrams for Boost and Buck mode (Figures 68 and 69).
- Table 348 (Absolute maximum ratings), p.223:
  - $V_{\text{PIN(LIM)}}(\text{default})$ : condition text corrected, maximum value changed from 3.6 V to  $\min(3.6, \text{VBAT\_RF}+0.2) \text{ V}$ .
  - $V_{\text{BAT(LIM)}}\text{VBAT1V}$ : minimum value changed from 0.9 V to -0.1 V.
  - $V_{\text{BAT(LIM)}}\text{VBAT3V}$ : minimum value changed from 1.8 V to -0.1 V.
  - $V_{\text{PIN(LIM)}}(1\text{V2})$ : minimum value changed from 0 V to -0.2 V, maximum value changed from 1.2 V to  $\min(1.2, \text{VBAT\_RF}+0.2) \text{ V}$ .
  - Added parameter  $V_{\text{PIN(LIM)}}(\text{VDCDC\_RF})$  with minimum value -0.2 V, maximum value  $\min(2, \text{VBAT\_RF}+0.2) \text{ V}$ .
  - Added parameter  $V_{\text{PIN(LIM)}}(\text{XTAL32Kp})$  with minimum value -0.2 V, maximum value  $\min(1.5, \text{VBAT\_RF}+0.2) \text{ V}$ .
  - $V_{\text{ESD(MM)}}(\text{WLCSP34})$ : maximum value changed from 175 V to 200 V.
- Table 349 (Recommended operating conditions), p.224:

- $V_{PP}$ : specification changed from 6.55 V, 6.8 V, 7.05 V (Min, Typ, Max) to 6.6 V, 6.7 V, 6.8 V (Min, Typ, Max); added condition  $T_J \leq 50\text{ }^{\circ}\text{C}$ .
- $V_{BAT}(VBAT3V)$ : also applies to pin  $V_{BAT\_RF}$ , conditions updated accordingly.
- Added parameter  $V_{BAT}(VBAT3V)NO\_OTP$  with minimum value 1.8 V, maximum value 3.3 V and condition 'OTP not programmed'.
- $V_{PIN}(\text{default})$ : maximum value changed from 3.3 V to  $\min(3.3, V_{BAT\_RF}+0.2)$ .
- Added parameter  $V_{PIN}(VDCDC\_RF)$  with minimum value 0 V, maximum value 2 V.
- Note 20: added text 'Trim values programmed in the OTP as well as the application image, should be copied into RAM while  $V_{BAT3V} \geq 2.5\text{ V}$ '.
- Table 351 (Timing characteristics), p.226:
  - Added Note 21 to typical values of  $t_{STA}(\text{BOOST})$  and  $t_{STA}(\text{BUCK})$ : 'Worst-case value under Normal Operating Conditions.'
- Table 352 (16 MHz Crystal Oscillator: Recommended operating conditions), p.226:
  - $\Delta f_{XTAL}(16M)$ : Min/Max values changed from -15/+15 ppm to -20/+20 ppm. Added Note 22: 'Using the internal varicaps a wide range of crystals can be trimmed to the required tolerance.'
  - Added parameter  $\Delta f_{XTAL}(16M)UNT$  with Min/Max values -40/+40 ppm, condition 'untrimmed' and Note 23: 'Maximum allowed frequency tolerance for compensation by the internal varicap trimming mechanism.'
- Table 363 (Radio: AC characteristics), p.230:
  - $P_{SENS}(EOC)$  specification changed from -89 dBm (Max) to -87 dBm (Max).

## 6.2 NON CRITICAL CHANGES

- Figure 3 and Figure 4 (system diagrams for Boost mode and Buck Mode) moved from section 1 (Block diagram) to section 26 (Specifications) and renamed to Figure 68 and Figure 69.
- Figure 9 (BootROM sequence), p.16:
  - Timeout loop (64 ms) for checking OTP LDO voltage clarified.
  - Added step 'Switch to XTAL16M' to Development mode.
- Table 6 (Power domains), p.17: description of power domain  $PD\_RAD$  (Radio) rephrased.
- Figure 17 (Clock generation block diagram), p.31: enable signal for Divide by 10 function corrected from  $TIMER0\_CTRL\_REG[TIM0\_CLK\_SEL]$  to  $TIMER0\_CTRL\_REG[TIM0\_CLK\_DIV]$ .
- Figure 30 (UART block diagram), p.44: updated to only show implemented flow control signals RTS and CTS.
- Section 14 (SPI+ interface), p.50: DMA functionality removed (not supported), Figure 36 updated accordingly.
- Section 15 (Quadrature decoder), p.54:
  - Figures 41, 42 and 43 updated: pin names corrected.
  - Last paragraph removed: 'The interrupt block monitors ...'.
- Figure 50 (Watchdog timer block diagram), p.60: date removed.
- Figures 57 and 58 (Supply overview), p.69: component values removed.
- Section 23 (BLE core), p.71: redundant feature bullet on Bluetooth Smart compliance removed.
- Figure 61 (Exchange memory mapping possibilities), p.72: text edited.
- Section 25 (Registers), p.78: added references to ARM Cortex-M0 documentation.
- Table 43 ( $BLE\_DIAGCNTL\_REG$ ), p.94: references to chapter 2.15 removed (internal design document).
- Table 108 ( $TRIM\_CTRL\_REG$ ), p.113: Note 17 added: 'The period duration of 250  $\mu\text{s}$  is derived by dividing the RC16M clock signal by 4000. Consequently, the period duration may vary over temperature.'
- Table 111 ( $CLK\_RCX20K\_REG$ ), p.115: oscillator name 'RCX32K' corrected to 'RCX'.
- Table 137 ( $UART\_MCR\_REG$ ), p.123: description of bit  $UART\_AFCE$  clarified, reference to section "Auto Flow Control" removed (internal design document).

- Table 163 (UART\_SRTS\_REG), p.146: description of bit UART\_SHADOW\_REQUEST\_TO\_SEND clarified.
- Table 177 (UART2\_MCR\_REG), p.152: description of bit UART\_AFCE clarified, reference to section "Auto Flow Control" removed (internal design document).
- Table 203 (UART2\_SRTS\_REG), p.175: description of bit UART\_SHADOW\_REQUEST\_TO\_SEND clarified.
- Table 338 (GP\_CONTROL\_REG), p.219: description of bit EM\_MAP: text 'Case <n>, available' removed.
- Figure 68 (System diagram: Boost mode) updated, p.221:
  - Pin RST not connected
  - Pin VDCDCA renamed to VDCDC\_RF
  - Pin VBATA renamed to VBAT\_RF
  - C8 = 1  $\mu$ F (was: 100 nF)
  - C9 = 1  $\mu$ F (was: NP)
- Figure 69 (System diagram: Buck mode) updated, p.222:
  - Pin RST not connected
  - Pin VDCDCA renamed to VDCDC\_RF
  - Pin VBATA renamed to VBAT\_RF
  - C8 = 1  $\mu$ F (was: 100 nF)
  - Added C9 = 1  $\mu$ F on pin VBAT\_RF
  - 32.768 kHz XTAL oscillator optional
- Table 349 (Recommended operating conditions), p.224:
  - $V_{BAT}(VBAT3V)$  and  $V_{BAT}(VBAT3V)NO\_OTP$ : reference to Note 19 moved from Conditions to Min column.
- Table 350 (DC characteristics), p.224 and p.225:
  - $I_{BAT}(DP\_SLP)\_BOOST\_1kB$  and  $I_{BAT}(DP\_SLP)\_BOOST\_2kB$ : condition changed from 'Typical boost-application' to 'Boost configuration'.
  - $I_{BAT}(DP\_SLP)\_BUCK\_1kB$  and  $I_{BAT}(DP\_SLP)\_BUCK\_2kB$ : condition changed from 'Typical buck-application' to 'Buck configuration'.
- Table 362 (Radio: DC characteristics), p.229:
  - Note 29: text '(VBAT3V = 3 V)' appended.
- Back page: contact information updated.

## 7 V1.63 February 25 2013

### 7.1 CRITICAL CHANGES

- Added note about WLCSP light sensitivity at the package information chapter
- Updated Ordering Information table
- Updated clocking diagram to include GPADC and ON timer0 clocks
- Updated BootROM flow chart in system's overview chapter
- Added Note about manual cold boot if power supply is less than 2.4V in the Power Management chapter
- Added Note on VBAT1V and VBAT3V voltage ramp up requirement in Absolute Maximum Ratings and increased max voltage levels to 3.6V
- Added Note on PSENS measurement details in specifications chapter **(only for FS!)**
- Added Near Field Mode on the features list and programming on the Specifications chapter

### 7.2 NON CRITICAL CHANGES

- Corrected TIM0\_CLK\_DIV register field description
- Corrected DEBUG\_REG bit 0 reset value

- Corrected reference to Direct Test Mode at chapter 24.6
- Changed OTP header regarding the sleep clock source flag
- Removed feature “Selectable Push-pull or open drain per pin” from the Input/Output ports chapter
- Added note at the end of chapter 18 about the watchdog operation in non-remapped systems.
- Merged various notes, in the specifications chapter
- Removed RCX frequency from Block Diagram
- Revised RCX parameters in specifications chapter and added note on maximum recommended connection interval time.
- Removed DCDC registers description.

## 8 V1.62 January 14 2013

### 8.1 CRITICAL CHANGES

- Changed status to “Preliminary”
- Updated Ordering Information table
- Added IQ Trim value in OTP header (0x4708)
- Added I<sub>BAT</sub>(EXT\_SLP)\_BOOST\_43KB and I<sub>BAT</sub>(EXT\_SLP)\_BUCK\_43KB in specifications chapter

### 8.2 NON CRITICAL CHANGES

- Corrected various typos in several sections
- Removed VPP\_EN from system diagrams
- Updated Retention RAM naming in the block diagram to follow the power domain naming (PD\_xx)
- Corrected current consumption of GP\_ADC to 5uA when rate at 100 ksamples

## 9 V1.61 December 5 2013

### 9.1 CRITICAL CHANGES

- Changed CLK\_16M\_REG[XTAL16\_BIAS\_SH\_DISABLE] to XTAL16\_BIAS\_SH\_ENABLE. Changed recommended usage in the register description (**Applies to ES4, FS document**)
- Changed the reset value of the CLK\_16M\_REG[XTAL16\_CUR\_SET] to 0x5 (**Applies to ES4, FS document**)
- Added Absolute Maximum Ratings table in the Specifications section
- Updated Specification tables with ES3 measured and characterized values

### 9.2 NON CRITICAL CHANGES

- Updated text in almost all sections regarding spelling or grammar mistakes
- Updated front page with correct number of available GPIOs for all packages

## 10 V1.50 September 6 2013

### 10.1 CRITICAL CHANGES

- Added 6KBytes of Retention RAM - 4 difference RAM cells. Total RAM size is now 50KB including SysRAM
- Changed BootROM code to search for specific values and not any values to identify the mode of operation (Normal, Development)
- Increased number of pads to support more GPIOs. QFN48 package is now also supported with 32 GPIOs. QFN40 and WLCSP34 remain unchanged
- Changed Baudrate of UART pin pairs while booting from UART in Development Mode
- Decreased power consumption in Extended Sleep mode
- Added a third Quadrature Decoder Axis for supporting the mouse scrolling wheel
- Added 3 extra PWM signals that can be mapped in any GPIO

- Added RCX oscillator with precision <500ppm and immune at temperature/voltage changes

#### 10.2 NON CRITICAL CHANGES

- Added ble\_rf\_diag interrupt for debugging capabilities
- Decreased XTAL Oscillator settle and trim time
- Added description for the General Purpose ADC
- Changed Booting flow charts for HW and SW (BootROM code)

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.