The D2-4P (D2-45057 and D2-45157) devices are complete System-on-Chip (SoC) Class-D digital audio amplifiers. These devices combine high performance integrated Power Stages, an optimized Audio Processor feature set, and a PWM controller to offer a complete, powerful, and very cost effective audio solution for high volume and cost-critical products.

This 4th generation Digital Audio Processor (D2-4P) device combines extensive integrated Digital Signal Processor (DSP) audio processing with amplifier control for a complete audio solution. Its ease of integration into the existing system processor provides complete support for all system product and amplifier functions.

The four configurable Power Stages operate as four separate Half-Bridge outputs, as two Full-Bridge outputs, or in combinations of Half-Bridge plus Full-Bridge, which provides flexible loudspeaker drive solutions. Separate PWM outputs provide additional combinations to drive headphone outputs or line level stereo and subwoofer outputs.

**Features**
- All digital Class-D amplifier and controller with integrated Digital Signal Processing (DSP)
- Four integrated Power Stages supporting:
  - 2 Channels, Bridged
  - 4 Channels, Half-Bridge
  - 2 Channels, Half-Bridge, plus 1 Channel, Bridged
- Output power (bridged):
  - 25 W (8 Ω, <1% THD); 30W (8 Ω, <10% THD)
- Fully programmable Digital Signal Processing (DSP)
  - Up to 5 programmable audio signal path channels
  - Programmable equalizers, filters, mixers, and limiters
- Includes D2 Audio DSP Sound Enhancement Algorithm and DTS® (SRS) WOW/HD™ Audio Enhancement Algorithms
- I2S and S/PDIF™ digital audio inputs
- Asynchronous sample rate converters; sample rates from 32kHz up to 192kHz
- Wide 9V to 26V Power Stage HV supply range, plus internally-generated gate drive supply
- Temperature and undervoltage monitoring and individual channel protection

**Applications**
- PC/multimedia speakers
- Digital TV audio systems
- Portable device docking stations
- Powered speaker systems

**Typical System Implementation**

![Diagram of a typical system implementation](image)

- **5-Channel PWM Engine**
- **24-Bit Digital Signal Processor**
- **2-Channel Sample Rate Converter**
- **Digital Audio Interface**
- **I2C Control Interface**
- **S/PDIF Digital I/O Interface**
- **SOC System Controller**
- **I2S Interface**
- **MOSFETs (Optional)**
- **Digital Audio Interface**
- **S/PDIF Digital I/O Interface**
- **Optical/Coax IN**
- **Optical/Coax OUT**
- **D2 Audio DSP Sound Enhancement Algorithm**
- **Third-Party Enhancements (SRS WOW/HD®)**
- **D2 Audio DSP Customization**
- **GUI**
- **PWM Output Drive**
- **Output Filter**
- **Amplifier Output 1**
- **Output Filter**
- **PWM Output Filter**
- **PWM Output Filter**
- **Stereo Line Out**
- **OR**
- **Headphone Out**
- **Subwoofer Line Out** (Optional)
- **Amplifier Output 2**
- **Amplifier Output 3**
- **Amplifier Output 4**
- **MOSFETs (Optional)**
- **SOC**
<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PART MARKING</th>
<th>AUDIO PROCESSING FEATURE SET SUPPORT</th>
<th>TEMP. RANGE (°C)</th>
<th>TAPE AND REEL (UNITS)</th>
<th>PACKAGE (RoHS Compliant)</th>
<th>PKG. DWG.</th>
</tr>
</thead>
<tbody>
<tr>
<td>D2-45057-QR</td>
<td>D2-45057-QR</td>
<td>D2 Audio DSP Sound Enhancement Algorithm</td>
<td>-10 to +85</td>
<td>68 Ld QFN L68.10 x 10 C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D2-45057-QR-T</td>
<td>D2-45057-QR</td>
<td>D2 Audio DSP Sound Enhancement Algorithm</td>
<td>-10 to +85</td>
<td>3k 68 Ld QFN L68.10 x 10 C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D2-45157-QR</td>
<td>D2-45157-QR</td>
<td>D2 Audio DSP Sound Enhancement Algorithm DTS® (SRS) WOW/HD™</td>
<td>-10 to +85</td>
<td>68 Ld QFN L68.10 x 10 C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D2-45157-QR-T</td>
<td>D2-45157-QR</td>
<td>D2 Audio DSP Sound Enhancement Algorithm DTS® (SRS) WOW/HD™</td>
<td>-10 to +85</td>
<td>3k 68 Ld QFN L68.10 x 10 C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1. The D2-4P devices support audio processing algorithms for the D2 Audio DSP Sound Enhancement Algorithm and DTS® (SRS) WOW/HD™ audio enhancement features. Algorithm support for these enhancements is device-dependent. See the device part number for feature support.
2. See TB 347 for details about reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. The Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
4. For Moisture Sensitivity Level (MSL), see the D2-45057 and D2-45157 device pages. For more information about MSL, see TB363.
Absolute Maximum Ratings

**Supply Voltage**
- HVDD[A:D], VDDHV: -0.3V to +28.0V
- RVDD, PWMVDD: -0.3V to 4.0V
- CVDD, PLLVDD: -0.3V to 2.4V

**Input Voltage**
- Any Input but XTALI: -0.3V to RVDD +0.3V
- XTALI: -0.3V to PLLVDD +0.3V

**Input Current, Any Pin but Supplies**
\[ ±10mA \]

**Thermal Resistance (Typical)**
- \( \theta_{JA} \) (°C/W): 68 Ld QFN Package (Notes 5, 6): 25 1
- \( \theta_{JC} \) (°C/W):

**Maximum Storage Temperature**
- -55°C to +150°C

**Pb-Free Reflow Profile**
- see TB493

**Recommended Operating Conditions**
- **Temperature Range**: -10°C to +85°C
- **High Voltage Supply Voltage**, HVDD[A:D], VDDHV: 9.0V to 26.5V
- **Digital I/O Supply Voltage**, PWMVDD: 3.3V
- **Core Supply Voltage**, CVDD: 1.8V
- **Analog Supply Voltage**, PLLVDD: 1.8V
- **Minimum Load Impedance** (HVDD[A:D] ≤ 24.0V), \( Z_L \): 4Ω

**CAUTION**: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

**NOTES:**
- 5. \( \theta_{JA} \) is measured in free air with the component mounted on a high-effectiveness thermal conductivity test board with "direct attach" features. See TB379.
- 6. For \( \theta_{JC} \), the "case temp" location is the center of the exposed metal pad on the package underside.
- 7. Absolute Maximum parameters are not tested in production.

### Electrical Specifications

**TA = + 25 °C**, HVDD[A:D]/VDDHV = 24 V, CVDD = PLLVDD = 1.8V ± 5%, RVDD = PWMVDD = 3.3V ±10%.

#### TEST CONDITIONS SYMBOL MIN TYP MAX UNIT

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Input High Logic Level (Note 8)</td>
<td></td>
<td>VIH</td>
<td>2-</td>
<td>-</td>
<td>-V</td>
</tr>
<tr>
<td>Digital Input Low Logic Level (Note 8)</td>
<td></td>
<td>VIL</td>
<td>-</td>
<td>-</td>
<td>0.8V</td>
</tr>
<tr>
<td>High Level Output Drive Voltage (IOUT at - Pin Drive Strength Current)</td>
<td></td>
<td>VOH</td>
<td>RVDD</td>
<td>-</td>
<td>0.4V</td>
</tr>
<tr>
<td>Low Level Output Drive Voltage (IOUT at + Pin Drive Strength Current)</td>
<td></td>
<td>VOL</td>
<td></td>
<td>-</td>
<td>0.4V</td>
</tr>
<tr>
<td>High Level Input Drive Voltage XTALI Pin</td>
<td></td>
<td>VIHX</td>
<td></td>
<td>0.7</td>
<td>PLLVDDV</td>
</tr>
<tr>
<td>Low Level Input Drive Voltage XTALI Pin</td>
<td></td>
<td>VILX</td>
<td></td>
<td>-</td>
<td>0.3V</td>
</tr>
<tr>
<td>Input Leakage Current (Note 9)</td>
<td></td>
<td>IIN</td>
<td></td>
<td>±</td>
<td>10μA</td>
</tr>
<tr>
<td>Input Capacitance CIN</td>
<td></td>
<td></td>
<td></td>
<td>9</td>
<td>-pF</td>
</tr>
<tr>
<td>Output Capacitance All Outputs Except OUT[A:D] COUNT</td>
<td></td>
<td></td>
<td></td>
<td>-9</td>
<td>-pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>OUT[A:D]</td>
<td>190</td>
</tr>
<tr>
<td>nRESET Pulse-Width tRST</td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>-ns</td>
</tr>
<tr>
<td>Internal Pull-Up Resistance to PWMVDD (for nERROR 0-3, OCFG, nPDN)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-100k</td>
</tr>
<tr>
<td>Digital I/O Supply Pin Voltage, Current RVDD and PWMVDD</td>
<td></td>
<td></td>
<td></td>
<td>3.3</td>
<td>3.6V</td>
</tr>
<tr>
<td>Active Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10mA</td>
</tr>
<tr>
<td>Power-Down Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.01mA</td>
</tr>
<tr>
<td>Core Supply Pins CVDD</td>
<td></td>
<td></td>
<td></td>
<td>1.7</td>
<td>1.8</td>
</tr>
<tr>
<td>Active Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>300mA</td>
</tr>
<tr>
<td>Power-Down Current (Note 10)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-6mA</td>
</tr>
</tbody>
</table>
Analog Supply Pins (PLL) PLL VDD 1.7 1.8 1.9 V
Active Current - 10 mA
Power-Down Current (Note 10) -5 mA
CRYSTAL OSCILLATOR
Crystal Frequency (Fundamental Mode Crystal) Xo 20 24.576 25 MHz
Duty Cycle Dt 40 - 60%
Start-Up Time (Start-Up Time is Oscillator Enabled (with Valid Supply) to Stable Oscillation) tSTART -5 20 ms
PLL
VCO Frequency FVCO 2 40 2 94.9 12 300 MHz
PLL Lock Time from any Input Change - 3 ms
1.8V POWER-ON RESET
Reset Enabled Voltage Level VEN 0.95 1.1 1.3 V
POR Minimum Output Pulse Width tDIS -5 µs
1.8 V BROWNOUT DETECTION
Detect Level 1.4 1.5 1.7 V
Pulse-Width Rejection tBOD1 -100 ns
Minimum Output Pulse-Width tO1 -20 ns
3.3 V (PWMVD) BROWNOUT DETECTION
Detect Level 2.5 2.7 2.9 V
Pulse-Width Rejection tBOD3 -100 ns
Minimum Output Pulse-Width tO3 -20 ns
GATE DRIVE INTERNAL +5V BROWNOUT DETECTION
Gate Drive Supply Undervoltage Threshold - 4.5 V
Gate Drive Supply Undervoltage Threshold Hysteresis - 200 mV
Gate Drive Supply Undervoltage Threshold Glitch Rejection - 50 ns
PROTECTION DETECT
High Voltage (+VDD HV) Undervoltage Protection - 79 V
Over current Trip Threshold - 4 A
Over current De-Glitch - 2.5 ns
Short-Circuit Current Limit (Peak) - 8 A
Over current Response Time - 20 ns
Thermal Shutdown (Power Stages) - 140 °C
Thermal Shutdown Hysteresis (Power Stages) - 30 °C

NOTES:
8. All input pins except XTALI.
9. Input leakage applies to all pins except XTAL O.
10. Power-down is with device in reset and clocks stopped.

Electrical Specifications
TA = +25 °C, HVDD [A:D]/VDDHV = 24 V, CVDD = PLL VDD = 1.8V ± 5%, RVDD = PW MVDD = 3.3 V ±10 %.
All grounds at 0.0 V. All voltages referenced to ground. PLL at 294.912 MHz, OSC at 24.576 MHz, core running at 147.456 MHz with typical audio data traffic.

PARAMETER
TEST CONDITIONS SYMBOL MIN TYP MAX UNIT
Performance Specifications

TA = +25°C, HVDD[A:D]/VDDHV = 24 V, CVDD = PLLVDD = 1.8 V ±5%, RVDD = PWMVDD = 3.3 V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576 MHz, core running at 147.456 MHz with typical audio data traffic.

<table>
<thead>
<tr>
<th>Parameter Symbol</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>rDS(ON) (MOSFETs at +25°C)</td>
<td>-200</td>
<td>-</td>
<td>Ω</td>
</tr>
<tr>
<td>rDS(ON) Mismatch</td>
<td>-1</td>
<td>-</td>
<td>%</td>
</tr>
<tr>
<td>PWM Switching Rate</td>
<td>-384</td>
<td>-</td>
<td>kHz</td>
</tr>
<tr>
<td>nPDN Input Off Delay tPDNOFF</td>
<td>-1.4</td>
<td>-</td>
<td>ms</td>
</tr>
<tr>
<td>nPDN Input On Delay tPDNON</td>
<td>-1.4</td>
<td>-</td>
<td>ms</td>
</tr>
</tbody>
</table>

Power Output

- <1% THD, Bridged, Load = 8Ω, HVDD[A:D] = 24V, POUT = -25 - W
- <10% THD, Bridged, Load = 8Ω, HVDD[A:D] = 24V, POUT = -30 - W
- <1% THD, Half-Bridge, Load = 8Ω, HVDD[A:D] = 24V, POUT = -7 - W
- <10% THD, Half-Bridge, Load = 8Ω, HVDD[A:D] = 24V, POUT = -9 - W

THD+N

- Load = 8Ω, Power = 25 W, Bridged, 1kHz, THD+N = 0.3% |
- Load = 8Ω, Power = 1W, Bridged, 1kHz, THD+N = 0.05%

SNR

- SNR = 110 dB

Efficiency (Power Stage, Load = 8Ω)

- Efficiency = 90%
Two-Wire (I2C) Interface Port Timing

<table>
<thead>
<tr>
<th>Symbol Description</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fSCL</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>tbuf</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>twlowSCLx</td>
<td></td>
<td>4.7</td>
<td>µs</td>
</tr>
<tr>
<td>twhighSCLx</td>
<td></td>
<td>4.0</td>
<td>µs</td>
</tr>
<tr>
<td>tsSTA</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>thSTA</td>
<td>4.0</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>thSDAx</td>
<td>1</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tsSDAx</td>
<td>250</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tdSDAx</td>
<td>3.5</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tr</td>
<td></td>
<td>-1</td>
<td>µs</td>
</tr>
<tr>
<td>tf</td>
<td></td>
<td>-300</td>
<td>ns</td>
</tr>
<tr>
<td>tsSTO</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

NOTES:
11. Data is clocked in as valid on the next XTALI rising edge after SCL goes low.
12. Limits established by characterization and not production tested.
### SPI™ Master Mode Interface Port Timing

$\text{TA} = +25 \, ^\circ\text{C}, \text{CVDD = PLLVDD = 1.8 V \pm 5\%}, \text{RVDD = PWMVDD = 3.3 V \pm 10\%}$. All grounds at 0.0V. All voltages referenced to ground.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DESCRIPTION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{V\text{MO}}$</td>
<td>M0I Valid From Clock Edge</td>
<td>-8 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{S\text{MI}}$</td>
<td>M0I Setup to Clock Edge</td>
<td>10 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{H\text{MISO}}$</td>
<td>Hold From Clock Edge</td>
<td>system clock + 2ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{WI\text{nSS}}$</td>
<td>Minimum Width</td>
<td>3 system clocks + 2ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### SPI™ Slave Mode Interface Port Timing

$\text{TA} = +25 \, ^\circ\text{C}, \text{CVDD = PLLVDD = 1.8 V \pm 5\%}, \text{RVDD = PWMVDD = 3.3 V \pm 10\%}$. All grounds at 0.0V. All voltages referenced to ground.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DESCRIPTION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{V\text{MI}}$</td>
<td>M0I Valid From Clock Edge</td>
<td>3 system clocks + 2ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{S\text{MO}}$</td>
<td>M0I Setup to Clock Edge</td>
<td>10 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{H\text{MOSI}}$</td>
<td>Hold From Clock Edge</td>
<td>system clock + 2ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{WI\text{nSS}}$</td>
<td>Minimum Width</td>
<td>3 system clocks + 2ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SCK (CPHA = 1, C POL = 0)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSI</td>
<td></td>
</tr>
<tr>
<td>nSS</td>
<td></td>
</tr>
</tbody>
</table>

SCK (CPHA = 0, C POL = 0)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MISO (CPHA = 0)</td>
<td></td>
</tr>
</tbody>
</table>
## Pin Descriptions

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>TYPE</th>
<th>VOLTAGE LEVEL (V)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>nRESET</td>
<td>I/3.3</td>
<td>Active low reset input with hysteresis. A low level activates a system level reset, which initializes all internal logic and program operations. The system latches the boot mode selection on the IRQ input pins on the rising edge.</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>TEMP/COM/TIO0</td>
<td>O</td>
<td>3.3</td>
<td>Board temperature monitor common I/O pin. Provides 16mA drive strength when operating as an output.</td>
</tr>
<tr>
<td>3</td>
<td>SDA</td>
<td>I/O</td>
<td>3.3</td>
<td>Two-wire serial data port, open drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport. Pin floats on reset.</td>
</tr>
<tr>
<td>PIN</td>
<td>PIN NAME</td>
<td>TYPE</td>
<td>VOLTAGE LEVEL (V)</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>-------</td>
<td>-----------------</td>
<td>------</td>
<td>-------------------</td>
<td>-------------</td>
</tr>
<tr>
<td>4</td>
<td>SCL I/O 3.3</td>
<td>Two-wire serial clock port, open drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for clock signaling. Pin floats on reset.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>SCLK I/O 3.3</td>
<td>I2S serial audio bit clock (SCLK) Input. Input has hysteresis.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>DIN I/O 3.3</td>
<td>I2S serial audio data (SDIN) Input. Input has hysteresis.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>LRCK I/O 3.3</td>
<td>I2S serial audio left/right (LRCK) Input. Input has hysteresis.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>MCLK O 3.3</td>
<td>I2S serial audio master clock output for external ADC/DAC components, drives low on reset. Output is an 8mA driver.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>CVDD P 3.3</td>
<td>Core power, +1.8VDC. Used in the chip internal DSP, logic, and interfaces.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>CGND GND 3.3</td>
<td>Core ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>RGND GND 3.3</td>
<td>Digital pad ringing ground. Internally connected to PWMGND.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>RVDD P 3.3</td>
<td>Digital pad ringing power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Both of these pins must be connected. Internally connected to PWMVDD.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>TEMPREF/SCK I/O 3.3</td>
<td>Reference pin for the temperature monitor and SPI clock. At deassertion of device reset, this pin operates as a SPI clock with 8mA drive strength. Upon internal D2-4P firmware execution, this pin becomes a temperature monitor reference.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>nMUTE/TIO1 O 3.3</td>
<td>Mute signal output. When active low, a mute condition drives this pin low. The output is a 16mA driver. Initializes as an input at reset, then becomes an output upon internal firmware execution.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>VOL1/MISO I/O 3.3</td>
<td>Volume control pulse input and SPI master-input/slave-output data signal. At deassertion of device reset, this pin operates as a SPI master input or slave output (when operating as an output, provides 4mA drive strength). At internal D2-4P firmware execution, this pin becomes an input for monitoring up/down phase pulses from volume control (one of two volume input pins).</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>TEMP1/MOSI I/O 3.3</td>
<td>Board temperature monitor pin and SPI master-output/slave-input data signal. At deassertion of device reset, this pin operates as a SPI master output or slave input (when operating as an output, provides 4mA drive strength). At internal D2-4P firmware execution, this pin becomes an input for monitoring board temperature.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>SPDIFRX I/O 3.3</td>
<td>S/PDIF digital audio data input.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>SPDIFTX O 3.3</td>
<td>S/PDIF digital audio data output. This pin is the S/PDIF audio output and drives an 8mA, 3.3V stereo output up to 192kHz. Pin floats on reset.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>TEST I 3.3</td>
<td>Hardware test mode control. For factory use only. Must be tied low.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>IRQA I 3.3</td>
<td>Interrupt request port A. One of two IRQ pins, tied to logic (3.3V) high or to ground. High/low logic status establishes the boot mode selection upon deassertion of the reset (nRESET) cycle.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>IRQB I 3.3</td>
<td>Interrupt request port B. One of two IRQ pins, tied to logic (3.3V) high or to ground. High/low logic status establishes the boot mode selection upon deassertion of the reset (nRESET) cycle.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>RGND GND 3.3</td>
<td>Digital pad ringing ground. Internally connected to PWMGND.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>nERROR/CFG0 I/O 3.3</td>
<td>Output configuration selection input and nERROR output. At device reset, this pin operates as an input and uses an application-installed pull-up or pull-down connection to the pin to specify one of four amplifier configurations. At internal D2-4P firmware execution, this pin becomes an output and provides an active-low output drive when amplifier protection monitoring detects an error condition. When operating as an output, this pin provides 4mA drive strength. Note: This pin may also be called “PSCURR” on some reference designs. Function is identical regardless of name.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>PS SYNC/CFG1 I/O 3.3</td>
<td>Output configuration selection input and power supply sync output. At device reset, this pin operates as an input and uses an application-installed pull-up or pull-down connection to the pin to specify one of four amplifier configurations. At internal D2-4P firmware execution, this pin becomes an output and provides a synchronizing signal to on-board power supply circuits. When operating as an output, this pin provides 4mA drive strength. Note: This pin may also be called “PSTEMP” on some reference designs. Function is identical regardless of name.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>PROTECT0 I/O 3.3</td>
<td>PWM protection input. Input has hysteresis. This pin's protection monitoring functionality is controlled by internal D2-4P firmware and is dependent on which of the four amplifier configurations is enabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIN</td>
<td>NAME</td>
<td>TYPE</td>
<td>VOLTAGE LEVEL (V)</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>-----</td>
<td>------</td>
<td>------</td>
<td>-------------------</td>
<td>-------------</td>
</tr>
<tr>
<td>27</td>
<td>PROTECT1</td>
<td>I/O</td>
<td>3.3</td>
<td>PWM protection input. Input has hysteresis. This pin's protection monitoring functionality is controlled by internal D2-4P firmware and is dependent on which of the four amplifier configurations is enabled.</td>
</tr>
<tr>
<td>28</td>
<td>PROTECT2</td>
<td>I/O</td>
<td>3.3</td>
<td>PWM protection input. Input has hysteresis. This pin's protection monitoring functionality is controlled by internal D2-4P firmware and is dependent on which of the four amplifier configurations is enabled.</td>
</tr>
<tr>
<td>29</td>
<td>ERROR0</td>
<td>O</td>
<td>3.3</td>
<td>Overcurrent protection output, channel A output stage. Open drain 16mA driver with internal 100kΩ pull-up (approximate). Pulls low when active from overcurrent detection of the output stage.</td>
</tr>
<tr>
<td>30</td>
<td>ERROR1</td>
<td>O</td>
<td>3.3</td>
<td>Overcurrent protection output, channel B output stage. Open drain 16mA driver with internal 100kΩ pull-up (approximate). Pulls low when active from overcurrent detection of the output stage.</td>
</tr>
<tr>
<td>31</td>
<td>ERROR2</td>
<td>O</td>
<td>3.3</td>
<td>Overcurrent protection output, channel C output stage. Open drain 16mA driver with internal 100kΩ pull-up (approximate). Pulls low when active from overcurrent detection of the output stage.</td>
</tr>
<tr>
<td>32</td>
<td>ERROR3</td>
<td>O</td>
<td>3.3</td>
<td>Overcurrent protection output, channel D output stage. Open drain 16mA driver with internal 100kΩ pull-up (approximate). Pulls low when active from overcurrent detection of the output stage.</td>
</tr>
<tr>
<td>33</td>
<td>HVDDD</td>
<td>P</td>
<td>HV</td>
<td>Output stage D high voltage supply power. A separate power pin connection is provided for each of the output stages. All of the HVDD[A:D] pins and the VDDHV pin connect to the system “HV” power source.</td>
</tr>
<tr>
<td>34</td>
<td>HGNDG</td>
<td>GND</td>
<td>HV</td>
<td>Output stage D high voltage supply ground. A separate ground pin connection is provided for each of the output stages. All of the HGND[A:D] pins connect to system “HV” power ground (see Note 15).</td>
</tr>
<tr>
<td>35</td>
<td>OUTD</td>
<td>O</td>
<td>HV</td>
<td>PWM power amplifier output, channel D.</td>
</tr>
<tr>
<td>36</td>
<td>HSBSD</td>
<td>I</td>
<td>HV</td>
<td>High-side bootstrap input, output channel D. Capacitor couples to OUTD amplifier output.</td>
</tr>
<tr>
<td>37</td>
<td>HSBSC</td>
<td>I</td>
<td>HV</td>
<td>High-side bootstrap input, output channel C. Capacitor couples to OUTC amplifier output.</td>
</tr>
<tr>
<td>38</td>
<td>OUTC</td>
<td>O</td>
<td>HV</td>
<td>PWM power amplifier output, channel C.</td>
</tr>
<tr>
<td>39</td>
<td>HGNDG</td>
<td>GND</td>
<td>HV</td>
<td>Output stage C high voltage supply ground. A separate ground pin connection is provided for each of the output stages. All of the HGND[A:D] pins connect to system “HV” power ground (see Note 15).</td>
</tr>
<tr>
<td>40</td>
<td>HVDDC</td>
<td>P</td>
<td>HV</td>
<td>Output stage C high voltage supply power. A separate power pin connection is provided for each of the output stages. All of the HVDD[A:D] pins and the VDDHV pin connect to the system “HV” power source. The internal +5V supply regulators also operate from this VDDHV input.</td>
</tr>
<tr>
<td>41</td>
<td>SUBOUT</td>
<td>O</td>
<td>3.3</td>
<td>“Subwoofer” channel PWM output with 16mA drive strength. Connects to filter network for supplying line-level analog output to subwoofer.</td>
</tr>
<tr>
<td>42</td>
<td>DNC</td>
<td>-</td>
<td>-</td>
<td>Do not connect to this pin.</td>
</tr>
<tr>
<td>43</td>
<td>IREFI</td>
<td>O</td>
<td>-</td>
<td>Overcurrent reference analog input. Used in setting the overcurrent error detect externally - set the threshold. The pin needs to be connected to a 100kΩ resistor to ground to set the overcurrent threshold according to the specified limits.</td>
</tr>
<tr>
<td>44</td>
<td>VDDHV</td>
<td>P</td>
<td>+HV</td>
<td>High voltage internal driver supply power. All of the HVDD[A:D] pins and the VDDHV pin connect to the system “HV” power source.</td>
</tr>
<tr>
<td>45</td>
<td>REG5V</td>
<td>P</td>
<td>5</td>
<td>5V internal regulator filter connect. A +5V supply is internally generated from the voltage source provided at the VDD pin. REG5V is used for external connection of decoupling capacitors.</td>
</tr>
<tr>
<td>46</td>
<td>HVDBB</td>
<td>P</td>
<td>HV</td>
<td>Output stage B high voltage supply power. A separate power pin connection is provided for each of the output stages. All of the HVDD[A:D] pins and the VDDHV pin connect to the system “HV” power source.</td>
</tr>
<tr>
<td>47</td>
<td>HGNDG</td>
<td>GND</td>
<td>HV</td>
<td>Output stage B high voltage supply ground. A separate ground pin connection is provided for each of the output stages. All of the HGND[A:D] pins connect to system “HV” power ground (see Note 15).</td>
</tr>
<tr>
<td>48</td>
<td>OUTB</td>
<td>O</td>
<td>HV</td>
<td>PWM power amplifier output, channel B.</td>
</tr>
<tr>
<td>49</td>
<td>HSBSB</td>
<td>I</td>
<td>HV</td>
<td>High-side bootstrap input, output channel B. The capacitor couples to the OUTB amplifier output.</td>
</tr>
<tr>
<td>50</td>
<td>HSBSA</td>
<td>I</td>
<td>HV</td>
<td>High-side bootstrap input, output channel A. The capacitor couples to the OUTA amplifier output.</td>
</tr>
<tr>
<td>51</td>
<td>OUTA</td>
<td>O</td>
<td>HV</td>
<td>PWM power amplifier output, channel A.</td>
</tr>
<tr>
<td>52</td>
<td>HGNDG</td>
<td>GND</td>
<td>HV</td>
<td>Output stage A high voltage supply ground. A separate ground pin connection is provided for each of the output stages. All of the HGND[A:D] pins connect to system “HV” power ground (see Note 15).</td>
</tr>
</tbody>
</table>
53 HVDD A P HV Output stage A high voltage supply power. A separate power pin connection is provided for each of the output stages. All of the HVDD [A:D] pins and the VDDH pin connect to the system "HV" power source.

54 nPDN I 3.3 Power-down and mute input. Active low. When this input is low, all four outputs become inactive and their output stages float, and their output is muted. Internal logic and other references remain active during this power-down state.

55 LINER O 3.3 "Right" channel PWM output, with 16mA drive strength. Connects to the filter network to supply the line-level analog output.

56 LINEL O 3.3 "Left" channel PWM output, with 16mA drive strength. Connects to the filter network to supply the line-level analog output.

57 OCFG1 I 3.3 Output configuration control select. OCFG0 and OCFG1 are logic inputs to select the output configuration mode of the output stages. Connects to either the PWMGND ground or PWMVDD (+3.3V) through a nominal 10kΩ resistor to select output configuration.

58 OCFG0 I 3.3 Output configuration control select. OCFG0 and OCFG1 are logic inputs to select the output configuration mode of the output stages. Connects to either the PWMGND ground or PWMVDD (+3.3V) through a nominal 10kΩ resistor to select output configuration.

59 PWMGND P 3.3 PWM output pin ground. Internally connected to RGND.

60 PWMVDD P 3.3 PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.

61 PLLGND P 1.8 PLL analog ground. Tie to a low voltage ground (CGND, RGND) through a single point connection to isolate ground noise on the board and minimize effects on the PLL.

62 XTALI P 1.8 Crystal oscillator analog input port.

63 XTALO P 1.8 Crystal oscillator analog output port (this output drives the crystal and XTALO does not have a drive strength specification).

64 PLLVDD P 1.8 PLL analog power, 1.8V.

65 VOL0 /nSS I/O 3.3 Volume control pulse input and SPI slave select. When device reset is deasserted, this pin operates as a SPI slave select input. At internal D2-4P firmware execution, this pin becomes an input for monitoring up/down phase pulses from volume control (one of two volume input pins.)

66 CGND P 1.8 Core ground

67 CVDD P 1.8 Core power, +1.8VDC. Used in the chip internal DSP, logic, and interfaces.

68 nRSTOUT O 3.3 Active low open-drain output with 16mA drive strength. This pin drives low when either the RVDD 3.3V brownout detector, PWMVDD 3.3V brownout detector, or 1.8V brownout detector goes active. Use this output to initiate a system reset to the nRESET pin upon brownout event detection.

NOTES:

13. All pin names are active high unless otherwise specified. Active low pins have an "n" prefix, such as nRESET.

14. All power and ground pins with the same names must be tied together to all other pins of their same name (that is, tie CVDD pins together, CGND pins together, RVD D pins together, and RG ND pins together). Tie CGND and RG ND together on the board and ensure the RGND and PWMGND pins are internally connected and tied together on the board.

15. The thermal pad is internally connected to all four HGND ground pins (HGNDA, HGNDB, HGNDC, and HGNDD). Any connection to the thermal pad must be made to the common ground for these four ground pins.
Typical Performance Characteristics

• Typical performance measurements are made using an Audio Precision™ 2700 Series audio analyzer.
• Precision power resistors are used for the 8Ω loudspeaker loads.
• Measurements are done using a +HV supply of +24.0VDC.

Full-Bridge Typical Performance Curves

FIGURE 5. THD vs POWER, FULL-BRIDGE
FIGURE 6. THD vs FREQUENCY, FULL-BRIDGE
FIGURE 7. FREQUENCY RESPONSE, FULL-BRIDGE
FIGURE 8. NOISE FLOOR, FULL-BRIDGE

0.01 1.00 0.02 0.05 0.10 0.20 0.50 1.00 2.00 5.00
THD (%)

0.06500.10.20.51.251.0
POWER (W)

HVDD = 24.0V, 8Ω LOAD, 1 kHz

0.001 1.000 0.002 0.005 0.010 0.020 0.050 0.100 0.200 0.500 20 20k 50 100 200 500 1k 2k 5k
FREQUENCY (Hz)

P = 25W

P = 14W

P = 7W

P = 1W

HVDD = 24.0V, 8Ω LOAD, AT 1W, 7W, 14W, 25W POWER OUT

-6 6 -5 -4 -3 -2 -1 0 1 2 3 4

THD (%)

HVDD = 24.0V, 8Ω LOAD, 3.5W


dB

dB A

FREQUENCY (Hz)

HVDD = 24.0V, 8Ω LOAD,

< -115dB, UNWEIGHTED

HVDD = 24.0V, 8Ω LOAD,

AT 1kHz, REFERENCE TO 30W
Half-Bridge Typical Performance Curves

FIGURE 9. THD vs POWER, HALF-BRIDGE
FIGURE 10. THD vs FREQUENCY, HALF-BRIDGE
FIGURE 11. FREQUENCY RESPONSE, HALF-BRIDGE
FIGURE 12. NOISE FLOOR, HALF-BRIDGE

THD (%)

POWER (W)

0.02
0.05
0.10
0.20
0.50
1.00
2.00
5.00

0.06 200.1 0.2 0.5 1 2 5 10

HVDD = 24.0V, 8Ω LOAD, 1 kHz

FREQUENCY (Hz)

THD (%)

0.001
0.002
0.005
0.010
0.020
0.050
0.100
0.200
0.500

2 0 20k50 100 200 500 1k 2k 5k 10k

HVDD = 24.0V, 8Ω LOAD, 2.4W POWER OUT

-1 2

12

-1 0

-8

-6

-4

-2

-0 2

4

6

8

10

20 20k 50 100 200 50 0 1k 2k 5k 10k

DC RESPONSE WITHOUT AC RESPONSE DUE TO LOUDSPEAKER

DC BLOCKING CAPACITOR

dBr A

FREQUENCY (Hz)

HVDD = 24.0V, 8Ω LOAD, 1W

-125

-30

-120

-115

-110

-105

-100

-95

-90

-85

-45

-40

-35

-60

+0

-55

-50

-45

-40

-35

-30

-25

-20

-15

-10

-5

-80

-75

-70

-65

-60

-55

-50

-45

-40

-35

-30

-25

-20

-15

-10

-5

-0

< -110dB, UNWEIGHTED

NOISE FLOOR AT 1kHz, +24V RAIL, SPDIF INPUT, 8Ω LOAD, UNITY DSP GAIN
The D2-4P devices, shown in Figure 13 on page 15, are integrated System-on-Chip (SoC) audio processors and Class D digital audio amplifiers. They include digital audio input selection, signal routing, complete audio processing, PWM controllers, amplifier and protection control, and integrated power stages. Stereo I2S and S/PDIF Digital input support, plus I2C and 2-wire SPI control interfaces, provide integration compatibility with existing system architectures and solutions.

The four configurable power stages can operate as four separate Half-Bridge outputs, as two Full-Bridge outputs, or in combinations of Half-Bridge plus Full-Bridge outputs. Separate PWM outputs provide additional combinations to drive headphone outputs or line-level stereo and subwoofer outputs. These application-dependent configurations provide for driving Stereo (2.0) Speaker, 2.1 Speaker, and Stereo (2.2) Bi-Amp Speaker solutions, as well as providing Stereo Line outputs, Headphone outputs, or Subwoofer line outputs.

Audio output implementations are defined by the configuration mode select pins and provide four combinations of powered and line amplifier outputs as shown in Table 1.

<table>
<thead>
<tr>
<th>CONFIGURATION MODE NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
</table>
| 02.0 L/R 4-Quadrant | • Powered left and right outputs with 4-quadrant, full bridge drivers  
| 12.0 L/R + L/R/Sub Line | • Powered left and right outputs with 2-quadrant, full bridge drivers  
| 22.1 L/R/Sub + L/R Line | • Two half bridge drivers for powered left and right outputs  
| 32.2 Bi-Amp | • Four half bridge drivers for powered bi-amp left + right outputs  

Audio path includes a stereo Sample Rate Converter (SRC), five independent audio processing channels, and device-specific audio enhancement algorithms. Programmable parameter settings for audio processing include volume control, path routing and mixing, high/low pass filtering, multi-band equalizers, compressors, and loudness. These parameters can be adjusted using the D2 Audio Customization GUI, or can be set by a system/amplifier microcontroller through the D2-4P's control interface.

Audio Enhancement Features

The D2-4P family devices include the D2 Audio DSP Sound Enhancement Algorithm or DTS® (SRS) WOW/HD™ audio enhancement algorithms. These device-specific functions are integrated within the firmware as part of the standard audio processing signal flow and are supported per device as:

- D2 Audio sound enhancement algorithm (Included in the D2-45057 device)
  - 2-channel stereo spatialization
  - Bass enhancement
  - Content/configuration EQ presets
  - Improved vocal clarity
  - Automatic room audio setup/equalization/optimization
  - Automatic loudspeaker setup/equalization/correction
  - DTS® (SRS) WOW/HD™

Each of these enhancements uses its own algorithms, where choice of enhancement is specified by device part number. The D2-45057 includes only D2 Audio DSP Sound Enhancement Algorithm support, and the D2-45157 includes only DTS® (SRS) WOW/HD™ support. These enhancements also have their own unique set of programmable parameters to control operation.

Serial Audio Digital Input

The D2-4P devices include one Serial Audio Interface (SAI) port that accommodates two digital audio input channels. The SAI port operates in slave mode only, supports the I2S digital audio industry standard, and can carry up to 24-bit Linear PCM audio words.

The digital audio input from the SAI input port routes directly through the Sample Rate Converters (SRC). Either the I2S digital input or the S/PDIF Digital input can be selected as the audio path source.

S/PDIF Digital Audio I/O

The D2-4P devices contain one IEC60958 compliant S/PDIF Digital receiver input and one IEC60958 compatible S/PDIF Digital transmitter.

The S/PDIF Digital receiver input includes an input transition detector, digital PLL clock recovery, and a decoder to separate the audio data. The receiver meets the jitter tolerance specified in IEC60958-4.
The S/PDIF Digital transmitter complies with the consumer applications defined in IEC60958-3. The transmitter supports 24-bit audio data, but does not support user data and channel status.

Compressed digital formats are not decoded within the D2-45057 and D2-45157. However, a bit-exact pass-through mode is supported from the SPDIFRX input to the SPDIFTX output, which allows for designs that require IEC61937-compliant original compressed audio input bitstream be made available at the product’s S/PDIF Digital output.

Sample Rate Converter

The D2-4P devices contain a 2-channel asynchronous Sample Rate Converter (SRC) within the audio input signal flow path. The SRC converts audio data input sampled at one input sample rate to a fixed 48kHz output sample rate, which aligns asynchronous input audio streams to a single rate for system processing.

Audio data presented to the SRC can be from either the SAI or S/PDIF Digital input sources with an input sample rate from 16kHz to 192kHz. In addition to converting the input sample rate to the output sample rate, input clock jitter and sampling jitter is attenuated by the SRC to further enhance audio quality.

DSP

A 24-bit fixed-point Digital Signal Processor (DSP) controls the majority of audio processing and system control functions on the D2-4P. Audio path signal routing, programmable-parameter processing blocks, and control logic are defined within the device’s internal firmware. Signal flows through the device are buffered and processed through hardware specific-function blocks such as the SRC. Internal device registers allow full integration of DSP control with the internal ROM-based firmware, as well as providing for external control of audio processing parameters.

Clock and PLL

Clocks are generated on-chip using a fundamental-mode crystal connected across the XTALI and XTALO pins. XTALO is an output, but it is designed only to drive the crystal and does not connect to any other circuit. XTALI is an input that connects to the other side of the crystal.

The clock generation contains a low jitter PLL to ensure low noise PWM output and a precise master clock source for sample rate conversion and the audio processing data paths. The internal PLL’s VC0 clock operates at 12x the crystal frequency (12 x 24.576MHz) and provides complete device and system timing reference. It is used throughout the device, including clock generators for brownout detection, system and power-on reset, DSP, S/PDIF Digital transmitter, and PWM engine timing.

Clock and PLL hardware functions are controlled by internal device firmware. They are not programmable and are optimized for device and system operation.

Timers

Two independent timers are used for device and system control. One timer is used for internal references for chip-specific operations. The other is used for the system/board temperature sensing control algorithm. Two I/O pins (TIO0 and TIO1) are associated with the timers. Their pin functions are defined by the device firmware. Only TIO0 is actually used in relationship to its timer, Timer 0, and operates the timing-related I/O functions of the temperature monitoring algorithm. Timer 1 is used for internal functions of the device. Its pin (TIO1) is not used for this timing operation and is defined by device firmware as the nMUTE input pin.

Audio Outputs

Audio outputs are provided through four output power stages that are configurable for driving loudspeakers. Three additional PWM outputs are also available for driving line-level audio outputs. Combinations of outputs and their audio processing channel assignment are defined by the device’s configuration mode settings.

Output Power Stages

The devices include four independent output stages (Figure 14) that are each implemented using a high-side (to positive HVDD supply) and a low-side (to HV supply ground) FET pair. Drivers and overcurrent monitoring are included in each of these four output stages. Depending on the selected configuration mode, these four stages can be used independently as single half-bridge outputs or as pairs for full-bridge outputs.

Audio processing PWM channel outputs are routed to the inputs of the four output stages based on the OCFG0 and OCFG1, nERROR/CFG0, and PSSYN/C1 configuration settings. Each output stage includes its own high-side and low-side current sensing that feeds to internal monitor logic and provides its nERROR output connection. Temperature and undervoltage monitoring also provide status and input to device protection control.

FIGURE 14. OUTPUT STAGE
Output Options

The D2-4P devices provide four configuration options for the power stage outputs. The power stage configuration is selected by strapping the OCFG0 and OCFG1 pins high or low. These defined configurations include:

• Two channels of full bridge, 4-quadrant outputs
• Two channels of full bridge, 2-quadrant outputs
• Four channels of half-bridge outputs
• Two channels of half-bridge and one channel of full bridge

Audio processing routing and control supporting the output stage configurations is defined by the logical high or low strapping of the nERROR/CFG0 and PSSYNC/CFG1 pins. Audio path definition, audio path output routing, and output stage configurations are automatically set to one of the four available modes based on these configuration settings.

PWM Audio Outputs

Three PWM outputs provide audio for up to three line-level outputs. Audio processing channel assignment is mapped to these PWM outputs based on the device's available configuration settings.

Using only a simple passive filter, the PWM outputs drive line-level outputs at a nominal 1VRMS. If active filter configurations are added, the PWM outputs can also drive headphone outputs or 2Vrms or higher line outputs. (alternately, these PWM outputs can also be used to drive powered outputs using additional power stages on the system design).

Control and Operation

Control Register Summary

The control interface provides access to the registers used for audio processing blocks and signal flow parameters. Audio input selection (I2S input or S/PDIF receiver input) and all programmable data elements used in the audio processing paths are controlled through these register parameters, and each parameter is defined with its specific register address.

Programming details, register identification, and parameter calculations are provided in the D2-4 Family /D2-4P Register API Specification document.

I2C 2-Wire Control Interface

The 2-Wire I2C compatible interface allows communication with an external controller. This interface is usable through either an external microcontroller bus, or for communication to EEPROMs, or other compatible peripheral chips.

The I2C interface supports normal and fast mode operation and is multi-master capable. In a D2-4P system application, it operates as an I2C slave device where the system controller operates as the I2C master.

Reading and Writing Control Registers

All reads or writes to registers (shown in Figures 15 and 16) begin with a Start Condition, followed by the Device Address byte, three Register Address bytes, three Data bytes, and a Stop Condition.

Register writes through the I2C interface are initiated by setting the read/write bit that is within the device address byte. The Write sequence shown in Figure 15 on page 19 is described in Table 2.

All reads to registers, shown in Figure 16 on page 19, require two steps. First, the master must send a dummy write, which consists of sending a Start, followed by the device address with the write bit set, and three register address bytes. Next, the master must send a repeated Start, send the device address with the read/write bit set to Read, and read the next three data bytes. The master must Acknowledge (ACK) the first two read bytes, send a Not Acknowledge (NACK) on the third byte received, and send a Stop condition to complete the transaction. The device's control interface acknowledges each byte by pulling SDA low on the bit immediately following each write byte. The read sequence shown in Figure 16 is described in Table 3.

<table>
<thead>
<tr>
<th>TABLE 2. I2C WRITE SEQUENCE</th>
<th>BYTE NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Device Address</td>
<td>Device address with R/W bit set</td>
</tr>
<tr>
<td>1</td>
<td>Register Address [23:16]</td>
<td>Upper eight bits of address</td>
</tr>
<tr>
<td>2</td>
<td>Register Address [15:8]</td>
<td>Middle eight bits of address</td>
</tr>
<tr>
<td>3</td>
<td>Register Address [7:0]</td>
<td>Lower eight bits of address</td>
</tr>
<tr>
<td>4</td>
<td>Data[23:16]</td>
<td>Upper eight bits of write data</td>
</tr>
<tr>
<td>5</td>
<td>Data[15:8]</td>
<td>Middle eight bits of write data</td>
</tr>
<tr>
<td>6</td>
<td>Data[7:0]</td>
<td>Lower eight bits of write data</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TABLE 3. I2C READ SEQUENCE</th>
<th>BYTE NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Device Address</td>
<td>Device address with Write bit set</td>
</tr>
<tr>
<td>1</td>
<td>Register Address [23:16]</td>
<td>Upper eight bits of address</td>
</tr>
<tr>
<td>2</td>
<td>Register Address [15:8]</td>
<td>Middle eight bits of address</td>
</tr>
<tr>
<td>3</td>
<td>Register Address [7:0]</td>
<td>Lower eight bits of address</td>
</tr>
<tr>
<td>4</td>
<td>Device Address</td>
<td>Device address with Read bit set</td>
</tr>
<tr>
<td>5</td>
<td>Data[23:16]</td>
<td>Upper eight bits of write data</td>
</tr>
<tr>
<td>6</td>
<td>Data[15:8]</td>
<td>Middle eight bits of write data</td>
</tr>
<tr>
<td>7</td>
<td>Data[7:0]</td>
<td>Lower eight bits of write data</td>
</tr>
</tbody>
</table>
Control Interface Address Spaces

Registers are accessed through the I2C control interface using the I2C channel address of 0xB2. This establishes the device or product under control through I2C communication as the D2-4P. Registers and memory spaces are defined within the D2-4P for specific internal operation and control. The highest-order byte of the register address (Bits 23:16) determines the internal address space used for control read or write access. The remaining 16 bits (Bits 15:0) describe the actual address within that space.

Programmable settings for the audio processing blocks are internally mapped to the address space defined with the highest order bits all zero. For example, 0x00nnnn, where nnnn is the address location within this address space.

Storing Parameters to EEPROM

The D2-4P can store parameter data to an EEPROM. If an EEPROM is installed in the application, the programmable parameter data can be saved in this EEPROM. This stored data can then be recalled upon reset or power-up.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is an alternate serial input port that provides an interface for loading parameter data from an optional EEPROM or Flash device during boot-up operation. The four SPI interface pins are all shared functions:

- Following a reset condition and while the device is initiating the boot-up process, these four SPI pins (TEMP REF /SCK, TEMP1/MOSI, VOL1/MISO, VOL0/nSS) function as a SPI input port for external boot loading operation
- As soon as the boot-up process is completed and the device begins executing its firmware program, these pins are no longer used for SPI functions and are reassigned by the firmware for use as dedicated-function I/O for amplifier operation

See the multiple-purpose pin descriptions in Table 5 for more information about these pin functions.

Reset and Device Initialization

The D2-4P must be reset to initialize and begin proper operation. A system reset is initiated by applying a low level to the nRESET input pin. External hardware circuitry or a controller within the amplifier system design must provide this reset signal and connect to the nRESET input to initiate the reset process. Device initialization begins after the nRESET pin is released from its low-active state.

The chip contains power rail sensors and brownout detectors on the 3.3V RVDD and PWMVDD power supplies and the 1.8V CVDD power supply. A loss or droop of power from these supplies triggers their brownout detectors, which asserts the nRSTOUT output pin, driving it low. The nRSTOUT pin should connect to the nRESET input through hardware on the amplifier design to ensure a proper reset occurs if the power supply voltages drop below their design specifications.

At the deassertion of nRESET, the chip reads the status of the boot mode selection pins (IRQA and IRQB) and begins the boot process, determined by the boot mode that is defined by these pins' logic state. These device pins are strapped either high or low on the system's design (PCB). The state of these pins that is latched into defines the boot mode operation.

---

FIGURE 15. I2C WRITE SEQUENCE OPERATION

---

FIGURE 16. I2C READ SEQUENCE OPERATION

---

Step 1

Step 2

Read Sequence

---
Boot Modes

The D2-4P devices contain embedded firmware to operate the part and run the amplifier system. Parameter information used by the programmable settings can be written to the device after it is operational and running. However, parameter data can also be read at boot time, which allows saved parameter settings to be used, or allows amplifier function to be set through a system microcontroller interface. The device is designed to boot in one of four possible boot modes, allowing control and data to be provided through these boot sources:

- I2C slave (to external microcontroller)
- I2C EEPROM
- Internal device ROM only
- SPI slave

The specific boot mode is selected based on the state of the IRQB and IRQA input pins at the time of reset de-assertion. Boot modes and their functions are shown in Table 4.

Note: “Boot mode” describes the mode of device initialization with respect to the source of parameter data or start-up control settings. Do not confuse Boot Mode with “Output Mode” or audio processing “Configuration Mode” settings that define amplifier-specific functions.

The device initializes as defined by its boot mode, but gets its configuration and parameter data from the host device. This host device can be either an external controller, or from an EEPROM. If a system uses both an external controller and an EEPROM, the EEPROM loads first. During this time, the controller must remain off the I2C bus until after the reading sequence from the EEPROM is complete.

Power Supply Requirements

The device requires operating power for these voltages:

- PWMVDD and RVDD:
  - 3.3V DC supply voltage
  - RVDD operates interface and I/O logic
  - PWMVDD is the same voltage and is used for the PWM outputs and output stage drive

- CVDD and PLLVDD:
  - 1.8V DC supply voltage
  - CVDD operates the internal processor and DSP core
  - PLLVDD also operates at the internal processor voltage levels, but is provided through a separate connection to allow isolation and bypassing for noise and performance improvements

- “High Voltage” (HVDD[A:D] and VDDHV):
  - HVDDA, HVDDB, HVDDC, and HVDDD are the “High Voltage” supplies used for operating each of the four output power stages
  - VDDHV is used as the source for the on-chip +5V regulator that is used for the output stage drivers
  - Individual power (HVDD[A:D]) and their corresponding ground (HGND[A:D]) pins are included for each of the four power stage outputs, providing channel isolation and low impedance source connections to each of the outputs. All the HVDD[A:D]/VDDHV pins connect to the same voltage source

High-Side Gate Drive Voltage

An on-chip bootstrap circuit provides the gate drive voltage used by each output stage. A pin is included for each output channel (HSBS[A:D]) for connection of a capacitor (nominal, 0.22µF/50V) from this pin to that channel’s PWM output.

Drivers for high-side FETs on the output stages require a voltage above the supply used for powering that FET. The charge pumping action of the driving PWM to this driver produces this “bootstrap” voltage, and uses this capacitor to filter and hold this gate drive voltage. This enables amplifier operation without needing a connection to an additional power supply voltage.

Power Supply Synchronization

The PSSYNC/CFG1 pin provides a power supply synchronization signal for switching power supplies. Firmware configures this pin to the frequency and duty cycle needed by the system switching regulator. This synchronization allows switching supplies used with the device to operate without generating in-band audio interference signals that could occur if the switching power supply is not locked to the amplifier switching. This PSSYNC/CFG1 pin is a shared pin (see the multiple-purpose pin descriptions in Table 5 on page 23). During device reset and initialization, the pin operates as one of two configuration input pins, where its high or low logic state is used to set the amplifier configuration mode. After completing reset and when the device firmware begins operating, this pin becomes the PSSYNC output.

<table>
<thead>
<tr>
<th>BOOT MODE</th>
<th>IRQB PIN</th>
<th>IRQA PIN</th>
<th>MASTER/SLAVE DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td></td>
<td></td>
<td>I2C Slave: Operates as an I2C slave, boot at address 0x88. An external 2-wire I2C master provides the boot code</td>
</tr>
<tr>
<td>101</td>
<td></td>
<td></td>
<td>I2C Master: Operates as a 2-wire master; loads the boot code from ROM on the I2C port</td>
</tr>
<tr>
<td>210</td>
<td></td>
<td></td>
<td>Internal ROM boot/operation</td>
</tr>
<tr>
<td>311</td>
<td></td>
<td></td>
<td>SPI Slave: SPI slave. An external SPI master provides the boot code</td>
</tr>
</tbody>
</table>
After CVDD reaches its minimum limit, VC\text{DD, min} must be the voltage that is present at CVDD. (If RVDD and PWMVDD supplies (nominal +3.3V) must not exceed (active) low. Asserting nPDN also causes all four nERROR[0:3] outputs to pull other references remain active during this power-down state. When this input is pulled low, all audio outputs turn off. The nPDN Input Pin makes other connections to this pin. An undervoltage condition for the voltages used by the output stage drivers requires their own +5VDC supply. Do not produce this +5V voltage. The REG5V pin is used for external voltage. An on-chip regulator operates from the VDDHV voltage to fold back a power supply regulator. During application of power to the system and while the CVDD and RVDD (including PWMVDD) voltages should be brought up together to avoid high current transients that could cause this connection should be made as close as practical to the pin. This capacitor connection to filter this regulated voltage. A 1.0µF and 1.8V supplies from that source. Also, as noted in " on page 4, all voltages of the same names must their specified limits. However, during application of power, the monitoring prevents operation until all supply voltages are within normal operation, it is held high with pull-up to the RVDD supply. The nPDN pin is active low and is inactive when at logic high. In other steps to clear this hardware latched shutdown, although overcurrent condition. Firmware protection control performs protection events that occur through firmware control from an overcurrent hardware shutdown logic, in addition to the separate overcurrent hardware shutdown logic, in addition to the separate.
nERROR/CFG0 and PSSYNC/CFG1 Pins

These pins define the amplifier configuration mode that the firmware uses to operate the amplifier. In addition to the OCFG0 and OCFG1 pins that set operation of the output stages, the nERROR/CFG0 and PSSYNC/CFG1 pins also establish audio signal processing path assignments and set up monitoring and protection for the configuration mode. The configuration pin logic levels are assigned by pull-up or pull-down resistors installed on that application.

The configuration defined by these pins is assigned when the D2-45057/D2-45157 exits its reset state. At that time, the logic statuses of the PSSYNC/CFG1 and nERROR/CFG0 pins are latched into internal device registers. These are shared-function pins, and after firmware begins executing, their functions are reassigned as outputs. See Table 5 on page 23 for more information about these pins and their shared functions.

Temperature Monitoring

The TEMPREF/SCK, TEMP1/MOSI, and TEMPCOM/TIO0 pins are used in a firmware-controlled algorithm to monitor temperature. These pins share other functions (see the multiple-purpose pin descriptions in Table 5 on page 23). During firmware execution, they operate as inputs and outputs for the measurement algorithm. Figure 17 shows the circuit for this temperature implementation.

A Negative Temperature Coefficient (NTC) 100kΩ resistor connects to the TEMP1/MOSI pin, and using the resistor's temperature/resistance correlation, the firmware monitors temperature of the NTC resistor. The internal device timing functions associated with the TIO0 pin provide calibration that correlates to system clock. A 49.9kΩ resistor connects to the TEMPREF/SCK pin and is used as a constant non-temperature-dependent reference for this algorithm. The firmware algorithm is internal to the D2-4P. The status from this temperature monitor is used for the temperature protection functions of the device and its application. There are no adjustments or parameters for changing settings.

FIGURE 17. TEMPERATURE MONITOR CIRCUIT

100 k
49.9 k
0.1µF

TEMP1/MOSI
TEMPREF/SCK
TEMPCOM/TIO0
Configuration Setting

The configuration mode is assigned through two pairs of pin settings. When the D2-4P exits its reset state, the logic status of the PSSYNC/CFG1 and nERROR/CFG0 pins is latched into internal device registers. During this initialization time, these pins operate as logic inputs. After initialization completes and the internal firmware begins executing, these pins are re-assigned as outputs for their shared functions, and the internal latched logic state that defines the configuration mode remains until the device is powered down or reset again. The OCFG0 and OCFG1 pin status is not latched; those pins must remain in their pull-up or pull-down state.

Selection of one of the four configuration modes is defined by strapping the configuration pins high or low:

- OCFG0 and OCFG1 define the output power stage configuration
- nERROR/CFG0 and PSSYNC/CFG1 define the amplifier and channel configuration

These four pins are connected to either a high level (+3.3V) or low level (ground = 0). Connections should be through a 10k Ω resistor and not directly to the supply or ground.

Table 6 on page 24 shows the audio processing channel assignment, audio content, and output assignments for each of the four configuration modes.

Both pairs of configuration setting pins (OCFG0, OCFG1) and (PSSYNC/CFG1, nERROR/CFG0) must be used and both must be set to the same configuration mode.

In modes 2 and 3, the filtering for high and low pass crossovers is applied to the audio signal flow path, enabling the appropriate high or low pass content to be properly filtered for the PWM output channels.
<table>
<thead>
<tr>
<th>MODE</th>
<th>CONFIGURATION</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CFGPINS</td>
<td>CONFG MODE</td>
<td>CFGPINS</td>
</tr>
<tr>
<td>AUDIO</td>
<td>PROCESSOR</td>
<td>AUDIO</td>
</tr>
<tr>
<td>CHANNEL</td>
<td></td>
<td>CHANNEL</td>
</tr>
<tr>
<td>AUDIO</td>
<td>CONTENT</td>
<td>AUDIO</td>
</tr>
<tr>
<td>POWER</td>
<td>STAGE OUTPUTS</td>
<td>POWER</td>
</tr>
<tr>
<td>ERRORS</td>
<td>to PROTECTORS</td>
<td>ERRORS</td>
</tr>
<tr>
<td>PWM</td>
<td>LINE OUTPUTS</td>
<td>PWM</td>
</tr>
<tr>
<td>OCFG1</td>
<td>OCFG0</td>
<td>OCFG1</td>
</tr>
<tr>
<td>PSSSYNC</td>
<td>/CFG1</td>
<td>PSSYNC</td>
</tr>
<tr>
<td>/CFG0</td>
<td></td>
<td>/CFG0</td>
</tr>
<tr>
<td>OUTA</td>
<td>OUTB</td>
<td>OUTA</td>
</tr>
<tr>
<td>OUTC</td>
<td>OUTD</td>
<td>OUTC</td>
</tr>
<tr>
<td>L1</td>
<td>L2</td>
<td>L1</td>
</tr>
<tr>
<td>R1</td>
<td>R2</td>
<td>R1</td>
</tr>
<tr>
<td>SUB</td>
<td></td>
<td>SUB</td>
</tr>
<tr>
<td>LINE</td>
<td>PROTECTORS unused (tie high)</td>
<td>LINE</td>
</tr>
<tr>
<td>HB</td>
<td></td>
<td>HB</td>
</tr>
<tr>
<td>HF</td>
<td></td>
<td>HF</td>
</tr>
<tr>
<td>LF</td>
<td></td>
<td>LF</td>
</tr>
<tr>
<td>LF</td>
<td></td>
<td>LF</td>
</tr>
<tr>
<td>HF</td>
<td></td>
<td>HF</td>
</tr>
<tr>
<td>LF</td>
<td></td>
<td>LF</td>
</tr>
</tbody>
</table>

**NOTE:** LF = Low Frequency, HF = High Frequency for Bi-Amp Config; HB = Half-Bridge
Error Reporting

- Chip temperature monitoring provides dual threshold status of high temperature conditions, providing both indication and device shutdown if needed.
- Provide indication and device shutdown (if needed) for user-induced faults such as clipping, output overload, or output shorts, including both shorted outputs or short-to-ground faults.
- Shut down the device if power supply sensors detect voltages from the high voltages, currents, and temperatures present in class-D amplifiers. This protection is also effective against shoot-through overcurrent, power supply brown-out, over-temperature, output short-circuit, and output overcurrent.

Protective Monitoring and Control

- Each PWM output FET includes a dual-threshold overcurrent sensor. Multiple functions occur depending on detection of overcurrent conditions:
  - The lower threshold monitors fault conditions such as shorts, including both shorted outputs or short-to-ground faults.
  - The higher threshold monitors fault conditions of the PWM drive (the PWM pin floats when shut down) until the controller acknowledges the fault event by turning off the nERROR output is asserted. These conditions remain latched through the duration of the overcurrent event.

- On-chip hardware thermal protection shuts down the device upon trigger.
- Thermalsensing provides two thresholds of temperature monitoring. Temperature monitoring is included for all supply voltages.
- The PROTECT[0:2] pins are used as protection inputs to the device firmware. Firmware action based on these pins' status depends on the type and severity of the detected event, but the action taken is to reduce conditions that contribute to the event, with the severity of a complete shutdown as in a high-limit shutdown. For lower-threshold event detections, graceful shutdown is included for all supply voltages.
- Thermal Protection and Monitors

- The PROTECT[0:2] pins are used as protection inputs to the firmware. The nERROR[0:3] pins.
- The PROTECT0-2 inputs drive four output stages. It also drives all four nERROR0-3 outputs low for more information about shared-function pins.
- Protection Monitoring and Control

During a reset condition, this pin operates as an input and is one of two input pins used to define the configuration mode. A resistor pull-up or pull-down on this pin establishes the mode of operation.

For more information about shared-function pins, refer to Table 6 on page 24.
nERROR0-3 outputs. Overcurrent detection algorithms in firmware monitor these peak level detections, and upon detection of an overload condition, automatically reduce PWM gain. This Automatic Gain Control (AGC) action helps prevent audio output clipping and helps avoid related excessive-level conditions. The AGC algorithm operation functions through a stepped-changing of PWM gain reduction corresponding to characteristics and time-event detection of overloads. At the lower (non shut-down) high-temperature threshold, the AGC function also acts to attenuate the outputs to attempt to reduce temperature. Output level gain and level change effects from the AGC function are similar to operation from a compressor. However, unlike a compressor where characteristics are determined by input levels, the PWM AGC operation is controlled through detection of near-overload output levels or from high temperature detection.

Power Supply Voltage Monitoring

Undervoltage sensors and brownout detectors monitor all supply voltages to the device. The logic and built-in protection of this voltage monitoring prevents operation until all supply voltages are within their specified limits. If any of these monitored voltages drop below their threshold, the device shuts down its outputs and asserts all four of the nERROR outputs.

Audio Processing

The audio processing, signal flow, and system definition is defined by the D2-4P internal ROM firmware and is executed by the DSP. The firmware defines the audio flow architecture, including the audio processing blocks. Each block is programmable and has adjustable audio-controlling parameters. The signal flow and audio processing blocks are shown in Figure 18. This architecture includes audio processing functions for:

- Input selection
- Mixers
- Input compressors and output limiters
- Tone controls
- 5-band and 3-band parametric equalizers
- Router
- High/low-pass crossover filters
- Volume and output level controls
- Loudness contour

Enhancement Audio Processing

The D2-45057 supports the D2 Audio DSP Sound Enhancement Algorithm. The D2-45157 supports the DTS® (SRS) WOW/HD™ algorithm.

Audio Processing Signal Flow Blocks

INPUT SELECTION

The Input Select registers specify the audio inputs that are assigned to the audio processing input path. Either the I2S or S/PDIF Digital inputs are available.

MIXERS

An input mixer provides a two-input, two-output mixing and routing path. Either input can be mixed at adjustable gain into either or both of the two outputs. The default setting is 0dB through each channel, with full cut-off for non-through channels. Attenuation is continuously variable with the programmable parameters. A stereo mixer provides a path from the two input channels. Stereo mixers are typically used to provide a mix of both stereo input channels for crossover processing and become the source for the subwoofer channel. Gains for both input channels are adjustable to feed the single stereo mixer output.

TONE CONTROLS

Both input channels contain a tone control block. Each of the filters (bass or treble) is implemented with a first-order (6dB/octave) roll-off, using programmable corner frequency and a boost or attenuating gain. The signal flow processing automatically provides a smooth transition between tone control changes.
FIGURE 18. D2-4P AUDIO SIGNAL FLOW

2x2 Mixer
Tone 1
5 Band EQ 1
Compressor 1
DIGITAL Input Select
S/PDIF Digital Input
2x1 Mixer
Speaker EQ 1
4x4 Router
Licensed Audio Processing Algorithm
* (See Note)
S/PDIF
2 SRC
I2S Digital Input
Compressor 2
Tone 2
5 Band EQ 2
Speaker EQ 2
HP 1
LP 1
HP 2
LP 2
HP 3
LP 3
HP 4
LP 4
HP 5
LP 5
3 Band EQ 1
3 Band EQ 1
3 Band EQ 1
3 Band EQ 1
Master Volume Control
Loudness 1
Loudness 2
Loudness 3
Loudness 4
Loudness 5
Limiter 1
Limiter 2
Limiter 3
Limiter 4
Limiter 5
Volume 1
Volume 2
Volume 3
Volume 4
Volume 5
Crossovers

* Note: Device-dependent licensed audio processing algorithm supporting D2Audio Sound Enhancement Algorithm, or SRS WOW/HD®. Refer to device or der information for part number specifying each algorithm.

PWM Channel Driver Mapping
Output stage channel assignment and amplifier topology is programmed with configuration pin settings. Four output modes are available with combinations of 4- and 2-quadrant full bridge, and half bridge operation for outputs A-D. Line and subwoofer output channel assignment is also established by output mode configuration settings.
COMPRESSORS AND LIMITERS

Two individual input compressors are included in the input audio path, one for each of the two input channels. Five output limiters are also included in the five output path channels. The Compressor and Limiter blocks operate identically, and their parameter settings allow independent control of the audio signals. Typically, the input path blocks are programmed to provide a compression function and the output path blocks are programmed to limit output signal levels. However, each path can be programmed as needed. Each Compressor/Limiter has configurable Compression Ratio, Threshold, Attack and Release Time, as well as Makeup Gain.

MULTI-BAND EQUALIZERS

Three sets of Multi-Band Parametric Equalizers are included in the audio signal processing path. Each band of the equalizers provides independent gain, frequency, and Q-factor programming. A 5-Band Equalizer and a Speaker Equalizer (SEQ) are included in both of the two input channels. Four 3-Band Equalizers are also located in the four output channels.

STEREO ROUTER

A 4x4 stereo router assigns any one of the four input channel paths to each of the four output paths. The router performs path assignment only. It does not provide gain or signal level adjustment.

HIGH/LOW-PASS CROSSOVER FILTERS

High-Pass and Low-Pass filter blocks are provided for each of the five output channels downstream of the Router and Stereo Mixer. These filter blocks provide a flexible Crossover function for all the output channels, including defining the subwoofer channel's frequency response. The High and Low Pass blocks operate together and are implemented as a total of four cascaded elements. Two of each of the elements are allocated for High Pass functionality and the other two elements are allocated for Low Pass functionality. Complete flexibility allows each element to be optionally defined for either High Pass or Low Pass. Each element is selectable for a slope of 6dB, 12dB, 18dB, or 24dB, or can be bypassed. Butterworth, Bessel, or Linkwitz-Riley filter implementations are available.

MASTER VOLUME CONTROL

Use the software-controlled Master Volume control to adjust the global volume for all five output channels. Master Volume operates a continuously adjustable attenuator, from unity gain down to -100dB and cutoff.

Each of the five output channels has its own dedicated output level adjustments that provides individual channel gain or attenuation after the output limiter stages. Settings provide output level adjustment from +12dB to -100dB.

LOUDNESS CONTOUR

An individual software-controlled Loudness Contour is included for each of the five amplifier output channels. The Loudness Contour curve is customized to allow for dynamically and automatically enhancing the frequency response of the audio program material relative to the Master Volume Level setting. The Loudness Contour models the frequency response correction as defined by the Fletcher/Munson audio response curve. It provides amplitude or volume changes to signals to which the ear does not respond equally at very low listening levels.

SOUND ENHANCEMENT ALGORITHM PROCESSING

The D2 Audio DSP Sound Enhancement Algorithm audio processing provides a full set of enhancements to audio that greatly add to the quality and listening experience of sound in wide scopes of consumer devices. The D2 Audio DSP Sound Enhancement Algorithm uses psycho-acoustic processing that creates a rich-sounding environment from small speakers and synthesizes the sound and quality equivalent to more complex systems. It is especially suited to consumer products that include televisions, docking stations, and mini hi-fi stereo products. Sound enhancement algorithm processing includes:

• 2-channel stereo spatialization
• Bass enhancement
• Content/configuration EQ presets
• Improved vocal clarity
• Automatic room audio setup/equalization/optimization
• Automatic loudspeaker setup/equalization/correction

The D2 Audio DSP Sound Enhancement Algorithm is completely included within the D2-4P Family devices.
Disclaimer for DTS® Technology License Required Notice:

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Visit our website to make sure you have the latest datasheet revision.

DATERevisionChange
Mar 19, 2019FN6785.2 Changed datasheet base part number to "D2-4P" Family Audio SOC.

Changed the following terms throughout the datasheet:
- "D2Audio" to "D2 Audio DSP"
- "DAE-4" to "D2-4P family"
- "DAE-4P" to "D2-4P family"
- "Digital Audio Engine" to "Digital Audio Processor"
- "SoundSuite" to "Sound Enhancement Algorithm"

Updated Related Literature

Updated audio enhancement features on page 16.
Updated Figure 1 on page 1, Figure 13 on page 15, and Figure 18 on page 27.
Removed About Intersil section.
Updated disclaimer.

May 5, 2016FN6785.1 Updated entire datasheet applying Intersil's new standards.

Updated the Ordering Information table on page 2.
Replaced Products verbiage to About Intersil verbiage.

Jul 29, 2010FN6785.0 Initial Release
Package Outline Drawing

Location within the zone indicated. The pin #1 identifier may be

Unless otherwise specified, tolerance: Decimal ± 0.05

Tiebar shown (if present) is a non-functional feature.

The configuration of the pin #1 identifier is optional, but must be

between 0.23mm and 0.28mm from the terminal tip.

Dimensions in ( ) for Reference Only.

Dimensioning and tolerancing conform to AMSE Y14.5m-1994.

NOTES:

1. Dimensions are in millimeters.
2. Either a mold or mark feature.
3. 5.
4. 2.
5.

For the most recent package outline drawing, see L68.10x10C.