The D2-4 Family (D2-41051 and D2-41151 (D2-41x51-QR)) devices are complete System-on-Chip (SoC) Audio Processors and Class-D Amplifier Controllers that offer a powerful yet very cost-effective audio solution for high volume consumer products, including digital TV systems, PC multimedia speakers, and portable device docking stations. This 4th generation Digital Audio Processor (D2-4 family) device combines extensive integrated DSP processing and configurable audio processing algorithms for complete audio system control.

The D2-4 family devices offer the optimum balance of functionality and lowest system material cost, especially in an SoC system architecture with I2S audio output. All audio processing and amplifier control is handled by the D2-4 family, and its ease of integration to the existing system processor handles all system control functions.

Related Literature
For a full list of related documents, visit our website:
- D2-41051 and D2-41151 device pages

Features
- All digital class-D amplifier controller with integrated Digital Signal Processing (DSP)
- Fully programmable audio signal path parameters
- Up to 5 channels of Digital Signal Processing (DSP)
- Includes equalizers, filters, mixers, and other common audio processing blocks
- Audio enhancement algorithms included
- I2S and S/PDIF™ digital audio stereo inputs
- I2C host control port
- Asynchronous sample rate converters, sample rates from 32kHz up to 192kHz
- Supports 2.0, 2.1, or bi-amp amplifier outputs with discrete or integrated power stages

Applications
- PC multimedia speakers
- Digital TV audio systems
- Portable device docking stations
- Powered speaker systems

FIGURE 1. TYPICAL APPLICATION

D2-4 FAMILY

PWM CONTROLLER AND AUDIO PROCESSOR

PWM OUTPUT DRIVERS

OUTPUT FILTER

PWM0

PWM1

INPUT FILTER

PWM2

PWM3

OUTPUT FILTER

PWM4

PWM5

INPUT FILTER

PWM6

PWM7

STEREO LINE OUT

OR HEADPHONE OUT

5 CHANNEL PWM ENGINE

24 BIT DIGITAL SIGNAL PROCESSOR

2 CHANNEL SAMPLE RATE CONVERTER

DIGITAL AUDIO INTERFACE

S/PDIF DIGITAL I/O INTERFACE

SOC SYSTEM CONTROLLER(S)

I2S

I²C CONTROL

S/PDIF BUFFER

S/PDIF BUFFER

OPTICAL/COAX IN (OPTIONAL)

OPTICAL/COAX OUT (OPTIONAL)

D2 AUDIO DSP

D2 AUDIO CUSTOMIZATION

GUI DRIVER

3RD PARTY ENHANCEMENTS (SRS WOW/HD®)

D2 AUDIO DSP
Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>AUDIO PROCESSING FEATURE</th>
<th>SET SUPPORT</th>
</tr>
</thead>
<tbody>
<tr>
<td>D2-41051-QR</td>
<td>D2 Audio DSP Sound Enhancement Algorithm</td>
<td></td>
</tr>
<tr>
<td>D2-41051-QR-TK</td>
<td>D2 Audio DSP Sound Enhancement Algorithm</td>
<td></td>
</tr>
<tr>
<td>D2-41151-QR</td>
<td>D2 Audio DSP Sound Enhancement Algorithm</td>
<td>DTS®(SRS) WOW/HD™</td>
</tr>
<tr>
<td>D2-41151-QR-TK</td>
<td>D2 Audio DSP Sound Enhancement Algorithm</td>
<td>DTS®(SRS) WOW/HD™</td>
</tr>
</tbody>
</table>

NOTES:
1. See TB347 for details about reel specifications.
2. The D2-4 family supports audio processing algorithms for the D2 Audio DSP Sound Enhancement Algorithm, and DTS®(SRS) WOW/HD® audio enhancement features. Algorithm support of these enhancements is device-dependent. See the specific part number for desired feature support.
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (Sn3/Pb-960 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). The Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
4. For Moisture Sensitivity Level (MSL), see the D2-41051 and D2-41151 device pages. For more information about MSL, see TB363.

Pin Configuration

48 LD QFN

TOP VIEW

1 2 3 4 5 6 7 8 9 10 11 12

36 35 34 33 32 31 30 29 28 27 26 25

SCLK  SDIN  LRCK  MCLK  CVDD  CGND  RGND  RVDD  TEMPREF/SCK  nMUTE/TIO1  VOL1/MISO  TEMP1/MOSI

36 35 34 33 32 31 30 29 28 27 26 25

PWMVDD  PWM0  PWM1  PWM2  PWM3  PWMGND  PWMVDD  PWM4  PWM5  PWM6  PWM7  PWMGND

48 47 46 45 44 43

38 37

SCL  SDA  TEMPCOM/TIO0  nRESET  nRSTOUT  CVDD  CGND  VOL0/nSSPLLAVDD  XTALO  XTALI  PLLAGND
<table>
<thead>
<tr>
<th>PIN</th>
<th>PIN NAME</th>
<th>TYPE</th>
<th>VOLTAGE LEVEL (V)</th>
<th>DRIVE STRENGTH (mA)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SCLK</td>
<td>I2S serial audio bit clock (SCLK) input. Input has hysteresis.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>SDIN</td>
<td>I2S serial audio data (SDIN) input. Input has hysteresis.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>LRCK</td>
<td>I2S serial audio left/right (LRCK) input. Input has hysteresis.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>MCLKO</td>
<td>3.3V</td>
<td>3.3V master clock output for external ADC/DAC components, drives low on reset. Output is an 8mA driver.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>CVDD</td>
<td>3.3V</td>
<td>3.3V core power, +1.8V DC. Used in the chip internal DSP, logic, and interfaces.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>CGND</td>
<td>3.3V</td>
<td>3.3V core ground</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>RGND</td>
<td>3.3V</td>
<td>3.3V digital pad ring ground. Internally connected to PWMGND.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| 8    | RVDD     | 3.3V | 3.3V digital pad ring power, 3.3V. These 3.3V supplies are used for all the digital I/O pad drivers and receivers, except for the analog pads. Both are required to be connected. Internally connected to PWMVD.
<p>| 9    | TEMPLREF | 3.3V | 3.3V reference pin for the temperature monitor and SPI clock. At deassertion of device reset, this pin operates as a SPI clock. Upon internal D2-4 family firmware execution, this pin becomes a temperature monitor reference. |
| 10   | nMUTE    | 3.3V | 3.3V mute signal output. When active low, the mute condition drives this pin low. Output is a 16mA driver. Initializes as an input on reset, then becomes an output upon internal firmware execution. |
| 11   | VOL1     | 3.3V | 3.3V volume control pulse input and SPI master-input/slave-output data signal. At deassertion of device reset, this pin operates as a SPI master input or slave output. Upon internal D2-4 family firmware execution, this pin becomes an input for monitoring up/down phase pulses from volume control (one of two volume input pins). |
| 12   | TEMP1    | 3.3V | 3.3V temperature monitor pin and SPI master-output/slave-input data signal. At deassertion of device reset, this pin operates as a SPI master output or slave input. Upon internal D2-4 family firmware execution, this pin becomes an input for monitoring temperature. |
| 13   | SPDIFRX  | 3.3V | 3.3V S/PDIF digital audio data input. |
| 14   | SPDIFTX  | 3.3V | 3.3V S/PDIF digital audio data output. This pin is the S/PDIF audio output and drives an 8mA, 3.3V stereo output up to 192kHz. Pin floats on reset. |
| 15   | TEST     | 3.3V | 3.3V hardware test mode control. For factory use only. Must be tied low. |
| 16   | IRQA     | 3.3V | 3.3V interrupt request port A. One of two IRQ pins, tied to logic (3.3V) high or to ground. High/low logic status establishes boot mode selection upon deassertion of the reset (nRESET) cycle. |
| 17   | IRQB     | 3.3V | 3.3V interrupt request port B. One of two IRQ pins, tied to logic (3.3V) high or to ground. High/low logic status establishes boot mode selection upon deassertion of the reset (nRESET) cycle. |
| 20   | nERROR   | 3.3V | 3.3V output configuration selection input, and nERROR output. Upon device reset, this pin operates as an input, using application-installed pull-up or pull-down connection to the pin to specify one of four amplifier configurations. Upon internal D2-4 family firmware execution, this pin becomes an output and provides an active-low output drive when the amplifier protection monitoring detects an error condition. |
| 21   | PSSYNC   | 3.3V | 3.3V output configuration selection input and power supply sync output. Upon device reset, this pin operates as an input, using application-installed pull-up or pull-down connection to the pin to specify one of four amplifier configurations. Upon internal D2-4 family firmware execution, this pin becomes an output and provides a synchronizing signal to the on-board power supply circuits. |</p>
<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>TYPE</th>
<th>VOLTAGE LEVEL (V)</th>
<th>DRIVE STRENGTH (mA)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOL0</td>
<td>/nSS</td>
<td>I/O</td>
<td>3.3</td>
<td>4</td>
<td>Volume control pulse input and SPI slave select. At deassertion of device reset, this pin operates as a SPI slave select input. Upon internal D2-4 family firmware execution, this pin becomes an input for monitoring up/down phase pulses from volume control (one of two volume input pins).</td>
</tr>
<tr>
<td>nRSTOUT</td>
<td>O</td>
<td>3.3</td>
<td>16</td>
<td>- OD Active low output. This pin drives low from the 3.3V brownout detector or 1.8V brownout detector going active. Use this output to initiate a system reset to the n RESET pin upon brownout event detection.</td>
<td></td>
</tr>
<tr>
<td>nRESET</td>
<td></td>
<td>3.3</td>
<td>- Active low reset input with hysteresis. Low level activates system level reset, initializing all internal logic and program operations. System latches boot mode selection on the IRQ input pins on the rising edge.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TEMPCOM/ TIO0</td>
<td></td>
<td>I/O</td>
<td>3.3</td>
<td>16</td>
<td>Temperature monitor common I/O pin.</td>
</tr>
<tr>
<td>SDA</td>
<td></td>
<td>I/O</td>
<td>3.3</td>
<td>8</td>
<td>OD Two-Wire serial data port, open-drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport. Pin floats on reset.</td>
</tr>
<tr>
<td>SCL</td>
<td></td>
<td>I/O</td>
<td>3.3</td>
<td>8</td>
<td>OD Two-Wire serial clock port, open-drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for clock signaling. Pin floats on reset.</td>
</tr>
</tbody>
</table>

NOTES:
5. All pin names are active high, unless otherwise specified. Pins that are active low have an “n” prefix, such as nRESET.
6. OD means the pad has an open-drain driver.
7. All power and ground pins of the same names must be tied together to all other pins of their same name (for example, tie the RVDD pins together, RGND pins together, C VDD pins together, C GND pins together, PWMVDD pins together, and PWMGND pins together.).
Specifications

Absolute Maximum Ratings

(Note 10)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage RVDD, PWMVDD</td>
<td>-0.3V</td>
<td>4.0V</td>
<td></td>
</tr>
<tr>
<td>CVDD, PLL VDD</td>
<td>-0.3V</td>
<td>2.4V</td>
<td></td>
</tr>
<tr>
<td>Input Voltage Any Input but XTALI</td>
<td>-0.3V</td>
<td>RVDD + 0.3V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>XTALI</td>
<td>PLLVDD + 0.3V</td>
<td></td>
</tr>
<tr>
<td>Input Current, any Pin but Supplies</td>
<td>±10mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Thermal Resistance (Typical)

θJA (° C/W) 27

θJC (° C/W)

Temperature Range (Operating) 0°C to +70°C

Maximum Storage Temperature -55°C to +150°C

Pb-Free Reflow Profile see TB493

WARNING: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

8. θJA is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See TB379.

9. For θJC, the "case temp" location is the center of the exposed metal pad on the package underside.

10. Absolute Maximum parameters are not tested in production.

Recommended Operating Conditions

TA = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic.

Electrical Specifications

TA = +25° C, CVDD = PLL VDD = 1.8 V ± 5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Supply Pins CVDD</td>
<td>1.7V</td>
<td>1.8V</td>
<td>1.9V</td>
</tr>
<tr>
<td>Active Current - 300 - mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power-Down Current (Note 11)</td>
<td>-6mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Digital I/O and PWM Pad Ring Supply Pins RVDD and PWMVDD</td>
<td>3.0V</td>
<td>3.3V</td>
<td>3.6V</td>
</tr>
<tr>
<td>Active Current -10 -mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power-Down Current (Note 11)</td>
<td>-0.01mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog Supply Pins (PLL) PLL VDD</td>
<td>1.7V</td>
<td>1.8V</td>
<td>1.9V</td>
</tr>
<tr>
<td>Active Current -10 -mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power-Down Current (Note 11)</td>
<td>-5mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NOTE:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11. Power Down is with device in reset and clocks stopped.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Digital Input High Logic Level (Note 12) VIH

Digital Input Low Logic Level (Note 12) VIL

High Level Output Drive Voltage (Note 13) (IOUT = -Pad Drive) VOH

Low Level Output Drive Voltage (Note 13) (IOUT = +Pad Drive) VOL

High Level Input Drive Voltage XTALI Pin VIHX

Low Level Input Drive Voltage XTALI Pin VILX

Input Leakage Current (Note 14) IIN

Input Capacitance CIN

Output Capacitance COUT

nRESET Pulse Width Test 10 ns
CRYSTAL OSCILLATOR

Crystal Frequency (Fundamental Mode Crystal) X0 20 24.57625 MHz
Duty Cycle Dt 40 - 60%
Start-Up Time (Start-Up Time is Oscillator enabled (with Valid Supply) to Stable Oscillation)
Tstart - 5 - 20 ms

PLL

VCO Frequency Fvco 240 294.912 3 000 MHz
PLL Lock Time from any Input Change - 3 - ms

1.8V POWER ON RESET

Reset Enabled Voltage Level Ven 0.95 1.10 1.30 V
POR Minimum Output Pulse Width Tdis - 5 - µs

1.8V BROWNOUT DETECTION

Detect Level 1.4 1.5 1.7 V
Pulse Width Rejection Tbo 1 - 100 - ns
Minimum Output Pulse Width T01 - 20 - ns

3.3V (CVDD) BROWNOUT DETECTION

Detect Level 2.4 2.7 2.9 V
Pulse Width Rejection Tbo 3 - 100 - ns
Minimum Output Pulse Width T03 - 20 - ns

NOTES:
12. All input pins except XTALI.
13. All digital output pins. Drive strength for each digital pin is in the "D2-4 Family Pin Descriptions" on page 4.
14. Input leakage applies to all pins except XTALO.

Electrical Specifications
TA = +25°C, CVDD = PLL VDD = 1.8 V ± 5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912 MHz, OSC at 24.576 MHZ, core running at 147.456 MHz with typical audio data traffic. (Continued)

PARAMETERS SYMBOL MIN TYP MAX UNIT

Serial Audio Interface Port Timing

DESCRIPTION SYMBOL MIN TYP MAX UNIT

SCLK Frequency - (SCLK) tsSCLK - - 12.5 MHz
SCLK Pulse Width (HIGH and LOW) - (SCLK) twSCLK 40 - - ns
LRCKR Set-Up to SCLK Rising - (LRCK) tsLRCLK 20 - - ns
LRCKR Hold from SCLK Rising - (LRCK) thLRCLK 20 - - ns
SDIN Set-Up to SCLK Rising - (SDIN) tsSDI 20 - - ns
SDIN Hold from SCLK Rising - (SDIN) thSDI 20 - - ns
**FIGURE 2. SERIAL AUDIO INTERFACE PORT TIMING**

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCL Frequency</td>
<td>$f_{SCL}$</td>
<td>100 kHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bus Free Time Between Transmissions</td>
<td>$t_{buf}$</td>
<td>4.7 µs</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>SCL Clock Low</td>
<td>$t_{lowSCL}$</td>
<td>4.7 µs</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>SCL Clock High</td>
<td>$t_{highSCL}$</td>
<td>4.0 µs</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Set-Up Time for a (Repeated) Start</td>
<td>$t_{SSTA}$</td>
<td>4.7 µs</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Start Condition Hold Time</td>
<td>$t_{hSTA}$</td>
<td>4.0 µs</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>SDA Hold from SCL Falling (See Note 15)</td>
<td>$t_{hSDA}$</td>
<td>1 ms</td>
<td></td>
<td></td>
<td>s</td>
</tr>
<tr>
<td>SDA Set-Up Time to SCL Rising</td>
<td>$t_{sSDA}$</td>
<td>250 ns</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SDA Output Delay Time from SCL Falling</td>
<td>$t_{dSDA}$</td>
<td>3.5 µs</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Rise Time of Both SDA and SCL (See Note 16)</td>
<td>$t_{r}$</td>
<td>1 µs</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Fall Time of Both SDA and SCL (See Note 16)</td>
<td>$t_{f}$</td>
<td>300 ns</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Set-Up Time for a Stop Condition</td>
<td>$t_{sSTO}$</td>
<td>4.7 µs</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

**NOTES:**

15. Data is clocked in as valid on next XTAL rising edge after SCL goes low.
16. Limits established by characterization and not production tested.

**FIGURE 3. I2C INTERFACE TIMING**

- $t_{lowSCL}$
- $SCLx$
- $SDAx$(INPUT)
- $tsSTA$
- $thSTAx$
- $tr$
- $tf$
- $tsSDA$
- $thSDAx$
- $tsSTO$
- $tbuf$
- $SDAx$(OUTPUT)
- $tdSDAx$
- $twhighSCLx$
Overview

The D2-4 family devices are integrated System-on-Chip (SoC) audio processors and Class D amplifier PWM controllers. They include complete digital audio input selection, signal routing, complete audio processing, and selectable PWM output options for driving multiple output power stage configurations. Stereo I2S and stereo S/PDIF digital input support, plus I2C and 2-wire SPI control interfaces enable integration compatibility with existing system architectures and solutions. The audio path includes a stereo Sample Rate Converter (SRC) plus device-specific audio enhancement processing algorithms.

Output Configurations

A 5-channel PWM engine with applications selected configuration settings provides output paths for combinations of output channels. Application-dependent configuration selection includes PWM controller outputs for driving Stereo Speaker, 2.1 Speaker, and Stereo Bi-Amp Speaker solutions, as well as Stereo Line, Headphone Outputs, or Subwoofer Line Outputs. Depending on configuration settings, Full-Bridge, Half-Bridge and Bridge-Tied-Load (BTL) output stage topologies, with either discrete or integrated output stages are supported.

Programmable Audio Processing

Programmable parameter settings for audio processing include volume control, path routing and mixing, high/low pass filtering, multi-band equalizers, compressors, and loudness. These parameters can be adjusted using the D2 Audio Customization GUI software during design and development, or can be set through the device's control interface within production amplifier products.

Typical Performance

Final system performance is largely determined by the amplifier configuration, its choice of output power stages and components, and overall system design. Typical performance capability of amplifier power outputs varies from less than 10Ws to systems over 150W. System audio performance includes 20Hz to 20kHz frequency response, SNR of greater than 100dB, and THD+N performance typically below 0.1%.

SPI™ Master Mode Interface Port Timing

<table>
<thead>
<tr>
<th>SYMBOL DESCRIPTION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>tV MO SI Valid from Clock Edge</td>
<td>8 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tS MI SO Set-Up to Clock Edge</td>
<td>10 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tH MISO Hold from Clock Edge</td>
<td>1 system clock + 2ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tWINSS Minimum Width</td>
<td>3 system clocks + 2ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SPI™ Slave Mode Interface Port Timing

<table>
<thead>
<tr>
<th>SYMBOL DESCRIPTION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>tV MI SO Valid from Clock Edge</td>
<td>3 system clocks + 2ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tS MO SI Set-Up to Clock Edge</td>
<td>10 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tH MOSI Hold from Clock Edge</td>
<td>1 system clock + 2ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tWINSS Minimum Width</td>
<td>3 system clocks + 2ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Audio Enhancement Processing

The D2-4 family devices include D2 Audio DSP Sound Enhancement Algorithm (within the D2-41051 device) and DTS® (SRS) WOW/HD™ (within the D2-41151 device) audio enhancement algorithms. These functions are integrated within the firmware of each device and are part of the standard audio signal flow.

Functional Description

Figure 5 on page 11 shows a block diagram of the D2-4 family devices and serves as a reference for many of the items in the following descriptions.

Serial Audio Digital Input

The D2-4 family devices include one Serial Audio Interface (SAI) port accommodating two channels of digital audio input. This SAI port supports the I2S digital audio industry standard, and can carry up to 24-bit Linear PCM audio words. The SAI input port operates in slave mode only. The digital audio input from the SAI input port routes directly through the Sample Rate Converters (SRC). Either this I2S digital input or the S/PDIF digital input can be selected as the audio path source.

S/PDIF Digital Audio I/O

The D2-4 family contains one IEC60958 compliant S/PDIF Digital receiver input and one IEC60958 compatible S/PDIF Digital transmitter.

The S/PDIF receiver input includes an input transition detector, digital PLL clock recovery, and a decoder to separate the audio data. The receiver meets the jitter tolerance specified in IEC60958-4.

The S/PDIF transmitter complies with the consumer applications defined in IEC60958-3. The transmitter supports 24-bit audio data, but does not support user data and channel status. Compressed digital formats are not decoded within the D2-4 family. However, a bit-exact pass-through mode is supported from the SPDIFRX input to the SPDIFTX output, which allows for designs that require that the IEC61937-compliant original compressed audio input bitstream is made available at the product's S/PDIF output.

Sample Rate Converter

The D2-4 family devices include a 2-channel asynchronous Sample Rate Converter (SRC). This SRC converts audio data input sampled at one input sample rate to a fixed 48kHz output sample rate that aligns asynchronous input audio streams to a single rate for system processing. With an input sample rate from 16kHz to 192kHz, audio data presented to the SRC can be from either the SAI or S/PDIF input sources. In addition to converting the input sample rate to the output sample rate, input clock jitter and sampling jitter are attenuated by the SRC.

DSP

A 24-bit fixed-point Digital Signal Processor (DSP) controls the majority of audio processing and system control functions within the D2-4 family devices.

Audio path signal routing, programmable-parameter processing blocks, and control logic are defined within the device's internal firmware. Signal flows through the devices are buffered and processed through hardware specific-function blocks, such as the SCR.

Audio Processing And Signal Flow

The audio processing within the D2-4 family devices is defined by the internal ROM firmware and executed by the DSP. This firmware defines the audio flow architecture and the processing blocks used in that definition. Figure 6 on page 13 shows the signal flow for the D2-4 family devices. General audio processing functions within this architecture include:

- Matrix mixers
- Routers
- Compressors and limiters
- Tone controls
- Multi-band equalizers (fully parametric and shelving)
- High-pass and low-pass crossover filters
- Volume and level controls
- Loudness compensation
- Input signal selection

Signal flow and total system definition is defined by the internal device firmware; however, each block is programmable, which allows for adjustment of all of their parameters. Signal flow and details of each of these audio processing blocks are shown in Figure 6.
FIGURE 5. D2-4 FAMILY FUNCTIONAL BLOCK DIAGRAM

- LINEAR INTERPOLATOR
- PWM CORRECTION
- NOISE SHAPER
- QUANTIZER
- OUTPUT DRIVE
- SPDIFRX
- SPDIFTX
- SERIAL AUDIO INTERFACE PORT (I2S DATA TYPE RECEIVER)
- SPI, I/O
- PLL
- SAMPLE RATE CONVERTERS
- INPUT SELECTION
- MIXERS, ROUTERS
- INPUT PROCESSING
- CONTROL, INITIALIZATION
- D2-4 FAMILY TONE CONTROLS
- MULTI-BAND EQUALIZERS
- HIGH/LOW-PASS CROSSOVERS
- LOUDNESS
- COMPRESSORS/LIMITERS
- INDIVIDUAL CHANNEL CONTROL
- VOLUME CONTROL
- ENHANCEMENT
- AUDIO PROCESSING ALGORITHMS (PART NUMBER DEPENDENT)

24-BIT FIXED-POINT DIGITAL SIGNAL PROCESSOR WITH 56-BIT MAC (SIGNAL PROCESSING AND CONFIGURATION BLOCKS DEFINED BY DEVICE ROM Firmware)

- S/PDIF DIGITAL AUDIO RECEIVER, TRANSMITTER
- SCLK
- SDIN
- LRCK
- MCLK
- nRESET
- nRSTOUT
- TEST
- IRQA
- IRQB
- XTALI
- XTALO
- 2-WIRE (I2C-COMPATIBLE)
- SDA
- SCL
- TIMERS, I/O
- TEMPREF/
- SCK
- TEMP1/
- MOSI
- VOL1/
- MISO
- VOL0/
- nSS
- TEMPCOM/
- TIO0
- NMUTE/
- TIO1
- PLLVDD
- PLLGND
- PWMVDD
- PWMGND
- RVDD
- RGND
- CVDD
- CGND

POWER SUPPLY PROTECT INPUTS
- PROTECT0
- PROTECT1
- PROTECT2

CONFIG, I/O
- PSSYNC/
- CFG1
- nERROR/
- CFG0
- PWM0
- PWM1
- PWM2
- PWM3
- PWM4
- PWM5
- PWM6
- PWM7

5 CHANNEL PULSE WIDTH MODULATOR ENGINE (D2 SOUND ENHANCEMENT ALGORITHM)

D2 SOUND ENHANCEMENT ALGORITHM

SRS WOW/HD® AUDIO PROCESSING FIRMWARE (ROM)
D2-4 Family Audio SOC function is defined by the D2-4 family internal firmware. However, their operation is not programmable, and their specific implementation is determined by the device hardware as general purpose inputs/outputs. These pins are implemented within multiple-purpose, where their functions are different depending on the device operating state. Functions of these pins are defined elsewhere in this document. These pins are used for driving output power stages, that are mapped to eight PWM output pins. Each of the PWM channels and their pins are used for driving output power stages, and/or for line level outputs, depending on the selected configuration mode. The D2-4 family devices incorporate five PWM output channels that support multiple PWM amplifier output topologies. The outputs support multiple PWM amplifier output topologies. The channel and function assignment of the outputs to control amplifier and device operation. Some pins are included within specific part number options of the D2 Audio DSP Sound Enhancement Algorithm (with the D2-41051 device): Automatic loudspeaker setup/equalization/correction, Automatic room audio setup/equalization/optimization, Improved vocal clarity, Content/configuration EQ presets, Bass enhancement, 2-channel stereo spatialization. These enhancements within the signal flow is shown in Figure 6 on page 13. Additional enhancements audio processing algorithms are compatible peripheral chips. The I2C interface is multi-master interface, or for communication to EEPROMs, or other compatible peripheral chips. The I2C interface is usable with either an external microcontroller interface for communicating with an external controller. This interface supports normal and fast mode operation. The D2-4 family devices include a 2-Wire I2C compatible interface for SPI functions, and operate as assigned by the firmware. The four SPI interface pins are all shared. This interface functions internally by firmware and is not programmable. One timer is used for internal references, and the other is used for the temperature sensing control. Two I/O pins are associated with the timers, and their pin functions are defined by the device firmware. Timer 0 is used for the timing-related executions of the device. Its pin (TIO0) is used as an input port for external boot operation and does not operate as an interactive control port. During a reset condition, the four pins (TEMPREF/SCK, TEMP1/MOSI, VOL1/MISO, and VOL0/nSS) operate as the SPI port that provides an interface for loading parameter data from an optional EEPROM or Flash device during boot-up operation. The Serial Peripheral Interface (SPI) is an alternate serial input/output interface, and each parameter is defined with its specific register. The control register interface is used for an external controller to adjust the amplifier's programmable settings and adjustments. The control register interface is used for SPI functions, and operate as assigned by the firmware. As soon as the boot-up process is completed and the device begins executing its firmware program, these pins are no longer used for this timing operation, and is defined by device firmware. Timer operation is established internally by firmware and is not programmable. Timer operation is established internally by firmware and is not used for this timing operation, and is defined by device firmware. Timer 1 is used for internal functions of the device. Its pin (TIO1) is used as an input port for external temperature monitoring operation. Two independent timers are used for device and system control. One timer is used for internal references, and the other is used for the temperature sensing control. Two I/O pins are associated with the timers, and their pin functions are defined by the device firmware. Timer 1 is used for internal functions of the device. Its pin (TIO1) is used as an input port for external temperature monitoring operation. The Application Programming Interface (API) specification. All of these control register functions are defined in the API specification.
FIGURE 6. D2-4 Family AUDIO SIGNAL FLOW

PWM PIN OUTPUTS

2X2 MIXER

TONE 1

5 BAND EQ 1

COMPRESSOR 1

PWM CHANNEL 0

PWM CHANNEL 1

PWM CHANNEL 2

PWM CHANNEL 3

DIGITAL INPUT SELECT

S/PDIF DIGITAL INPUT

2X1 MIXER

SPEAKER EQ 1

4X4 ROUTER

LICENSED AUDIO PROCESSING ALGORITHM

*(SEE NOTE)

S/PDIF PWM CHANNEL 4

2 SRC I2S DIGITAL INPUT

COMPRESSOR 2

TONE 2

5 BAND EQ 2

SPEAKER EQ 2

HP 1

LP 1

HP 2

LP 2

HP 3

LP 3

HP 4

LP 4

HP 5

LP 5

3 BAND EQ 1

3 BAND EQ 1

3 BAND EQ 1

3 BAND EQ 1

MASTER VOLUME CONTROL

LOUDNESS 1

LOUDNESS 2

LOUDNESS 3

LOUDNESS 4

LOUDNESS 5

LIMITER 1

LIMITER 2

LIMITER 3

LIMITER 4

LIMITER 5

VOLUME 1

VOLUME 2

VOLUME 3

VOLUME 4

VOLUME 5

CROSSOVERS

5 4 3 2 1

5 4 3 2 1

5 4 3 2 1

5 4 3 2 1

* NOTE: DEVICE DEPENDENT LICENSED AUDIO PROCESSING ALGORITHM SUPPORTING D2 SOUND ENHANCEMENT ALGORITHM, OR SRS WOW/HD. REFER TO DEVICE ORDER INFORMATION FOR PART NUMBER SPECIFYING EACH ALGORITHM.
D2-4 Family Audio SOC system initialization. The I2C bus is busy as a master device. After the device firmware initializes and begins running, this error output is active low and only becomes used as an output after the device firmware begins operating. This pin becomes the PSSYNC pin, also determining which protection inputs are used.

- **Overcurrent Sensing**
  - The detectors' purpose is to generate a pulse or logic level upon detection of high current, where this logic level is connected to the amplifier's design to monitor system temperature. The temperature sensing algorithm uses external hardware on the amplifier design to monitor system temperature. This operation uses three of the I/O pins (TEMPREF/SCK, TEMP1/MOSI, and TEMPCOM/TIO1). These pins have shared functions. During device initialization, these pins operate as part of the SPI interface; however, after the firmware is executing, the temperature sensing function switches to the normal operation used for temperature monitoring.

- **Power Supply Synchronization**
  - The PSSYNC/CFG1 pin provides a power supply synchronization signal for switching power supplies. Firmware configures this pin to the frequency and duty cycle needed by the system switching. This synchronization allows switching supplies used at each power stage output to the frequency and duty cycle needed by the system switching. The PSSYNC/CFG1 pin is a shared pin. During device reset and supply is not locked to the amplifier switching. The chip contains power rail sensors and brownout detectors on both the 3.3V and 1.8V power supplies. A loss or droop of power from either of these supplies triggers their brownout detectors, which assert the nRSTOUT pin, driving it low. Connect the nRSTOUT pin and connect to the nRESET input to initiate the reset process. The chip contains power rail sensors and brownout detectors on the 3.3V and 1.8V supplies from that 5V source. As noted in Note 7, the 3.3V and 1.8V supplies are powersupplied to the chip by the regulator. The PLLVDD may be brought up together to avoid high current transients that could fold back a power supply regulator. The CVDD and RVDD (including PWMVDD) power supplies should be brought up together to avoid high current transients that could fold back a power supply regulator. The CVDD and RVDD (including PWMVDD) power supplies should be brought up together to avoid high current transients that could fold back a power supply regulator.

- **Error Reporting**
  - The system and device internal monitoring uses an I/O pin (nERROR/CFG1) as an output to signal a channel shutdown error. nERROR/CFG1 is shared by the system and device internal monitoring. When the error output is low, the system's design (PCB) asserts the nRSTOUT pin, driving it low. Connect the nRSTOUT pin and connect to the nRESET input to initiate the reset process. The error output is also used to signal an external microcontroller. This output can be used to turn on a simple indicator.

- **Clock and PLL**
  - The clock generation contains a low jitter PLL critical for low phase noise and is designed only to drive the crystal and does not connect to the crystal. The clock is generated on-chip using a fundamental-mode crystal connected across the XTALI and XTALO pins. XTALO is an output, and the crystal frequency is connected to XTALI. The clock generation contains a low jitter PLL critical for low phase noise. The clock frequency is connected to XTALI. The clock generation contains a low jitter PLL critical for low phase noise.

- **Boo Modes**
  - Boot mode is initiated by applying a low level to the nRESET input through hardware on the amplifier design to the nRESET input. At the deassertion of nRESET, the chip reads the status of the pins' logic state. These device pins are strapped either high or low on the system's design (PCB). Boot mode operation is defined by the state of these pins that is latched into. See the section for related descriptions.
**Boot Modes**

The D2-4 family devices contain internal firmware to operate the part and run the amplifier system. Parameter information used by the programmable settings can be written to the device after it is operational and running. Parameter data can also be read at boot time, which allows saved parameter settings to be used in processing. The device is designed to boot in one of four possible modes, allowing control and data to be provided from these boot sources:

- **I²C slave (to external microcontroller)**
- **I²C EEPROM**
- **Internal device ROM only**
- **SPI slave**

The specific boot mode is selected based on the state of the IRQB and IRQA input pins at the time of reset de-assertion. Boot modes are shown in Table 1.

The device initializes as defined by its boot mode; however, it gets its configuration and parameter data from the host device. This host device can be either an external controller or from an EEPROM. If a system uses both an external controller and an EEPROM, the EEPROM loads first. During this time, the controller must remain off the I²C bus.

**Output Mode Configurations**

The D2-4 family devices support four amplifier output configuration modes of powered output and line output combinations. These four modes are shown in Table 2.

These configuration modes use different combinations of the five PWM output channels, and each mode maps the eight PWM pins to their appropriate PWM channel path. This channel content and mapping of the pins is shown in Table 3 on page 16. Of the total eight PWM pins, not all pins are used with every configuration mode. Timing and drive characteristics of each PWM pin output are automatically programmed for correct operation when those pins are connected to their designated output stages.

In Modes 2 and 3, the filtering for high and low pass crossovers is applied to the audio signal flow path, enabling the appropriate high or low pass content to be properly filtered for the PWM output channels.

The protect pin inputs are mapped to the PWM channels that are used for the powered outputs. This protect pin mapping assignment is shown in Table 3 for the different configurations.

**Configuration Mode Assignment**

The configuration mode is assigned when the D2-4 family device exits its reset state. At that time, the logic status of the PSSYNC/CFG1 and nERROR/CFG0 pins are latched into internal device registers. During this initialization time, these pins operate as logic inputs. After completion of the initialization and the internal firmware begins executing, these pins are reassigned as outputs for their shared functions. The internal latched logic state that defines the configuration mode remains until the device is powered down or reset again. Each mode requires a specific amplifier design hardware connection, and the configuration pin logic levels are defined through pull-up or pull-down resistors installed on that design's board. These modes are not programmable and are not intended to be changed for each hardware design.

<table>
<thead>
<tr>
<th>TABLE 1. BOOT MODE SETTINGS</th>
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<tr>
<td>101</td>
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<tr>
<td>210</td>
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<tr>
<th>TABLE 2. D2-4 1x51 OUTPUT CONFIGURATION MODES</th>
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<td><strong>CONFIG MODE NAME</strong></td>
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</tr>
<tr>
<td>12.0 L/R</td>
</tr>
<tr>
<td>22.1 L/R/Sub</td>
</tr>
<tr>
<td>32.2 Bi-Amp</td>
</tr>
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<td>CONFIG</td>
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<tr>
<td>--------</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>02.0 L/R</td>
</tr>
<tr>
<td>12.0 L/R</td>
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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

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<tr>
<td>Mar 19, 2019</td>
<td>FN6783.2</td>
<td>Changed the base parts on page 1 in header to D2-4 Family Audio SOC.</td>
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<td>Updated Related Literature section.</td>
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<td>Replaced all words named &quot;D2AudioTM&quot; to &quot;D2 Audio DSP&quot;; &quot;DAE-4&quot; to &quot;D2-4 family&quot;; &quot;Digital Audio Engine&quot; to &quot;Digital Audio Processor&quot;; &quot;SoundSuite&quot; to &quot;Sound Enhancement Algorithm&quot;; &quot;DSP Canvas II&quot; to &quot;D2 Audio Customization GUI&quot;.</td>
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<td>Updated Audio Enhancement Feature Processing bullet points on page 10.</td>
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<td>Updated links throughout document.</td>
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<td>Updated Figures 1, 2, 3, 4, 5, and 6.</td>
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May 5, 2016

FN6783.1

Updated entire datasheet applying Intersil's new standards.

Updated the Ordering Information table on page 3.

Updated Note 8 on page 6.

Added the Disclaimer for DTS® (SRS) Technology License Required Notice.

Added Revision History section.

Replaced Products verbiage to About Intersil verbiage.

Updated POD to the latest revision changes as follows:

- Corrected Note 4 from: "Dimension b applies to..." to: "Dimension applies to..." 'b' leftover from when dimensions were in table format.
- Enclosed Notes #'s 4, 5 and 6 in a triangle.
NOTES:

1. Dimensions are in millimeters.
2. Element 6.20 or mark feature.
3. Element 6.30 ± 0.15 (4X).
4. Element 44X0.50 (4X).
5. Element 4X5.5 (4X).
6. Element 4X0.60 (4X).
7. Element 48X0.40 (4X).
8. Element 0.00 MIN.
9. Element 0.05 MAX.

Element 136:

- Element 25 
- Element 24 
- Element 13 
- Element 0.90 ± 0.1

Element 0.10:

- Element 0.08 SEE DETAIL "X"
- Element 0.10

Element 0.23:

- Element 0.23 +0.07 / -0.05

- Element 6 (6.80 TYP)
- Element 4 (4.30)
- Element 48X (48X 0.23)