D2-4 Family Audio SOC

Intelligent Digital Amplifier PWM Controller and Audio Processor

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The D2-4 Family (D2-41051 and D2-41151 (D2-41x51-QR)) devices are complete System-on-Chip (SoC) Audio Processor and Class-D Amplifier Controllers that offer a powerful yet very cost effective audio solution for high volume consumer products, including digital TV systems, PC multimedia speakers, and portable device docking stations. This 4th generation Digital Audio Processor (D2-4 family) device combines extensive integrated DSP processing and configurable audio processing algorithms for complete audio system control.

The D2-4 family devices offer the optimum balance of functionality and lowest system material cost, especially in an SoC system architecture with I^{2}S audio output. All audio processing and amplifier control is handled by the D2-4 family, and its ease of integration to the existing system processor handles all system control functions.

Related Literature

For a full list of related documents, visit our website:

- D2-41051 and D2-41151 device pages

Features

- All digital class-D amplifier controller with integrated Digital Signal Processing (DSP)
- Fully programmable audio signal path parameters
- Up to 5 channels of Digital Signal Processing (DSP)
- Includes equalizers, filters, mixers, and other common audio processing blocks
- Audio enhancement algorithms included
- I^{2}S and S/PDIF™ digital audio stereo inputs
- I^{2}C host control port
- Asynchronous sample rate converters, sample rates from 32kHz up to 192kHz
- Supports 2.0, 2.1, or bi-amp amplifier outputs with discrete or integrated power stages

Applications

- PC/multimedia speakers
- Digital TV audio systems
- Portable device docking stations
- Powered speaker systems

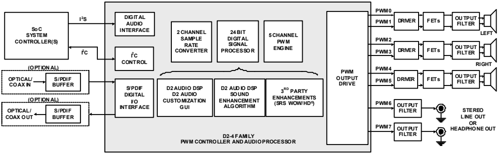

FIGURE 1. TYPICAL APPLICATION

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Ordering Information

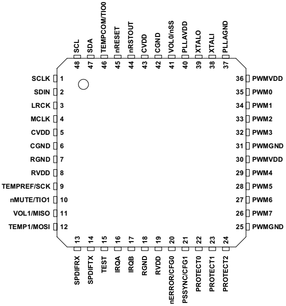
PART NUMBER (Notes 3, 4)	AUDIO PROCESSING FEATURE SET SUPPORT (Note 2)	PART MARKING	TEMP RANGE (°C)	TAPE AND REEL (Units)	PACKAGE (RoHS Compliant)	PKG. DWG. #
D2-41051-QR	D2 Audio DSP Sound Enhancement Algorithm	D2-41051-QR	-10 to +85	-	48 Ld QFN	L48.7x7
D2-41051-QR-TK (Note 1)	D2 Audio DSP Sound Enhancement Algorithm	D2-41051-QR	-10 to +85	1k	48 Ld QFN	L48.7x7
D2-41151-QR	D2 Audio DSP Sound Enhancement Algorithm DTS®(SRS) WOW/HD™	D2-41151-QR	-10 to +85	-	48 Ld QFN	L48.7x7
D2-41151-QR-TK (Note 1)	D2 Audio DSP Sound Enhancement Algorithm DTS®(SRS) WOW/HD™	D2-41151-QR	-10 to +85	1k	48 Ld QFN	L48.7x7

NOTES:

1. See TB347 for details about reel specifications.
2. The D2-4 family supports audio processing algorithms for the D2 Audio DSP Sound Enhancement Algorithm, and DTS®(SRS) WOW/HD® audio enhancement features. Algorithm support of these enhancements is device-dependent. See the specific part number for desired feature support.
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). The Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see the D2-41051 and D2-41151 device pages. For more information about MSL, see TB363.

Pin Configuration

48 LD QFN
TOP VIEW



D2-4 Family Pin Descriptions

PIN	PIN NAME (Notes 5, 7)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA) (Note 6)	DESCRIPTION
1	SCLK	I	3.3	-	I^2S serial audio bit clock (SCLK) Input. Input has hysteresis.
2	SDIN	I	3.3	-	I^2S serial audio data (SDIN) Input. Input has hysteresis.
3	LRCK	I	3.3	-	I^2S serial audio left/right (LRCK) Input. Input has hysteresis.
4	MCLK	O	3.3	16	I^2S serial audio master clock output for external ADC/DAC components, drives low on reset. Output is an 8mA driver.
5, 43	CVDD	P	3.3	-	Core power, $+1.8V_{DC}$. Used in the chip internal DSP, logic, and interfaces.
6, 42	CGND	P	3.3	-	Core ground
7, 18	RGND	P	3.3	-	Digital pad ring ground. Internally connected to PWMGND.
8, 19	RVDD	P	3.3	-	Digital pad ring power, 3.3V. These 3.3V supplies are used for all the digital I/O pad drivers and receivers, except for the analog pads. Both are required to be connected. Internally connected to PWMVDD.
9	TEMPREF/ SCK	I/O	3.3	4	Reference pin for the temperature monitor and SPI clock. At deassertion of device reset, this pin operates as a SPI clock. Upon internal D2-4 family firmware execution, this pin becomes a temperature monitor reference.
10	nMUTE/ TIO1	O	3.3	16	Mute signal output. When active low, the mute condition drives this pin low. Output is a 16mA driver. Initializes as an input on reset, then becomes an output upon internal firmware execution.
11	VOL1/ MISO	I/O	3.3	4	Volume control pulse input and SPI master-input/slave-output data signal. At deassertion of device reset, this pin operates as a SPI master input or slave output. Upon internal D2-4 family firmware execution, this pin becomes an input for monitoring up/down phase pulses from volume control (one of two volume input pins).
12	TEMP1/ MOSI	I/O	3.3	4	Temperature monitor pin and SPI master-output/slave-input data signal. At deassertion of device reset, this pin operates as a SPI master output or slave input. Upon internal D2-4 family firmware execution, this pin becomes an input for monitoring temperature.
13	SPDIFRX	I	3.3	-	S/PDIF digital audio data input.
14	SPDIFTX	O	3.3	8	S/PDIF digital audio data output. This pin is the S/PDIF audio output and drives an 8mA, 3.3V stereo output up to 192kHz. Pin floats on reset.
15	TEST	I	3.3	-	Hardware test mode control. For factory use only. Must be tied low.
16	IRQA	I	3.3	-	Interrupt request port A. One of two IRQ pins, tied to logic (3.3V) high or to ground. High/low logic status establishes boot mode selection upon deassertion of the reset (nRESET) cycle.
17	IRQB	I	3.3	-	Interrupt request port B. One of two IRQ pins, tied to logic (3.3V) high or to ground. High/low logic status establishes boot mode selection upon deassertion of the reset (nRESET) cycle.
20	nERROR/ CFG0	I/O	3.3	4	Output configuration selection input, and nERROR output. Upon device reset, this pin operates as an input, using application-installed pull-up or pull-down connection to the pin to specify one of four amplifier configurations. Upon internal D2-4 family firmware execution, this pin becomes an output and provides an active-low output drive when the amplifier protection monitoring detects an error condition.
21	PSSYNC/ CFG1	I/O	3.3	4	Output configuration selection input and power supply sync output. Upon device reset, this pin operates as an input, using application-installed pull-up or pull-down connection to the pin to specify one of four amplifier configurations. Upon internal D2-4 family firmware execution, this pin becomes an output and provides a synchronizing signal to the on-board power supply circuits.

D2-4 Family Pin Descriptions (Continued)

PIN	PIN NAME (Notes 5, 7)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA) (Note 6)	DESCRIPTION
22	PROTECT0	I/O	3.3	4	PWM protection input. Input has hysteresis. Protection monitoring functionality of these pins is controlled by an internal D2-4 family firmware, and dependent on which of the four amplifier configurations is enabled.
23	PROTECT1	I/O	3.3	4	
24	PROTECT2	I/O	3.3	4	
25, 31	PWMGND	P	3.3	-	PWM output pin ground. Internally connected to RGND.
26	PWM7	I/O	3.3	8 or 16	PWM outputs. Output is 8mA or 16mA, depending on the output mode configuration setting. Pins float on reset.
27	PWM6	I/O	3.3	8 or 16	
28	PWM5	I/O	3.3	8 or 16	
29	PWM4	I/O	3.3	8 or 16	
30, 36	PWMVDD	P	3.3	-	PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.
32	PWM3	I/O	3.3	8 or 16	PWM outputs. Output is 8mA or 16mA, depending on the output mode configuration setting. Pins float on reset.
33	PWM2	I/O	3.3	8 or 16	
34	PWM1	I/O	3.3	8 or 16	
35	PWM0	I/O	3.3	8 or 16	
37	PLLAGND	P	1.8	-	PLL analog ground
38	XTALI	P	1.8	-	Crystal oscillator analog input port.
39	XTALO	P	1.8	-	Crystal oscillator analog output port. This output drives the crystal and XTALO does not have a drive strength specification.
40	PLLAVDD	P	1.8	-	PLL analog power, 1.8V
41	VOLO/ nSS	I/O	3.3	4	Volume control pulse input and SPI slave select. At deassertion of device reset, this pin operates as a SPI slave select input. Upon internal D2-4 family firmware execution, this pin becomes an input for monitoring up/down phase pulses from volume control (one of two volume input pins).
44	nRSTOUT	O	3.3	16 -OD	Active low output. This pin drives low from the 3.3V brownout detector or 1.8V brownout detector going active. Use this output to initiate a system reset to the nRESET pin upon brownout event detection.
45	nRESET	I	3.3	-	Active low reset input with hysteresis. Low level activates system level reset, initializing all internal logic and program operations. System latches boot mode selection on the IRQ input pins on the rising edge.
46	TEMPCOM/ TIO0	I/O	3.3	16	Temperature monitor common I/O pin.
47	SDA	I/O	3.3	8- OD	Two-Wire serial data port, open-drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport. Pin floats on reset.
48	SCL	I/O	3.3	8- OD	Two-Wire serial clock port, open-drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for clock signaling. Pins floats on reset.

NOTES:

5. All pin names are active high, unless otherwise specified. Pins that are active low have an “n” prefix, such as nRESET.
6. OD means the pad has an open-drain driver.
7. All power and ground pins of the same names must be tied together to all other pins of their same name (for example, tie the RVDD pins together, RGND pins together, CVDD pins together, CGND pins together, PWMVDD pins together, and PWMGND pins together.)

Absolute Maximum Ratings (Note 10)

Supply Voltage	
RVDD, PWMVDD	-0.3V to 4.0V
CVDD, PLLVDD	-0.3V to 2.4V
Input Voltage	
Any Input but XTALI	-0.3V to RVDD + 0.3V
XTALI	-0.3V to PLLVDD + 0.3V
Input Current, any Pin but Supplies	±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld QFN (Notes 8, 9)	27	2
Temperature Range (Operating)	0°C to +70°C	
Maximum Storage Temperature	-55°C to +150°C	
Pb-Free Reflow Profile	see TB493	

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

8. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
9. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
10. Absolute Maximum parameters are not tested in production.

Recommended Operating Conditions

T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Core Supply Pins	CVDD	1.7	1.8	1.9	V
Active Current		-	300	-	mA
Power-Down Current (Note 11)		-	6	-	mA
Digital I/O and PWM Pad Ring Supply Pins	RVDD and PWMVDD	3.0	3.3	3.6	V
Active Current		-	10	-	mA
Power-Down Current (Note 11)		-	0.01	-	mA
Analog Supply Pins (PLL)	PLLVDD	1.7	1.8	1.9	V
Active Current		-	10	-	mA
Power-Down Current (Note 11)		-	5	-	mA

NOTE:

11. Power Down is with device in reset and clocks stopped.

Electrical Specifications

T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital Input High Logic Level (Note 12)	V_{IH}	2	-	-	V
Digital Input Low Logic Level (Note 12)	V_{IL}	-	-	0.8	V
High Level Output Drive Voltage (Note 13) (I_{OUT} = -Pad Drive)	V_{OH}	RVDD - 0.4	-	-	V
Low Level Output Drive Voltage (Note 13) (I_{OUT} = +Pad Drive)	V_{OL}	-	-	0.4	V
High Level Input Drive Voltage XTALI Pin	V_{IHX}	0.7	-	PLLVDD	V
Low Level Input Drive Voltage XTALI Pin	V_{ILX}	-	-	0.3	V
Input Leakage Current (Note 14)	I_{IN}	-	-	±10	µA
Input Capacitance	C_{IN}	-	9	-	pF
Output Capacitance	C_{OUT}	-	9	-	pF
nRESET Pulse Width	Trst	-	10	-	ns

Electrical Specifications

T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic. **(Continued)**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CRYSTAL OSCILLATOR					
Crystal Frequency (Fundamental Mode Crystal)	Xo	20	24.576	25	MHz
Duty Cycle	Dt	40	-	60	%
Start-Up Time (Start-Up Time is Oscillator enabled (with Valid Supply) to Stable Oscillation)	Tstart	-	5	20	ms
PLL					
VCO Frequency	Fvco	240	294.912	300	MHz
PLL Lock Time from any Input Change		-	3	-	ms
1.8V POWER ON RESET					
Reset Enabled Voltage Level	Ven	0.95	1.10	1.30	V
POR Minimum Output Pulse Width	Tdis	-	5	-	µs
1.8V BROWNOUT DETECTION					
Detect Level		1.4	1.5	1.7	V
Pulse Width Rejection	Tbod1	-	100	-	ns
Minimum Output Pulse Width	To1	-	20	-	ns
3.3V (CVDD) BROWNOUT DETECTION					
Detect Level		2.4	2.7	2.9	V
Pulse Width Rejection	Tbod3	-	100	-	ns
Minimum Output Pulse Width	To3	-	20	-	ns

NOTES:

12. All input pins except XTALI.

13. All digital output pins. Drive strength for each digital pin is in the "D2-4 Family Pin Descriptions" on page 4.

14. Input leakage applies to all pins except XTALO.

Serial Audio Interface Port Timing

T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%, XTALI = 24.576MHz, NESSI clock polarity = 1. All grounds at 0.0V. All voltages referenced to ground.

DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency - (SCLK)	t_CSCLK	-	-	12.5	MHz
SCLK Pulse Width (HIGH and LOW) - (SCLK)	t_WSCLK	40	-	-	ns
LRCKR Set-Up to SCLK Rising - (LRCK)	t_SLRCLK	20	-	-	ns
LRCKR Hold from SCLK Rising - (LRCK)	t_hLRCLK	20	-	-	ns
SDIN Set-Up to SCLK Rising - (SDIN)	t_SSDI	20	-	-	ns
SDIN Hold from SCLK Rising - (SDIN)	t_hSDI	20	-	-	ns

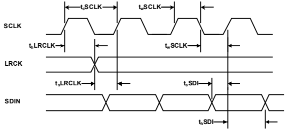


FIGURE 2. SERIAL AUDIO INTERFACE PORT TIMING

Two-Wire (I^{2}C) Interface Port Timing

T_A = +25° C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNIT
SCL Frequency	fSCL	-	-	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7	-	-	µs
SCL Clock Low	t_{wlow}SCLx	4.7	-	-	µs
SCL Clock High	t_{whigh}SCLx	4.0	-	-	µs
Set-Up Time for a (Repeated) Start	t_sSTA	4.7	-	-	µs
Start Condition Hold Time	t_hSTA	4.0	-	-	µs
SDA Hold from SCL Falling (See Note 15)	t_hSDAx	-	1	-	sys clk
SDA Set-Up Time to SCL Rising	t_sSDAx	250	-	-	ns
SDA Output Delay Time from SCL Falling	t_dSDAx	-	-	3.5	µs
Rise Time of Both SDA and SCL (See Note 16)	t_r	-	-	1	µs
Fall Time of Both SDA and SCL (See Note 16)	t_f	-	-	300	ns
Set-Up Time for a Stop Condition	t_sSTO	4.7	-	-	µs

NOTES:

15. Data is clocked in as valid on next XTALI rising edge after SCL goes low.
16. Limits established by characterization and not production tested.

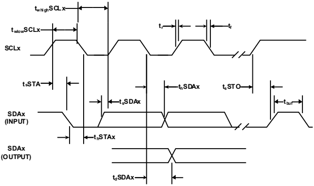


FIGURE 3. I^{2}C INTERFACE TIMING

SPI™ Master Mode Interface Port Timing

T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_V	MOSI Valid from Clock Edge	-	8	ns
t_S	MISO Set-Up to Clock Edge	10	-	ns
t_H	MISO Hold from Clock Edge	1 system clock + 2ns		
t_{WI}	nSS Minimum Width	3 system clocks + 2ns		

SPI™ Slave Mode Interface Port Timing

T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_V	MISO Valid from Clock Edge	3 system clocks + 2ns		
t_S	MOSI Set-Up to Clock Edge	10	-	ns
t_H	MOSI Hold from Clock Edge	1 system clock + 2ns		
t_{WI}	nSS Minimum Width	3 system clocks + 2ns		

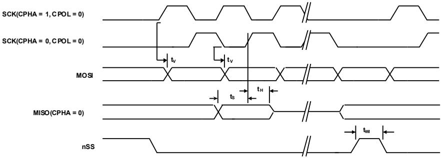


FIGURE 4. SPI TIMING

Overview

The D2-4 family devices are integrated System-on-Chip (SoC) audio processors and Class D amplifier PWM controllers. They include complete digital audio input selection, signal routing, complete audio processing, and selectable PWM output options for driving multiple output power stage configurations. Stereo I^2S and stereo S/PDIF digital input support, plus I^2C and 2-wire SPI control interfaces enable integration compatibility with existing system architectures and solutions. The audio path includes a stereo Sample Rate Converter (SRC) plus device-specific audio enhancement processing algorithms.

Output Configurations

A 5-channel PWM engine with application-selected configuration settings provides output paths for combinations of output channels. Application dependent configuration selection includes PWM controller outputs for driving Stereo Speaker, 2.1 Speaker, and Stereo Bi-Amp Speaker solutions, as well as Stereo Line, Headphone Outputs, or Subwoofer Line Outputs. Depending on configuration settings, Full-Bridge, Half-Bridge and Bridge-Tied-Load (BTL) output stage topologies, with either discrete or integrated output stages are supported.

Programmable Audio Processing

Programmable parameter settings for audio processing include volume control, path routing and mixing, high/low pass filtering, multi-band equalizers, compressors, and loudness. These parameters can be adjusted using the D2 Audio Customization GUI software during design and development, or can be set through the device's control interface within production amplifier products.

Typical Performance

Final system performance is largely determined by the amplifier configuration, its choice of output power stages and components, and overall system design. Typical performance capability of amplifier power outputs varies from less than 10Ws to systems over 150W. System audio performance includes 20Hz to 20kHz frequency response, SNR of greater than 100dB, and THD+N performance typically below 0.1%.

Audio Enhancement Processing

The D2-4 family devices include D2 Audio DSP Sound Enhancement Algorithm (within the D2-41051 device) and DTS®(SRS) WOW/HD™ (within the D2-41151 device) audio enhancement algorithms. These functions are integrated within the firmware of each device and are part of the standard audio signal flow.

Functional Description

Figure 5 on page 11 shows a block diagram of the D2-4 family devices and serves as a reference for many of the items in the following descriptions.

Serial Audio Digital Input

The D2-4 family devices include one Serial Audio Interface (SAI) port accommodating two channels of digital audio input. This SAI port supports the I^{2}S digital audio industry standard, and can carry up to 24-bit Linear PCM audio words. The SAI input port operates in slave mode only. The digital audio input from the SAI input port routes directly through the Sample Rate Converters (SRC). Either this I^{2}S digital input or the S/PDIF digital input can be selected as the audio path source.

S/PDIF Digital Audio I/O

The D2-4 family contains one IEC60958 compliant S/PDIF Digital receiver input and one IEC60958 compatible S/PDIF Digital transmitter.

The S/PDIF receiver input includes an input transition detector, digital PLL clock recovery, and a decoder to separate the audio data. The receiver meets the jitter tolerance specified in IEC60958-4.

The S/PDIF transmitter complies with the consumer applications defined in IEC60958-3. The transmitter supports 24-bit audio data, but does not support user data and channel status.

Compressed digital formats are not decoded within the D2-4 family. However, a bit-exact pass-through mode is supported from the SPDIFRX input to the SPDIFTX output, which allows for designs that require that the IEC61937-compliant original compressed audio input bitstream is made available at the product's S/PDIF output.

Sample Rate Converter

The D2-4 family devices include a 2-channel asynchronous Sample Rate Converter (SRC). This SRC converts audio data input sampled at one input sample rate to a fixed 48kHz output sample rate that aligns asynchronous input audio streams to a single rate for system processing. With an input sample rate from 16kHz to 192kHz, audio data presented to the SRC can be from either the SAI or S/PDIF input sources. In addition to converting the input sample rate to the output sample rate, input clock jitter and sampling jitter are attenuated by the SRC.

DSP

A 24-bit fixed-point Digital Signal Processor (DSP) controls the majority of audio processing and system control functions within the D2-4 family devices.

Audio path signal routing, programmable-parameter processing blocks, and control logic are defined within the device's internal firmware. Signal flows through the devices are buffered and processed through hardware specific-function blocks, such as the SCR.

Audio Processing And Signal Flow

The audio processing within the D2-4 family devices is defined by the internal ROM firmware and executed by the DSP. This firmware defines the audio flow architecture and the processing blocks used in that definition. Figure 6 on page 13 shows the signal flow for the D2-4 family devices. General audio processing functions within this architecture include:

- Matrix mixers
- Routers
- Compressors and limiters
- Tone controls
- Multi-band equalizers (fully parametric and shelving)
- High-pass and low-pass crossover filters
- Volume and level controls
- Loudness compensation
- Input signal selection

Signal flow and total system definition is defined by the internal device firmware; however, each block is programmable, which allows for adjustment of all of their parameters.

Signal flow and details of each of these audio processing blocks are shown in Figure 6.

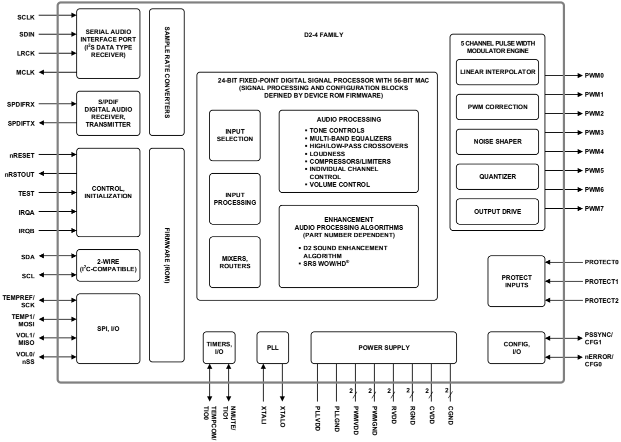


FIGURE 5. D2-4 FAMILY FUNCTIONAL BLOCK DIAGRAM

Audio Enhancement Feature Processing

Additional enhancement audio processing algorithms are included within specific part number options of the D2-4 family devices. These specific enhancements are:

D2 Audio DSP Sound Enhancement Algorithm (with the D2-41051 device):

- 2-channel stereo spatialization
- Bass enhancement
- Content/configuration EQ presets
- Improved vocal clarity
- Automatic room audio setup/equalization/optimization
- Automatic loudspeaker setup/equalization/correction
- DTS®SRS WOW/HD™ (with the D2-41151 device)

Each of these enhancements are unique to the particular part number, and each enhancement has its own set of programmable parameters to control operation. The location of these enhancements within the signal flow is shown in Figure 6 on page 13.

PWM Audio Outputs

The D2-4 family devices incorporate five PWM output channels that are mapped to eight PWM output pins. Each of the PWM channels and their pins are used for driving output power stages, and/or for line level outputs, depending on the selected configuration mode.

The outputs support multiple PWM amplifier output topologies. These supported topologies include half-bridge N+N or N+P, and full-bridge N+N or N+P using 2-level modulation with 2 or 4-quadrant control. The channel and function assignment of the eight output pins as well as the associated output topology is established by the output mode configuration settings. See "Output Mode Configurations" on page 15 for a description and selection of these output configurations, and their associated mapping of the PWM output pins.

Using a simple passive filter, the PWM outputs drive line-level outputs at a nominal $1V_{rms}$. Headphone outputs or line-level outputs that require a $2V_{rms}$ or higher output level are implemented using an active filter.

I/O Control Pins

Several device pins are used as specific-function inputs and outputs to control amplifier and device operation. Some pins are multiple-purpose, where their functions are different depending on the device operating state. Functions of these pins are defined in "D2-4 Family Pin Descriptions" on page 4, and additional descriptions are included within the functional block descriptions elsewhere in this document. These pins are implemented within the device hardware as general purpose inputs/outputs. However, their operation is not programmable, and their specific function is defined by the D2-4 family internal firmware.

Timers

Two independent timers are used for device and system control. One timer is used for internal references, and the other is used for the temperature sensing control. Two I/O pins are associated with the timers, and their pin functions are defined by the device firmware. Timer 0 is used for the timing-related executions of the temperature monitoring algorithm. Its pin (TIO0) is used as an input and output for that temperature monitoring operation. Timer 1 is used for internal functions of the device. Its pin (TIO1) is not used for this timing operation, and is defined by device firmware as the nMUTE I/O pin. Timer operation is established internally by firmware and is not programmable.

I^2C 2-Wire Control Interface

The D2-4 family devices include a 2-Wire I^2C compatible interface for communicating with an external controller.

This interface is usable with either an external microcontroller interface, or for communication to EEPROMs, or other compatible peripheral chips. The I^2C interface is multi-master capable, operates as independent master and slave, and supports normal and fast mode operation.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is an alternate serial input port that provides an interface for loading parameter data from an optional EEPROM or Flash device during boot-up operation.

The four SPI interface pins are all shared. This interface functions only as an input port for external boot operation and does not operate as an interactive control port. During a reset condition, initiating the boot-up process, the four pins (TEMPREF/SCK, TEMP1/MOSI, VOL1/MISO, and VOL0/nSS) operate as the SPI port. As soon as the boot-up process is completed and the device begins executing its firmware program, these pins are no longer used for SPI functions, and operate as assigned by the firmware.

Control Register Summary

The control register interface is used for an external controller to adjust the amplifier's programmable settings and adjustments within its signal flow. The parameters for each of the signal processing blocks are accessed through a register programming interface, and each parameter is defined with its specific register address. Audio input selection (I^2S input or S/PDIF receiver input) and output elements (PWM amplifier and line outputs, and S/PDIF transmitter) are controlled through their register parameters.

All of these control register functions are defined in the Application Programming Interface (API) specification.

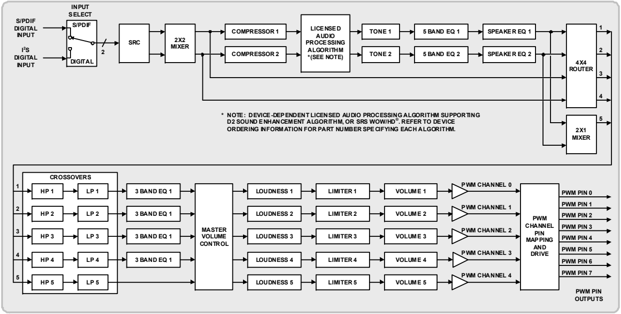


FIGURE 6. D2-4 Family AUDIO SIGNAL FLOW

Temperature Sensing

The temperature sensing algorithm uses external hardware on the amplifier's design to monitor system temperature. This external hardware includes a Negative Temperature Coefficient (NTC) resistor located physically on the design in areas that require monitoring.

This operation uses three of the I/O pins (TEMPREF/SCK, TEMP1/MOSI, and TEMPCOM/TIO1). These pins have shared functions. During device initialization, these pins operate as part of the SPI interface; however, after the firmware is executing, the SPI functionality turns off and these pins are dedicated to the temperature monitoring function.

Overcurrent Sensing

The device senses overcurrent with current threshold detectors connected in the power supply used at each power stage output of the amplifier design.

The detectors' purpose is to generate a pulse or logic level upon detection of high current, where this logic level is connected to one of the three protection input (PROTECT[0:2]) pins.

These protection input pins are primarily intended for protecting the PWM powered output stages. They are activated by either a pulse or level driven into the pin. Firmware within the D2-4 family devices monitors the internal hardware connected to these pins and adjusts or disables the PWM output drive, depending on the conditions monitored on these protection input pins.

The number of powered outputs in a design depends on which one of the four configurations is defined. The configuration settings, established upon device reset through the configuration pins, also determine which protection inputs are used.

Power Supply Synchronization

The PSSYNC/CFG1 pin provides a power supply synchronization signal for switching power supplies. Firmware configures this pin to the frequency and duty cycle needed by the system switching regulator. This synchronization allows switching supplies used with the device to operate without generating in-band audio interference signals that could occur if the switching power supply is not locked to the amplifier switching.

This PSSYNC/CFG1 pin is a shared pin. During device reset and initialization, the pin operates as one of two configuration input pins, where its high or low logic state is used to set the amplifier configuration mode. After completion of reset and when the device firmware begins operating, this pin becomes the PSSYNC output.

Error Reporting

The system and device internal monitoring uses an I/O pin (nERROR/CFG1) as an output to signal a channel shutdown error condition to an external system controller. This output can be used to turn on a simple indicator.

The error output is also used to signal an external microcontroller that the I^2C bus may be busy. When the error output is low during system initialization, the I^2C bus is busy as a master device.

This error output is active low and only becomes used as an output after the device firmware initializes and begins running. This same pin is shared as an input. During a reset condition, this pin operates as an input and is one of two input pins that are used to define the configuration mode. A resistor pull-up or pull-down on this pin establishes the mode input configuration state. After the initialization sequence completes, these resistors do not affect the error output operation.

Power Sequencing

The CVDD and RVDD (including PWMVDD) power supplies should be brought up together to avoid high current transients that could fold back a power supply regulator. The PLLVDD may be brought up separately. The best practice is for all supplies to feed from regulators using a common power source. Typically this can be achieved by using a single 5V power source and regulating the 3.3V and 1.8V supplies from that 5V source. As noted in Note 7, all voltages of the same names must be tied together at the board level.

Clock and PLL

The clock is generated on-chip using a fundamental-mode crystal connected across the XTALI and XTALO pins. XTALO is an output, but it is designed only to drive the crystal and does not connect to any other circuit. XTALI is an input that connects to the other side of the crystal.

The clock generation contains a low jitter PLL critical for low noise PWM output and a precise master clock source for sample rate conversion and the audio processing data paths. The clock system is used throughout the device, and provides clock generators for brown-out detection, system and power-on reset, DSP, S/PDIF transmitter, and the PWM engine.

Clock and PLL hardware functions are controlled by internal device firmware. They are not programmable and are optimized for device and system operation.

Reset and Device Initialization

The D2-4 family devices must be reset to initialize and begin proper operation. A system reset is initiated by applying a low level to the nRESET input pin. External hardware circuitry or a controller within the amplifier system design must provide this reset signal and connect to the nRESET input to initiate the reset process. Device initialization then begins after the nRESET pin is released from its low-active state.

The chip contains power rail sensors and brownout detectors on the 3.3V and 1.8V power supplies. A loss or droop of power from either of these supplies triggers their brownout detectors, which asserts the nRSTOUT pin, driving it low. Connect the nRSTOUT pin to the nRESET input through hardware on the amplifier design to ensure a proper reset occurs if the power supply voltages drop below their design specifications.

At the deassertion of nRESET, the chip reads the status of the boot mode selection pins (IRQA and IRQB) and begins the boot process, determined by the boot mode that is defined by these pins' logic state. These device pins are strapped either high or low on the system's design (PCB). Boot mode operation is defined by the state of these pins that is latched into. See the "Boot Modes" on page 15 section for related descriptions.

Boot Modes

The D2-4 family devices contain internal firmware to operate the part and run the amplifier system. Parameter information used by the programmable settings can be written to the device after it is operational and running. Parameter data can also be read at boot time, which allows saved parameter settings to be used in processing. The device is designed to boot in one of four possible modes, allowing control and data to be provided from these boot sources:

- I^{2}C slave (to external microcontroller)
- I^{2}C EEPROM
- Internal device ROM only
- SPI slave

The specific boot mode is selected based on the state of the IRQB and IRQA input pins at the time of reset de-assertion. Boot modes are shown in Table 1.

TABLE 1. BOOT MODE SETTINGS

BOOT MODE	IRQB PIN	IRQA PIN	MASTER /SLAVE	DESCRIPTION
0	0	0	I^{2}C Slave	Operates as I^{2}C slave, boot at address 0x88. An external 2-wire I^{2}C master provides the boot code.
1	0	1	I^{2}C Master	Operates as 2-wire master; loads boot code from ROM on I^{2}C port.
2	1	0	-	Internal ROM Boot/Operation
3	1	1	SPI Slave	SPI slave. External SPI master provides boot code.

The device initializes as defined by its boot mode; however, it gets its configuration and parameter data from the host device. This host device can be either an external controller or from an EEPROM. If a system uses both an external controller and an EEPROM, the EEPROM loads first. During this time, the controller must remain off the I^{2}C bus.

Output Mode Configurations

The D2-4 family devices support four amplifier output configuration modes of powered output and line output combinations. These four modes are shown in Table 2.

TABLE 2. D2-41x51-QR OUTPUT CONFIGURATION MODES

CONFIG MODE	NAME	FUNCTION
0	2.0 L/R 4-Quadrant	• Powered Left and Right Outputs with 4-Quadrant, Full Bridge Drivers. • No Line-Level Outputs
1	2.0 L/R + L/R/Sub Line	• Powered Left and Right Outputs with 2-Quadrant, Full Bridge Drivers. • Single-Ended Stereo Left + Right Line-Level Outputs. • Dual-Ended Subwoofer Line-Level Output
2	2.1 L/R/Sub + L/R Line	• Powered Left and Right Outputs with 2-Quadrant Half Bridge Drivers. • Powered Subwoofer Output With 2-Quadrant, Full Bridge Driver. • Single-Ended Stereo Left + Right Line-Level Outputs. • Crossover Filtering Added to Signal Flow.
3	2.2 Bi-Amp	• Powered Left and Right Bi-Amp Outputs with 2-Quadrant Drivers. • Crossover Filtering Added to Signal Flow.

These configuration modes use different combinations of the five PWM output channels, and each mode maps the eight PWM pins to their appropriate PWM channel path. This channel content and mapping of the pins is shown in Table 3 on page 16. Of the total eight PWM pins, not all pins are used with every configuration mode. Timing and drive characteristics of each PWM pin output are automatically programmed for correct operation when those pins are connected to their designated output stages.

In Modes 2 and 3, the filtering for high and low pass crossovers is applied to the audio signal flow path, enabling the appropriate high or low pass content to be properly filtered for the PWM output channels.

The protect pin inputs are mapped to the PWM channels that are used for the powered outputs. This protect pin mapping assignment is shown in Table 3 for the different configurations.

Configuration Mode Assignment

The configuration mode is assigned when the D2-4 family device exits its reset state. At that time, the logic status of the PSSYNC/CFG1 and nERROR/CFG0 pins are latched into internal device registers. During this initialization time, these pins operate as logic inputs. After completion of the initialization and the internal firmware begins executing, these pins are reassigned as outputs for their shared functions. The internal latched logic state that defines the configuration mode remains until the device is powered down or reset again. Each mode requires a specific amplifier design hardware connection, and the configuration pin logic levels are defined through pull-up or pull-down resistors installed on that design's board. These modes are not programmable and are not intended to be changed for each hardware design.

TABLE 3. PWM CHANNEL ASSIGNMENT AND CONFIGURATION DETAILS

CONFIG MODE	CONFIG NAME	PSSYNC /CFG1 PIN LOGIC LEVEL	nERROR /CFG0 PIN LOGIC LEVEL	PWM CHANNEL NUMBER	PWM CHANNEL CONTENT	PWM PINS	PROTECT PIN ASSIGNMENT	SUPPORTED OUTPUT TOPOLOGY	AUDIO FUNCTION
0	2.0 L/R 4-Quadrant	0	0	0	L-Spkr	0-3	0	4-Quadrant, Full Bridge	Powered Left
				1	R-Spkr	4-7	1	4-Quadrant, Full Bridge	Powered Right
				2	-	-	-	-	-
				3	-	-	-	-	-
				4	-	-	-	-	-
1	2.0 L/R + L/R/Sub Line	0	1	0	L-Spkr	0, 1	0	2-Quadrant, Full Bridge	Powered Left
				1	R-Spkr	2, 3	1	2-Quadrant, Full Bridge	Powered Right
				2	L-Line	6	-	Line Level	Line/Headphone Left
				3	R-Line	7	-	Line Level	Line/Headphone Right
				4	Sub	4, 5	-	Line Level	Line Level Sub
2	2.1 L/R/Sub + L/R Line	1	0	0	L Spkr	0, 1	0	Half Bridge	Powered Left
				1	R Spkr	2, 3	1	Half Bridge	Powered Right
				2	L Line	6	-	Line Level	Line/Headphone Left
				3	R Line	7	-	Line Level	Line/Headphone Right
				4	Sub	4, 5	2	2-Quadrant, Full Bridge	Powered Sub
3	2.2 Bi-Amp	1	1	0	L Hi-Freq	0, 1	0,1	Half Bridge	Powered Left HF
				1	L Lo-Freq	2, 3	1,0	Half Bridge	Powered Left LF
				2	R Hi-Freq	4, 5	2	Half Bridge	Powered Right HF
				3	R Lo-Freq	6, 7	2	Half Bridge	Powered Right LF
				4	-	-	-	-	-

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Mar 19, 2019	FN6783.2	Changed the base parts on page 1 in header to D2-4 Family Audio SOC. Updated Related Literature section. Replaced all words named "D2AudioTM" to "D2 Audio DSP"; "DAE-4" to "D2-4 family"; "Digital Audio Engine" to "Digital Audio Processor"; "SoundSuite" to "Sound Enhancement Algorithm"; "DSP Canvas II" to "D2 Audio Customization GUI". Updated Audio Enhancement Feature Processing bullet points on page page 10. Updated links throughout document. Updated Figures 1, 2, 3, 4, 5, and 6. Removed About Intersil section. Updated Trademarks section. Updated disclaimer.
May 5, 2016	FN6783.1	Updated entire datasheet applying Intersil's new standards. Updated the Ordering Information table on page 3. Updated Note 8 on page 6. Added the Disclaimer for DTS® (SRS) Technology License Required Notice. Added Revision History section. Replaced Products verbiage to About Intersil verbiage. Updated POD to the latest revision changes are as follows: -Corrected Note 4 from: "Dimension b applies to..." to: "Dimension applies to..." 'b' leftover from when dimensions were in table format. -Enclosed Notes #'s 4, 5 and 6 in a triangle.

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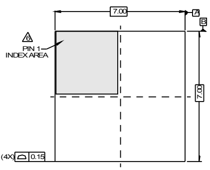
Package Outline Drawing

For the most recent package outline drawing, see L48.7x7.

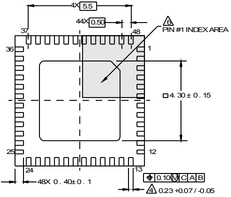
L48.7x7

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 5, 4/10



TOP VIEW



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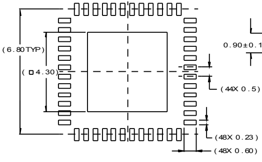
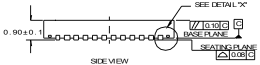
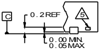


TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

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