PROGRAMMABLE FLEXPC™ CLOCK FOR P4 PROCESSOR

IDTCV115F

FEATURES:

- **One high precision N and SSC programmable PLL for SRC/PCI**
- **One high precision N and SSC programmable PLL for CPU**
- **One high precision SSC programmable PLL for SATA**
- **One high precision PLL for 96MHz/48MHz**
- **Band-gap circuit for differential outputs**
- **Support multiple spread spectrum modulation, down and center**
- **Support SMBus block read/write, index read/write**
- **Selectable output strength for REF, PCI, and USB48MHz**
- **Available in SSOP package**

KEY SPECIFICATIONS:

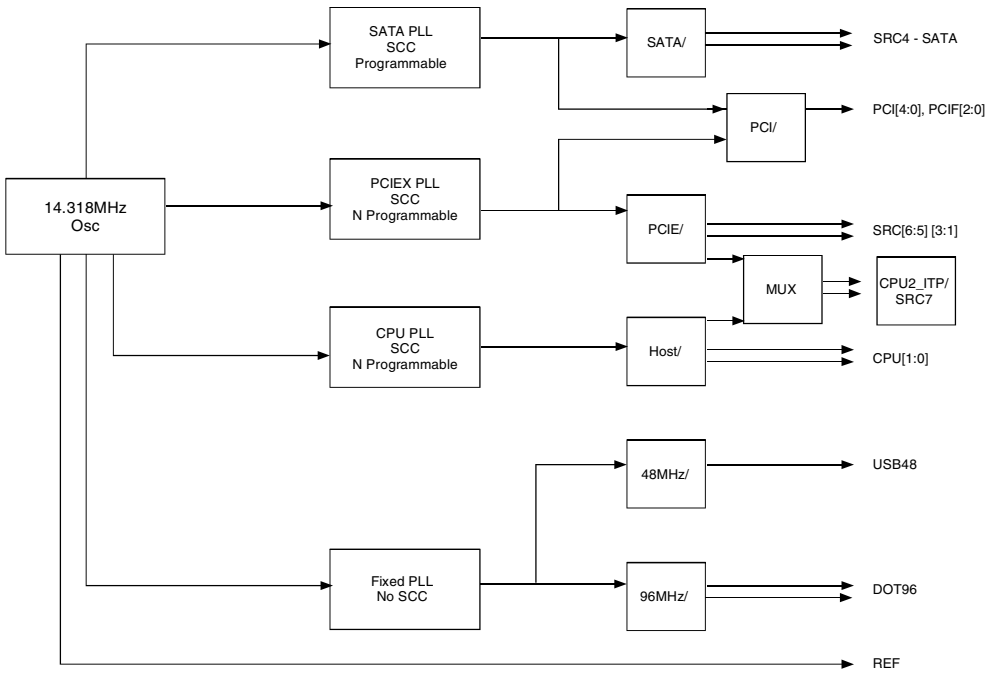
- **CPU/SRC CLK cycle to cycle jitter < 85ps**
- **SATA CLK cycle to cycle jitter < 85ps**

DESCRIPTION:

IDTCV115F is a 56 pin clock device, complying the latest Intel CK410E requirements, for Intel advance P4 processors. The CPU output buffer is designed to support up to 400MHz processor. One dedicated PLL for Serial ATA clock provides high accuracy frequency. This device also implements Band-gap referenced I_{REF} to reduce the impact of V_{DD} variation on differential outputs, which can provide more robust system performance.

Each CPU/SRC/PCI, SATA clock has its own Spread Spectrum selection, which allows for isolated changes instead of affecting other clock groups.

FUNCTIONAL BLOCK DIAGRAM



OUTPUT TABLE

CPU	CPU2_ITP/SRC	SRC	SATA	PCI/PCIF	REF	DOT96	48MHz
2	1	5	1	8	1	1	1

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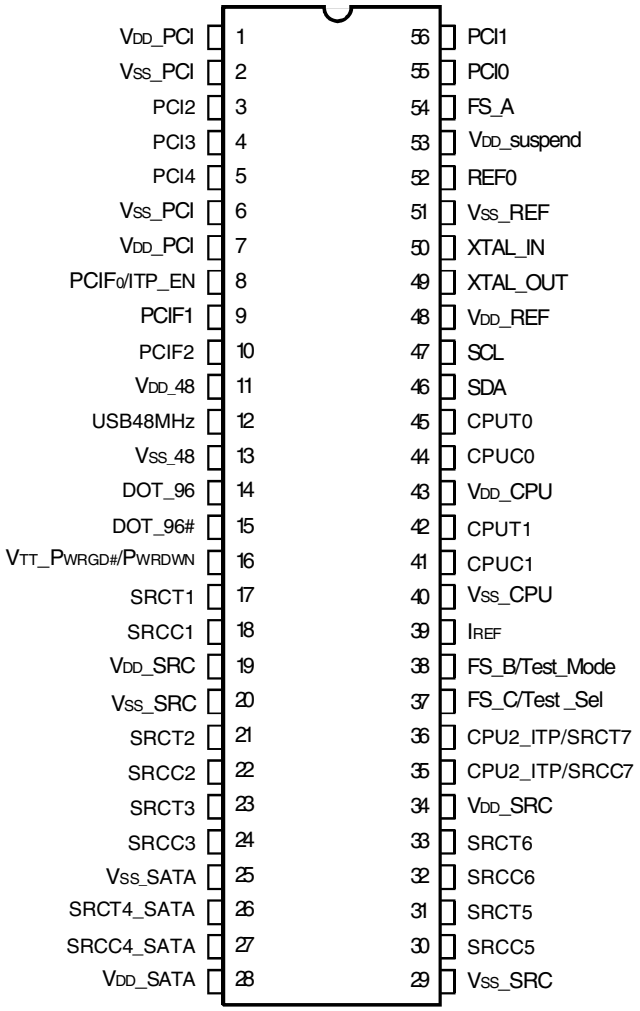
PIN CONFIGURATION



SSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Min	Max	Unit
V_{DDA}	3.3V Core Supply Voltage		4.6	V
V_{DD}	3.3V Logic Input Supply Voltage	GND - 0.5	4.6	V
T_{STG}	Storage Temperature	–65	+150	° C
$T_{AMBIENT}$	Ambient Operating Temperature	0	+70	° C
T_{CASE}	Case Temperature		+115	° C
ESD Prot	Input ESD Protection Human Body Model	2000		V

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TEST MODE SELECT(1)

If TEST_SEL sampled above 2V at $V_{TT}\_P_{WRGD}$ active LOW

Pin38 (test_mode)	CPU	SRC	PCI/F	REF	DOT96	USB
1	REF/N	REF/N	REF/N	REF	REF/N	REF/N
0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

NOTE:
1. Once test clock operation has been invoked, TEST_MODE pin will select between the Hi-Z and REF/N.

ITP_EN

ITP_EN	pin 38	pin 39
1	CPUC2_ITP	CPUT_ITP
0	SRCC7	SRCT7

HW FREQUENCY SELECTION TABLE

FSC, B, A	CPU	SRC4_SATA	SRC[3:1], SCR[7:5]	PCI	USB	DOT	REF
101	100	100	100	33.3	48	96	14.318
001	133	100	100	33.3	48	96	14.318
011	166	100	100	33.3	48	96	14.318
010	200	100	100	33.3	48	96	14.318
000	266	100	100	33.3	48	96	14.318
100	333	100	100	33.3	48	96	14.318
110	400	100	100	33.3	48	96	14.318
111	Reserve	100	100	33.3	48	96	14.318

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PIN DESCRIPTION

Pin Number	Name	Type	Description
1	V_{DD}_PCI	PWR	3.3V
2	V_{SS}_PCI	GND	GND
3	PCI2	OUT	PCI clock
4	PCI3	OUT	PCI clock
5	PCI4	OUT	PCI clock
6	V_{SS}_PCI	GND	GND
7	V_{DD}_PCI	PWR	3.3V
8	PCIF0/ITP_EN	I/O	PCI clock, free running. CPU_2 select (sampled at V_{TT}_P_{WRGD}# assertion), HIGH = CPU_2.
9	PCIF1	OUT	PCI clock, free running
10	PCIF2	OUT	PCI clock, free running
11	V_{DD}_48	PWR	3.3V
12	USB48	OUT	48MHz clock
13	V_{SS}_48	GND	GND
14	DOT_96T	OUT	96MHz 0.7V current mode differential clock output
15	DOT_96C	OUT	96MHz 0.7V current mode differential clock output
16	V_{TT}_P_{WRGD}#/P_{WRDWN}	IN	3.3V LVTTL input is a level-sensitive strobe used to latch the FS_A, FS_B, FS_C/TEST_SEL and PCIF_0/ITP_EN inputs. After V_{TT}_P_{WRGD}# assertion, becomes a real-time input for asserting power down (active high). Internal pull LOW.
17	SRCT1	OUT	Differential Serial reference clock
18	SRCC1	OUT	Differential Serial reference clock
19	V_{DD}_SRC	PWR	3.3V
20	V_{SS}	GND	GND
21	SRCT2	OUT	Differential Serial reference clock
22	SRCC2	OUT	Differential Serial reference clock
23	SRCT3	OUT	Differential Serial reference clock
24	SRCC3	OUT	Differential Serial reference clock
25	V_{SS}	GND	GND
26	SRCT4_SATA	OUT	SATA clock
27	SRCC4_SATA	OUT	SATA clock
28	V_{DD}_SRC	PWR	3.3V
29	V_{SS}_SRC	GND	GND
30	SRCC5	OUT	Differential Serial reference clock
31	SRCT5	OUT	Differential Serial reference clock
32	SRCC6	OUT	Differential Serial reference clock
33	SRCT6	OUT	Differential Serial reference clock
34	V_{DD}_SRC	PWR	3.3V
35	CPUC2_ITP/ SRCC7	OUT	Selectable CPU or SRC differential clock output. ITP_EN=0 @ V_{TT}_P_{WRGD}# assertion = SRC_7
36	CPUT2_ITP/ SRCT7	OUT	Selectable CPU or SRC differential clock output. ITP_EN=0 @ V_{TT}_P_{WRGD}# assertion = SRC_7
37	FS_C/Test_Sel	IN	CPU frequency selection. Selects test mode if pulled above 2V when V_{TT}_P_{WRGD}# is asserted.
38	FS_B/Test_Mode	IN	CPU frequency selection. In test mode, 1=Hi-Z, 0=REF/N.
39	IREF	OUT	Reference current for differential output buffer
40	V_{SS}	GND	GND
41	CPUC1	OUT	Host 0.7V current mode differential clock output
42	CPUT1	OUT	Host 0.7V current mode differential clock output
43	V_{DD}_CPU	PWR	3.3V
44	CPUC0	OUT	Host 0.7V current mode differential clock output
45	CPUT0	OUT	Host 0.7V current mode differential clock output
46	SDA	I/O	SMBus data

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PIN DESCRIPTION (CONT.)

Pin Number	Name	Type	Description
47	SCL	IN	SMBus CLK
48	V_{DD}_REF	PWR	3.3V
49	XTAL_OUT	OUT	Xtal output
50	XTAL_IN	IN	Xtal input
51	V_{SS}_REF	GND	GND
52	REF0	OUT	14.318 MHz reference clock output
53	V_{DD}_Suspend	PWR	In the power down mode, supply 3.3V to SM control registers, <1mA. In the normal operation, regular V_{DD}.
54	FS_A	IN	CPU frequency selection
55	PCI0	OUT	PCI clock
56	PCI1	OUT	PCI clock

SM PROTOCOL

INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20-27	8	Master	Byte count, N (0 is not valid)
28	1	Slave	Ack (Acknowledge)
29-36	8	Master	first data byte (Offset data byte)
37	1	Slave	Ack (Acknowledge)
38-45	8	Master	2nd data byte
46	1	Slave	Ack (Acknowledge)
			:
		Master	Nth data byte
		Slave	Acknowledge
		Master	Stop

INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit30-37).

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20	1	Master	Repeated Start
21-28	8	Master	D3h
29	1	Slave	Ack (Acknowledge)
30-37	8	Slave	Byte count, N (block read back of N bytes), Byte 8
38	1	Master	Ack (Acknowledge)
39-46	8	Slave	first data byte (Offset data byte)
47	1	Master	Ack (Acknowledge)
48-55	8	Slave	2nd data byte
			Ack (Acknowledge)
			:
		Master	Ack (Acknowledge)
		Slave	Nth data byte
			Not acknowledge
		Master	Stop

INDEX BYTE WRITE

Setting bit[11:18] = starting address, bit[20:27] = 01h.

INDEX BYTE READ

Setting bit[11:18] = starting address. After reading back the first data byte, master issues Stop bit.

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S.E. CLOCK STRENGTH SELECTION (PCI, REF, USB48)

Str[1:0]	
00	1
01	0.8
10	0.6
11	1.2

PCI

When Byte5 bit6 = 0; otherwise, PCI = SRC frequency/3

PCIS[1:0]	PCI
00	33.33
01	36.36
10	40
11	n/a

S_CNS, S_PNS, H_CNS,H_PNS N SELECTION

NS[1:0]	
00	Standard of Each CPU Mode (Band)
01	N Selection 1
10	N Selection 2
11	Don't care

SSC MAGNITUDE CONTROL, SMC

SMC[2:0]	%
000	OFF
001	- 0.3
010	- 0.5
011	±0.125
100	±0.25
101	±0.375
110	±0.5
111	±0.4

RESOLUTION

	N Resolution (MHz)	%
CPU = 100MHz mode	0.666667	0.67%
CPU = 133MHz mode	0.888889	0.67%
CPU = 166MHz mode	1.333333	0.8%
CPU = 200MHz mode	1.333333	0.67%
CPU = 266MHz mode	2.666667	1.00%
CPU = 333MHz mode	2.666667	0.8%
CPU = 400MHz mode	2.666667	0.67%
SRC (PCI Express)	0.666667	0.67%

RESOLUTION FINE TUNE

IB_[1:0]	00 and 11	01 (resolution * 1/3)	10 (resolution * 2/3)
CPU = 100MHz mode	No increase	0.2222 MHz	0.4444MHz
CPU = 133MHz mode	No increase	0.2963MHz	0.5926MHz
CPU = 166MHz mode	No increase	0.4444MHz	0.8888MHz
CPU = 200MHz mode	No increase	0.4444MHz	0.8888MHz
CPU = 266MHz mode	No increase	0.888888MHz	1.77777MHz
CPU = 333MHz mode	No increase	0.888888MHz	1.77777MHz
CPU = 400MHz mode	No increase	0.888888MHz	1.77777MHz

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BYTE 0

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	CPUT2, CPUC2/ SRCT7, SRCC7	Output Enable	Tristate	Enable	RW	1
6	SRCT6, SRCC6	Output Enable	Tristate	Enable	RW	1
5	SRCT5, SRCC5	Output Enable	Tristate	Enable	RW	1
4	SRCT4, SRCC4 (SATA)	Output Enable	Tristate	Enable	RW	1
3	SRCT3, SRCC3	Output Enable	Tristate	Enable	RW	1
2	SRCT2, SRCC2	Output Enable	Tristate	Enable	RW	1
1	SRCT1, SRCC1	Output Enable	Tristate	Enable	RW	1
0	REF0 2x drive	2x drive Enable	1x	2x	RW	1

BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	DOT96T, DOT96C	Output Enable	Tristate	Enable	RW	1
6	Reserved				RW	1
5	USB48	Output Enable	Tristate	Enable	RW	1
4	Reserved				RW	0
3	REF0	Output Enable	Tristate	Enable	RW	1
2	CPUT1, CPUC1	Output Enable	Tristate	Enable	RW	1
1	CPUT0, CPUC0	Output Enable	Tristate	Enable	RW	1
0	Reserved				RW	0

BYTE 2

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	PCI4	Output Enable	Tristate	Enable	RW	1
6	PCI3	Output Enable	Tristate	Enable	RW	1
5	PCI2	Output Enable	Tristate	Enable	RW	1
4	PCI1	Output Enable	Tristate	Enable	RW	1
3	PCI0	Output Enable	Tristate	Enable	RW	1
2	PCIF2	Output Enable	Tristate	Enable	RW	1
1	PCIF1	Output Enable	Tristate	Enable	RW	1
0	PCIF0	Output Enable	Tristate	Enable	RW	1

BYTE 3

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7		FSC latched value on power up			R	see note 1
6		FSB latched value on power up			R	
5		FSA latched value on power up			R	
4	SRCT[7:1]	SRCT P_{WRDWN} drive mode	Driven in power down	Tristate in power down	RW	0
3	CPUT2	CPUT2 P_{WRDWN} drive mode	Driven in power down	Tristate in power down	RW	0
2	CPUT1	CPUT1 P_{WRDWN} drive mode	Driven in power down	Tristate in power down	RW	0
1	CPUT0	CPUT0 P_{WRDWN} drive mode	Driven in power down	Tristate in power down	RW	0
0	DOT96T	DOT96 P_{WRDWN} drive mode	Driven in power down	Tristate	RW	0

NOTE:
1. The default value depends on the value of frequency select bits FSA, FSB, and FSC at power-on.

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BYTE 4

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	PCIFStr1	PCIF strength selection				0
6	PCIFStr0	see SE Clock Strength table				0
5	PCIStr1	PCI strength selection				0
4	PCIStr0	see SE Clock Strength table				1
3	REFStr1	REF strength selection				0
2	REFStr0	see SE Clock Strength table				0
1	48MHStr1	USB48MHz strength selection				1
0	48MHzStr0	see SE Clock Strength table				1

BYTE 5

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7						0
6	PCIPLLS	PCI PLL select	SATA PLL	PCI EX PLL	RW	0
5	PCIS1	See PCIS table, only valid when			RW	0
4	PCIS0	Byte5 bit 6 = 0 See PCIS Table			RW	0
3	SM control registers contents Power Down mode	During the Power Down	Reset SM to default	SM contents have no change	RW	1
2	SATA_SMC2	SATA PLL spread spectrum			RW	0
1	SATA_SMC1	magnitude control select			RW	1
0	SATA_SMC0	see SMC table			RW	0

BYTE 6

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	WDHRB	Hard Alarm read back, reset by WD disable			R	0
6	WDSRB	Soft Alarm read back, rest by WD disable			R	0
5	SRC_SMC2	SRC(PCIEXpress) PLL spread spectrum magnitude			RW	0
4	SRC_SMC1	control select see SMC table			RW	1
3	SRC_SMC0				RW	0
2	CPU_SMC2	CPU PLL spread spectrum			RW	1
1	CPU_SMC1	control magnitude select			RW	0
0	CPU_SMC0	see SMC table			RW	0

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BYTE 7

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7		Revision ID				0
6		Revision ID				0
5		Revision ID				0
4		Revision ID				0
3		Vendor ID				0
2		Vendor ID				1
1		Vendor ID				0
0		Vendor ID				1

BYTE 8

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7					RW	0
6					RW	0
5					RW	0
4					RW	1
3					RW	1
2					RW	1
1					RW	1
0					RW	1

BYTES 9 - 15 ARE DUMMY BITES

BYTE 16

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Reserved				RW	0
6	Reserved				RW	0
5	IB2_1	For CN2			RW	0
4	IB2_0				RW	0
3	Reserved				RW	0
2	Reserved				RW	0
1	IB1_1	For CN1			RW	0
0	IB1_0				RW	0

BYTE 17

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Reserved				RW	0
6	Reserved				RW	0
5	Reserved				RW	0
4	Reserved				RW	0
3	Reserved				RW	0
2	Reserved				RW	0
1	Reserved				RW	0
0	CN1_8				RW	0

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BYTE 18

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	CN1_7	CPU PLL N selection 1			RW	1
6	CN1_6				RW	0
5	CN1_5				RW	0
4	CN1_4				RW	1
3	CN1_3				RW	0
2	CN1_2				RW	1
1	CN1_1				RW	1
0	CN1_0				RW	0

BYTE 19

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	CN2_8, MSB	CPU N selection 2				0
6	CN2_7					1
5	CN2_6					0
4	CN2_5					0
3	CN2_4					1
2	CN2_3					0
1	CN2_2					1
0	CN2_1					1

BYTE 20

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	CN2_0	CPU N selection 2				0
6						0
5						0
4						0
3						0
2						0
1	Reserved				RW	0
0	PN1_7				RW	1

BYTE 21

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	PN1_6	SRC PLL (PCI Express) N Selection 1			RW	0
6	PN1_5				RW	0
5	PN1_4				RW	1
4	PN1_3				RW	0
3	PN1_2				RW	1
2	PN1_1				RW	1
1	PN1_0				RW	0
0	Reserved				RW	0

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BYTE 22

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	PN2_7	SRC PLL (PCI Express) N Selection 2			RW	1
6	PN2_6				RW	0
5	PN2_5				RW	0
4	PN2_4				RW	1
3	PN2_3				RW	0
2	PN2_2				RW	1
1	PN2_1				RW	1
0	PN2_0				RW	0

BYTE 23

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Reserved				RW	0
6	Reserved				RW	0
5	S_CNS1	Soft Alarm CPU PLL N select, see S_CNS N Selection Table			RW	0
4	S_CNS0				RW	0
3	S_PNS1	Soft Alarm SRC PLL (PCI Express) N select, see S_PNS N Selection Table			RW	0
2	S_PNS0				RW	0
1						0
0						0

BYTE 24

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Reserved				RW	0
6	Reserved				RW	0
5	H_CNS2	Hard Alarm CPU PLL N select, see H_CNS N Selection Table			RW	0
4	H_CNS0				RW	0
3	H_PNS1	Hard Alarm SRC PLL (PCI Express) N select, see H_PNS N selection table			RW	0
2	H_PNS0				RW	0
1						0
0						0

BYTE 25

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	WD Timer 7	Watchdog timer Default is 11*290ms Hard Alarm = WD timer * 290ms			RW	0
6	WD Timer 6				RW	0
5	WD Timer 5				RW	0
4	WD Timer 4				RW	0
3	WD Timer 3				RW	1
2	WD Timer 2				RW	0
1	WD Timer 1				RW	1
0	WD Timer 0				RW	1

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BYTE 26

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7					RW	0
6					RW	0
5					RW	0
4					RW	0
3	Soft Timer 3	Soft Alarm timer Soft Alarm = Soft timer * 290ms			RW	0
2	Soft Timer 2				RW	0
1	Soft Timer 1				RW	0
0	Soft Timer 0				RW	1

BYTE 27

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Watch Dog Enable	Watch Dog Enable	Disable	Enable	RW	0
6						0
5	Soft Alarm Enable	Soft Alarm Enable	Disable	Enable	RW	0
4					RW	0
3	Hard Alarm Enable	Hard Alarm Enable	Disable	Enable	RW	0
2					RW	0
1	Reserved				RW	0
0	Reserved				RW	0

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PLL FREQUENCY PROGRAMMING PROCEDURES

The user changes PLL frequency through Soft Alarm or Hard Alarm. The Watch Dog circuit has to be enabled. Based on their application, the user may enable either one or both of the alarms.

User presets the CPU PLL N and SRC PLL N value:

1. Set CPU PLL N, CN1 and CN2, byte 18 and byte 19
2. Set SRC(PCI Express) PLL N, PN1 and PN2, byte 21, 22

User selects the frequency for Soft Alarm and Hard Alarm, if enabled respectively:

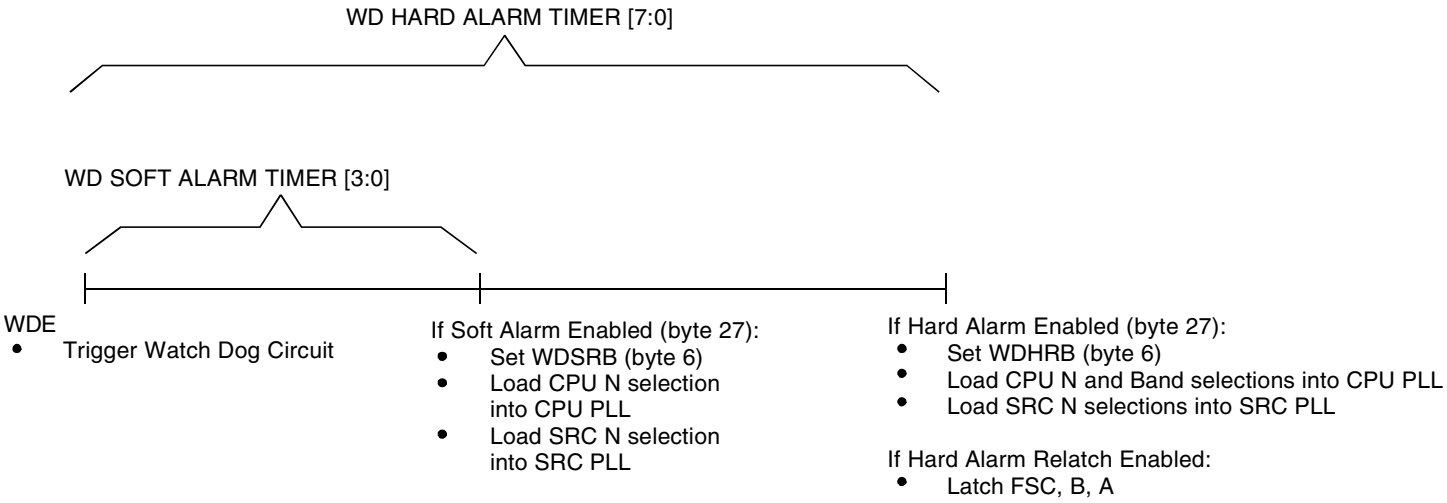
4. Select Soft Alarm frequency, byte 23
5. Select Hard Alarm frequency, byte 24

User sets the Timer and enables the WD circuit for frequency switch:

6. Set Hard Alarm Timer, byte 25
7. Set Soft Alarm Timer, byte 26
8. Enable Soft and Hard Alarm, byte 27
9. Enable Watch Dog (WDE), byte 27

- WDE Disable resets WDSRB and WDHRB.
- PCI CLK is selectable from SRC PLL or SATA PLL, byte 5 bit 6. If from SRC PLL, PCI frequency = 1/3 of SRC frequency. If from SATA, PCI is fixed to 3 selections, 33MHz, 36MHz and 40MHz, byte 5 bit[5:4].

WD SOFT AND HARD ALARM/TIME OUT OPERATION



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ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.3V ± 5%	2	—	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	3.3V ± 5%	V_{SS} - 0.3	—	0.8	V
V_{IH_FS}	FS Input HIGH Voltage	For FSA,B,C and Test_Mode	0.7	—	V_{DD} + 0.3	V
V_{IL_FS}	FS Input LOW Voltage	For FSA,B,C and Test_Mode	V_{SS} - 0.3	—	0.35	V
I_{IL}	Input LeakageCurrent	0< V_{IN} < V_{DD}, no internal pull-up or pull-down	–5	—	+5	µA
$I_{DD3.3OP}$	Operating Supply Current	Full active, C_L = full load	—	—	400	mA
$I_{DD3.3PD}$	Powerdown Current	All differential pairs driven	—	—	70	mA
		All differential pairs tri-stated	—	—	12	
F_I	Input Frequency(1)	V_{DD} = 3.3V	—	14.31818	—	MHz
L_{PIN}	Pin Inductance(2)		—	—	7	nH
C_{IN}	Input Capacitance(2)	Logic inputs	—	—	5	pF
C_{OUT}		Output pin capacitance	—	—	6	
C_{INX}		XTAL_IN and XTAL_OUT pins	—	—	5	
T_{STAB}	Clock Stabilization(2,3)	From V_{DD} power-up or de-assertion of PD# to first clock	—	—	1.8	ms
	Modulation Frequency(2)	Triangular modulation	30	—	33	KHz
	T_{DRIVE_SRC}(2)	SRC output enable after PCI_Stop# de-assertion	—	—	15	ns
	$T_{DRIVE\_PD\#}$(2)	CPU output enable after PD# de-assertion	—	—	300	us
	$T_{FALL\_PD\#}$(2)	Fall time of PD#	—	—	5	ns
	$T_{RISE\_PD\#}$(2)	Rise time of PD#	—	—	5	ns
	$T_{DRIVE\_CPU\_Stop\#}$(2)	CPU output enable after CPU_Stop# de-assertion	—	—	10	us
	$T_{FALL\_CPU\_Stop\#}$(2)	Fall time of PD#	—	—	5	ns
	$T_{RISE\_CPU\_Stop\#}$(2)	Rise time of PD#	—	—	5	ns

NOTES:
1. Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.
2. This parameter is guaranteed by design, but not 100% production tested.
3. See TIMING DIAGRAMS for timing requirements.

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ELECTRICAL CHARACTERISTICS - CPU, SRC, AND DOT96 0.7 CURRENT MODE DIFFERENTIAL PAIR(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Z_O	Current Source Output Impedance(2)	$V_O = V_X$	3000	—	—	Ω
V_{OH3}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL3}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.4	V
V_{HIGH}	Voltage HIGH(2)	Statistical measurement on single-ended signal using	660	—	1150	mV
V_{LOW}	Voltage LOW(2)	oscilloscope math function	–300	—	150	
V_{OVS}	Max Voltage(2)	Measurement on single-ended signal using absolute value	—	—	1150	mV
V_{UDS}	Min Voltage(2)		–300	—	—	
$V_{CROSS(ABS)}$	Crossing Voltage (abs)(2)		250	—	550	mV
d - V_{CROSS}	Crossing Voltage (var)(2)	Variation of crossing over all edges	—	—	140	mV
ppm	Static Error(2,3)	See T_{PERIOD} Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Average Period(3)	400MHz nominal / -0.5% spread	2.4993	—	2.5133	ns
		333.33MHz nominal / -0.5% spread	2.9991	—	3.016	
		266.66MHz nominal / -0.5% spread	3.7489	—	3.77	
		200MHz nominal / -0.5% spread	4.9985	—	5.0266	
		166.66MHz nominal / -0.5% spread	5.9982	—	6.032	
		133.33MHz nominal / -0.5% spread	7.4978	—	7.54	
		100MHz nominal / -0.5% spread	9.997	—	10.0533	
		96MHz nominal	10.4135	—	10.4198	
T_{ABSMIN}	Absolute Min Period(2,3)	400MHz nominal / -0.5% spread	2.4143	—	—	ns
		333.33MHz nominal / -0.5% spread	2.9141	—	—	
		266.66MHz nominal / -0.5% spread	3.6639	—	—	
		200MHz nominal / -0.5% spread	4.9135	—	—	
		166.66MHz nominal / -0.5% spread	5.9132	—	—	
		133.33MHz nominal / -0.5% spread	7.4128	—	—	
		100MHz nominal / -0.5% spread	9.912	—	—	
		96MHz nominal	10.1635	—	—	
t_R	Rise Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
t_F	Fall Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
d-t_R	Rise Time Variation(2)		—	—	125	ps
d-t_F	Fall Time Variation(2)		—	—	125	ps
d_{T3}	Duty Cycle(2)	Measurement from differential waveform	45	—	55	%

NOTES:
1. SRC clock outputs run only at 100MHz.
2. This parameter is guaranteed by design, but not 100% production tested.
3. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

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ELECTRICAL CHARACTERISTICS - CPU, SRC, AND DOT96 0.7 CURRENT MODE DIFFERENTIAL PAIR, CONTINUED(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{SK3}	Skew, CPU[1:0](2)	V_T = 50%	—	—	100	ps
	Skew, CPU2(2)		—	—	250	
	Skew, SRC(2)		—	—	250	
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle, CPU[1:0](2)	Measurement from differential waveform	—	—	85	ps
	Jitter, Cycle to Cycle, CPU2(2)		—	—	100	
	Jitter, Cycle to Cycle, SRC(2)		—	—	125	
	Jitter, Cycle to Cycle, DOT96(2)		—	—	250	

NOTES:
1. SRC clock outputs run only at 100MHz.
2. This parameter is guaranteed by design, but not 100% production tested.

ELECTRICAL CHARACTERISTICS - PCICLK / PCICLK_F

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 30pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Static Error(1,2)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period(2)	33.33MHz output nominal	29.991	—	30.009	ns
		33.33MHz output spread	29.991	—	30.1598	
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
t_{SK1}	Skew(1)	V_T = 1.5V	—	—	500	ps
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V	—	—	500	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

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ELECTRICAL CHARACTERISTICS, 48MHZ, USB

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Static Error(1,2)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period(2)	48MHz output nominal	20.8257	—	20.834	ns
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-29	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-23	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	29	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	27	
	Edge Rate(1)	Rising edge rate	1	—	2	V/ns
	Edge Rate(1)	Falling edge rate	1	—	2	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle		—	—	350	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - REF-14.318MHZ

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period	14.318MHz output nominal	69.827	—	69.855	ns
V_{OH}	Output HIGH Voltage(1)	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage(1)	I_{OL} = 1mA	—	—	0.4	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V	—	—	1000	ps

NOTE:
1. This parameter is guaranteed by design, but not 100% production tested.

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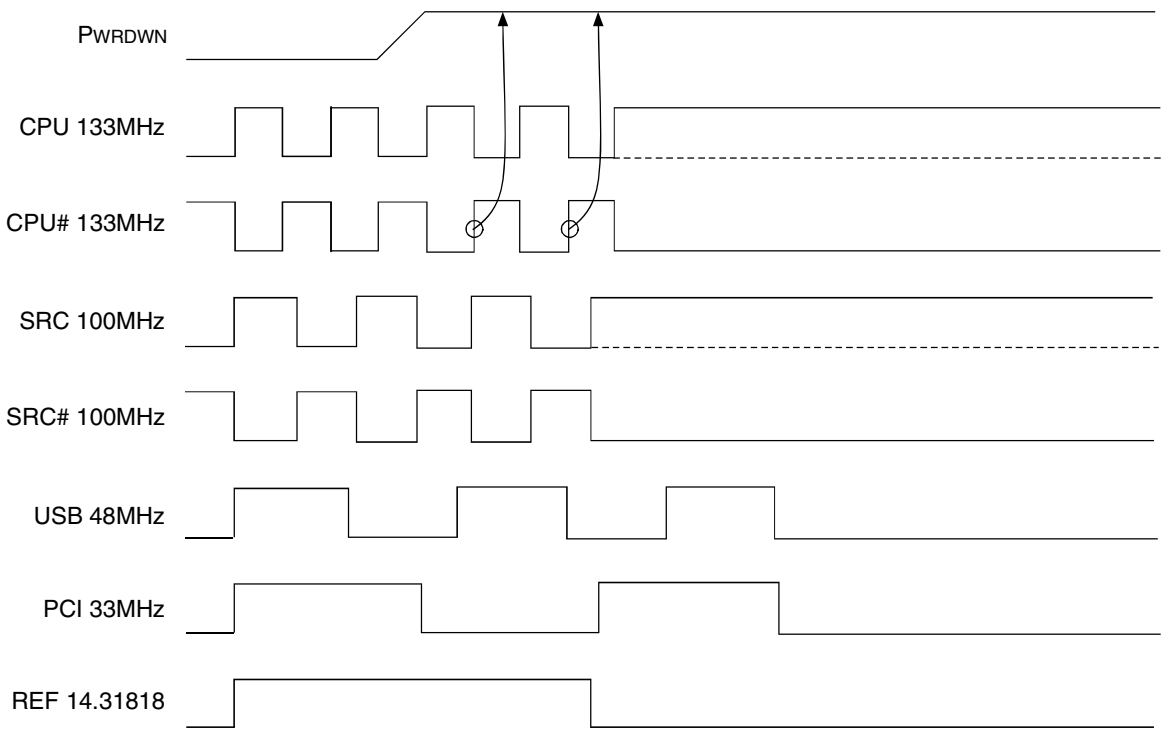
PD, POWER DOWN

PD is an asynchronous active high input used to shut off all clocks cleanly prior to clock power. When PD is asserted high all clocks will be driven low before turning off the VCO. In PD de-assertion all clocks will start without glitches.

PWRDWN	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
0	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
1	IREF * 2 or float	Float	IREF * 2 or float	Float	Low	Low	IREF * 2 or float	Float	Low

PD ASSERTION



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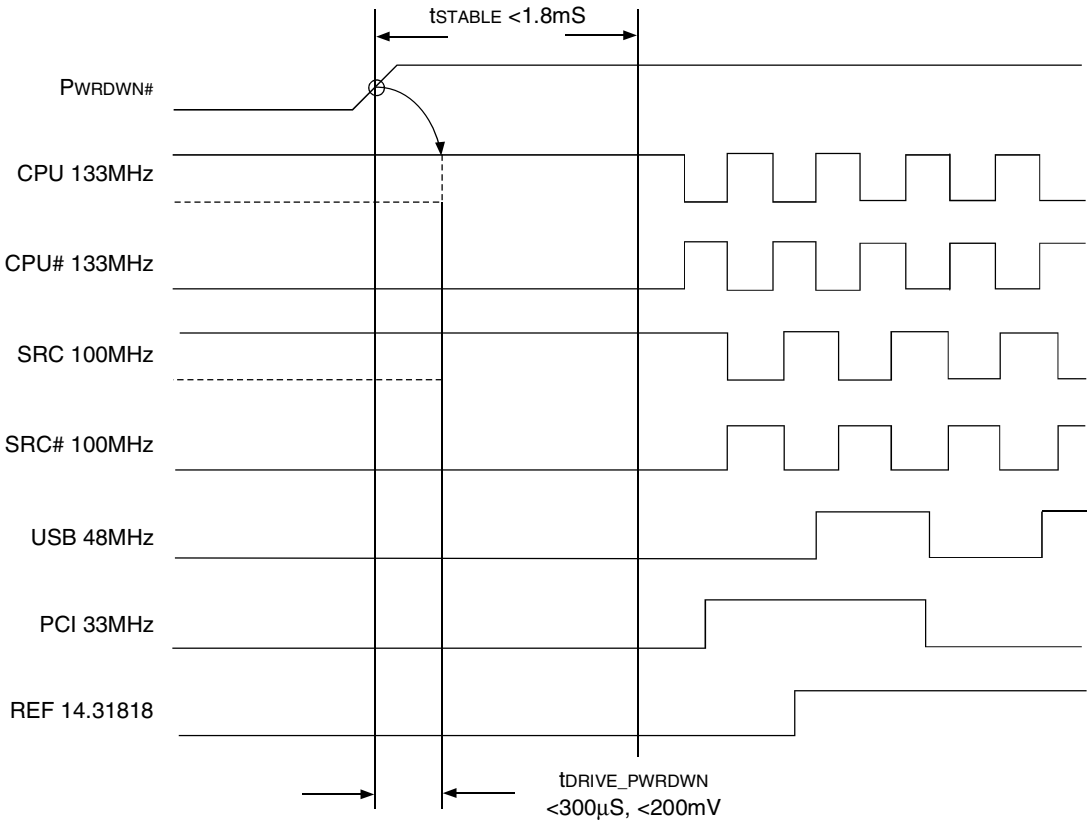
PD DE-ASSERTION



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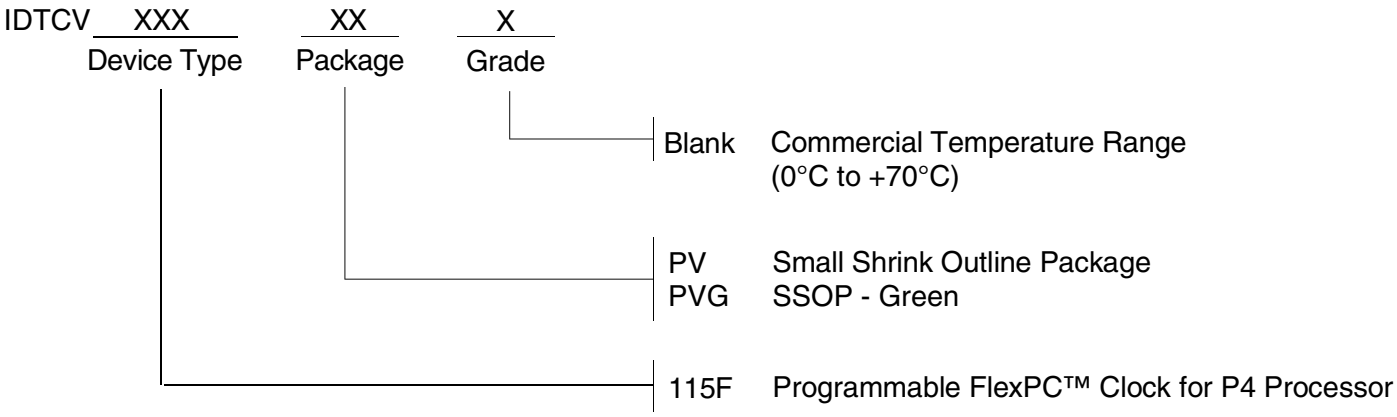

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