

FEATURES:

- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes one clock input to one bank of ten outputs
- Output enable bank control
- External feedback (FBIN) pin is used to synchronize the outputs to the clock input signal
- No external RC network required for PLL loop stability
- Operates at 3.3V VDD
- tpd Phase Error at 133MHz: $< \pm 150\text{ps}$
- Jitter (peak-to-peak) at 133MHz: $< \pm 75\text{ps}$ @ 133MHz
- Spread Spectrum Compatible
- Operating frequency 25MHz to 140MHz
- Available in 24-Pin TSSOP package

APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

DESCRIPTION:

The CSP2510C is a high performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CSP2510C operates at 3.3V.

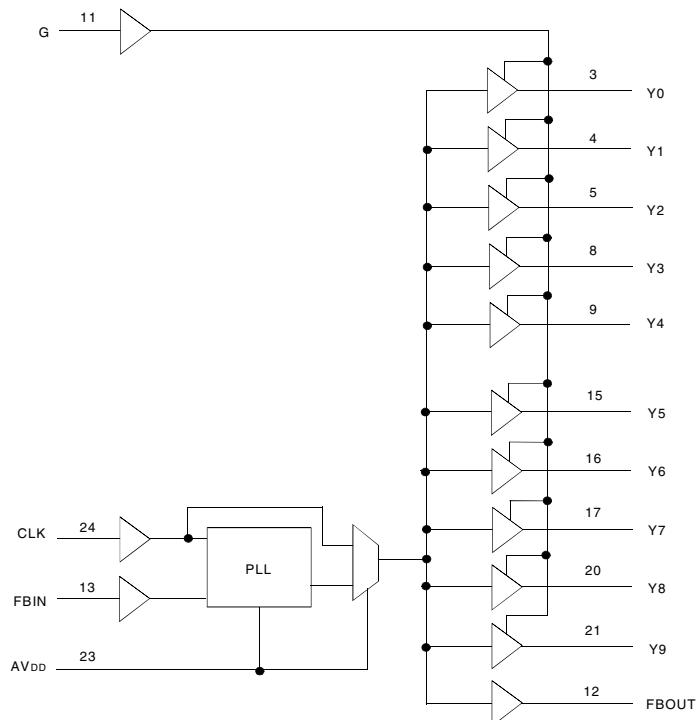
One bank of ten outputs provide low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. The outputs can be enabled or disabled via the control Ginput. When the Ginput is high, the outputs switch in phase and frequency with CLK; when the Ginput is low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CSP2510C does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

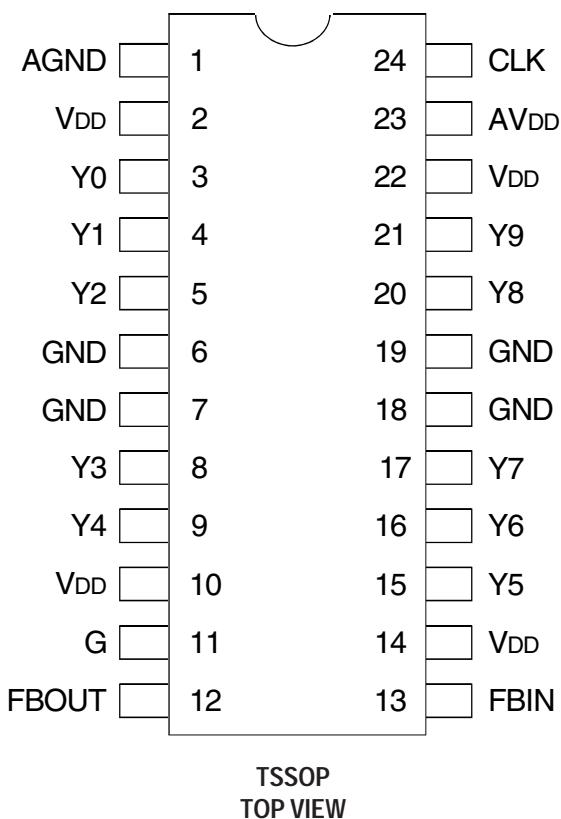
Because it is based on PLL circuitry, the CSP2510C requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for the test purposes by strapping AVDD to ground.

The CSP2510C is specified for operation from 0°C to +85°C. This device is also available (on special order) in Industrial temperature range (-40°C to +85°C). See ordering information for details.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Max	Unit
V _{DD}	Supply Voltage Range	-0.5 to +4.6	V
V _I ⁽¹⁾	Input Voltage Range	-0.5 to +6.5	V
V _O ^(1,2)	Voltage range applied to any output in the high or low state	-0.5 to V _{DD} + 0.5	V
I _{IK} (V _I < 0)	Input clamp current	-50	mA
I _{OK} (V _O < 0 or V _O > V _{DD})	Terminal Voltage with Respect to GND (inputs V _{IH} 2.5, V _{IL} 2.5)	±50	mA
I _O (V _O = 0 to V _{DD})	Continuous Output Current	±50	mA
V _{DD} or GND	Continuous Current	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _J	Junction Temperature	+150	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

CAPACITANCE

Parameter	Description	Min.	Typ.	Max.	Unit
C _{IN}	Input Capacitance V _I = V _{DD} or GND	—	5	—	pF
C _O	Output Capacitance V _O = V _{DD} or GND	—	6	—	pF
C _L	Load Capacitance	—	30	—	pF

NOTE:

1. Unused inputs must be held HIGH or LOW to prevent them from floating.

RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Min.	Max.	Unit
V _{DD} , AV _{DD}	Power Supply Voltage	3	3.6	V
T _A	Operating Free-Air Temperature	0	+85	°C

PIN DESCRIPTION

Terminal		Type	Description
Name	No.		
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CSP2510C clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
G	11	I	Output bank enable. G is the output enable for outputs Y(0:9). When G is low, outputs Y(0:9) are disabled to a logic-low state. When G is high, all outputs Y(0:9) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
Y (0:9)	3, 4, 5, 8, 9, 15, 16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank Y(0:9) is enabled via the G input. These outputs can be disabled to a logic-low state by de-asserting the G control input.
AVDD	23	Power	Analog power supply. AVDD provides the power reference for the analog circuitry. In addition, AVDD can be used to bypass the PLL for test purposes. When AVDD is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
VDD	2, 10, 14, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

STATIC FUNCTION TABLE (AVDD = 0V)

Inputs		Outputs	
G	CLK	Y(0:9)	FBOUT
L	L	L	L
L	H	L	H
H	H	H	H
H	L	L	L
H	running	running	running

DYNAMIC FUNCTION TABLE (AVDD = 3.3V)

Inputs		Outputs	
G	CLK	Y(0:9)	FBOUT
X	L	L	L
L	running	L	running in phase with CLK
L	H	L	H
H	running	running in phase with CLK	running in phase with CLK
H	H	H	H

DC ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE⁽¹⁾

Symbol	Description	Test Conditions	V _{DD}	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IK}	Input Clamp Voltage	I _I = -18mA	3V	—	—	-1.2	V
V _{IH}	Input HIGH Level		—	2	—	—	V
V _{IL}	Input LOW Level		—	—	—	0.8	V
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100µA	Min. to Max.	V _{DD} -0.2	—	—	V
		I _{OH} = -12mA	3V	2.1	—	—	
		I _{OH} = -6mA	3V	2.4	—	—	
V _{OL}	LOW Level Output Voltage	I _{OL} = 100µA	Min. to Max.	—	—	0.2	V
		I _{OL} = 12mA	3V	—	—	0.8	
		I _{OL} = 6mA	3V	—	—	0.55	
I _I	Input Current	V _I = V _{DD} or GND	3.6V	—	—	±5	µA
I _{DD}	Supply Current	V _I = V _{DD} or GND, AV _{DD} = GND, I _O = 0, Outputs: LOW or HIGH	3.6V	—	—	10	µA
ΔI _{DD}	Change in Supply Current	One input at V _{DD} - 0.6V, other inputs at V _{DD} or GND	3.3V to 3.6V	—	—	500	µA
C _{PD}	Power Dissipation Capacitance		3.6V	—	10	14	pF
I _{DDA} ⁽³⁾	AV _{DD} Power Supply Current		AV _{DD} = 3.3V	—	10	—	mA

NOTES:

1. For Industrial devices, operating free-air temperature = -40°C to +85°C.
2. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
3. For I_{DD} of AV_{DD}, see TYPICAL CHARACTERISTICS.

TIMING REQUIREMENTS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE⁽¹⁾

		Min.	Max.	Unit
f _{CLOCK}	Clock frequency	25	140	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time ⁽²⁾	—	1	ms

NOTES:

1. For Industrial devices, operating free-air temperature = -40°C to +85°C.
2. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

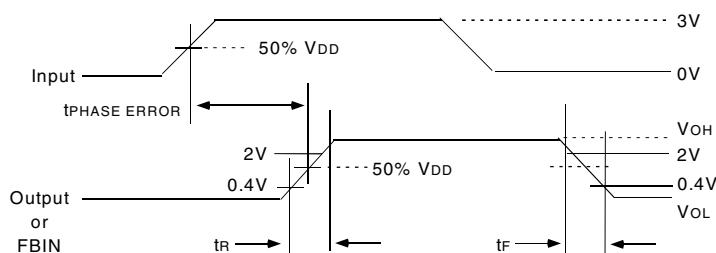
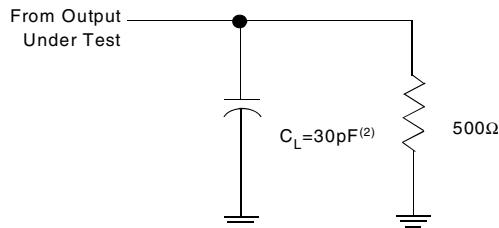
SWITCHING CHARACTERISTICS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, $C_L = 30\text{pF}^{(1)}$

Parameter ⁽²⁾	From (Input)	To (Output)	$V_{DD} = 3.3V \pm 0.3V$			Unit
			Min.	Typ.	Max.	
t_{PHASE} error	$100\text{MHz} < \text{CLK}\uparrow < 133\text{MHz}$	$\text{FBIN}\uparrow$	-150	—	150	ps
t_{PHASE} error - jitter ⁽³⁾	$\text{CLK}\uparrow = 133\text{MHz}$	$\text{FBIN}\uparrow$	-50	—	50	ps
$t_{\text{SK}(o)}^{(4)}$	Any Y (133MHz)	Any Y	—	—	150	ps
Jitter (cycle-cycle) (peak-to-peak)	$\text{CLK} = 133\text{MHz}$	Any Y or FBOUT	-75	—	75	ps
Duty cycle reference ⁽⁵⁾	$\text{CLK} = 133\text{MHz}$	Any Y or FBOUT	45	—	55	%
t_R		Any Y or FBOUT	0.8	—	2.1	ns
t_F		Any Y or FBOUT	0.8	—	2.7	ns

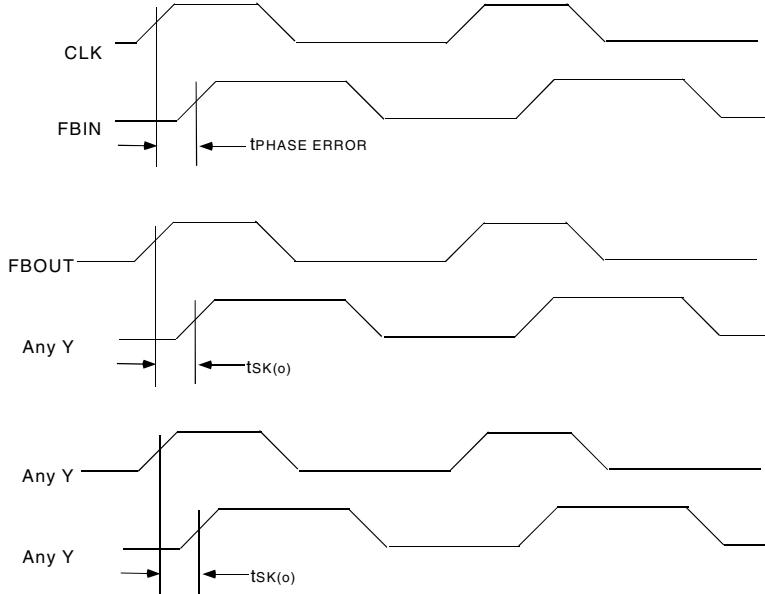
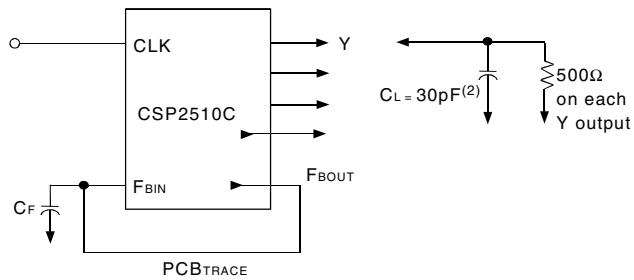
NOTES:

1. For Industrial devices, operating free-air temperature = -40°C to +85°C. See PARAMETER MEASUREMENT INFORMATION.
2. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
3. Phase error does not include jitter.
4. The $t_{\text{SK}(o)}$ specification is only valid for equal loading of all outputs.
5. See TYPICAL CHARACTERISTICS.

PARAMETER MEASUREMENT INFORMATION⁽¹⁾



Load Circuit and Voltage Waveforms



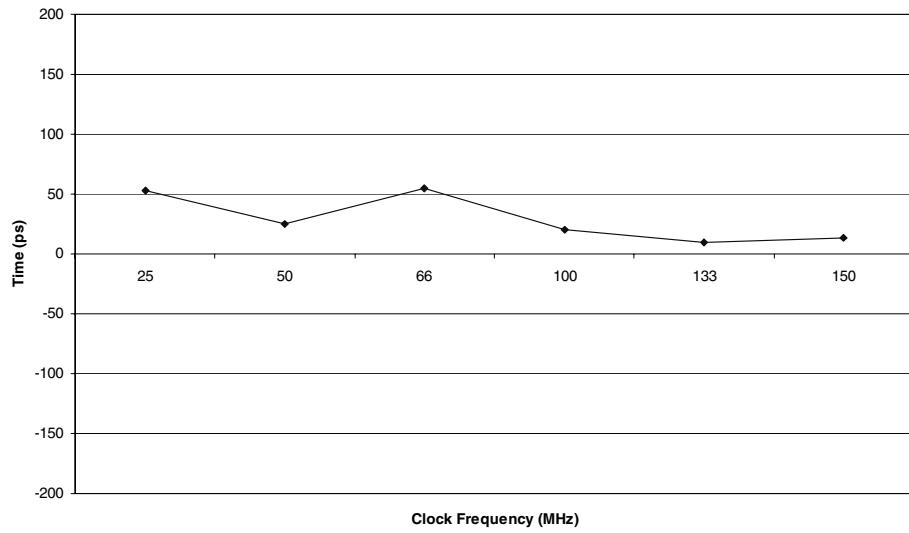
Phase ERROR and Skew Calculations^(3,4)

NOTES:

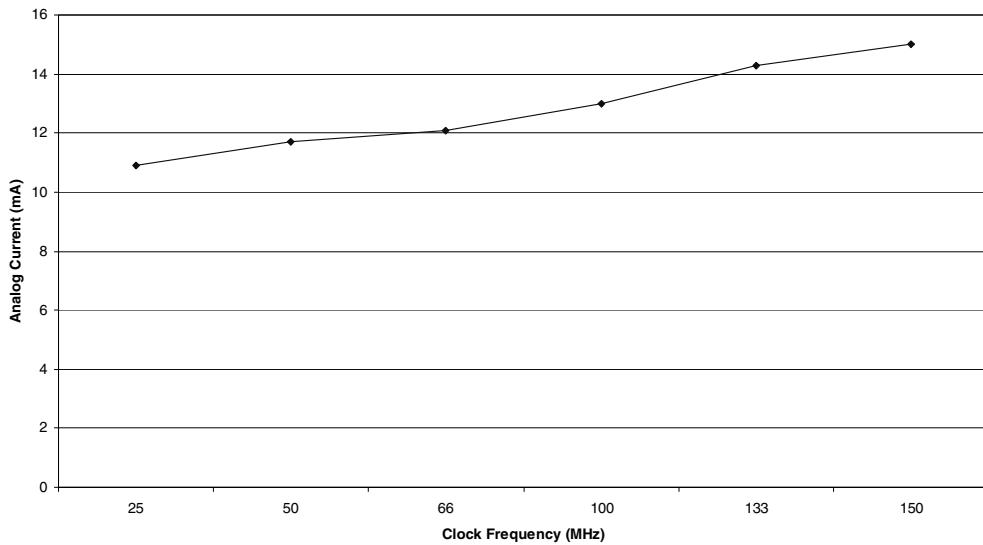
1. All inputs pulses are supplied by generators having the following characteristics: PRR $\leq 100\text{MHz}$ $Z_0 = 50\Omega$, $t_r \leq 1.2\text{ ns}$, $t_f \leq 1.2\text{ ns}$.
2. C_L includes probe and jig capacitance.
3. The outputs are measured one at a time with one transition per measurement.
4. Phase error measurements require equal loading at outputs Y and FBOUT. $C_F = C_L - C_{\text{FBIN}} - C_{\text{PCB TRACE}}$; $C_{\text{FBIN}} \approx 6\text{pF}$.

TYPICAL CHARACTERISTICS

Phase Error vs Clock Frequency
AV_{DD} and V_{DD} = 3.3V
Ta = 25C

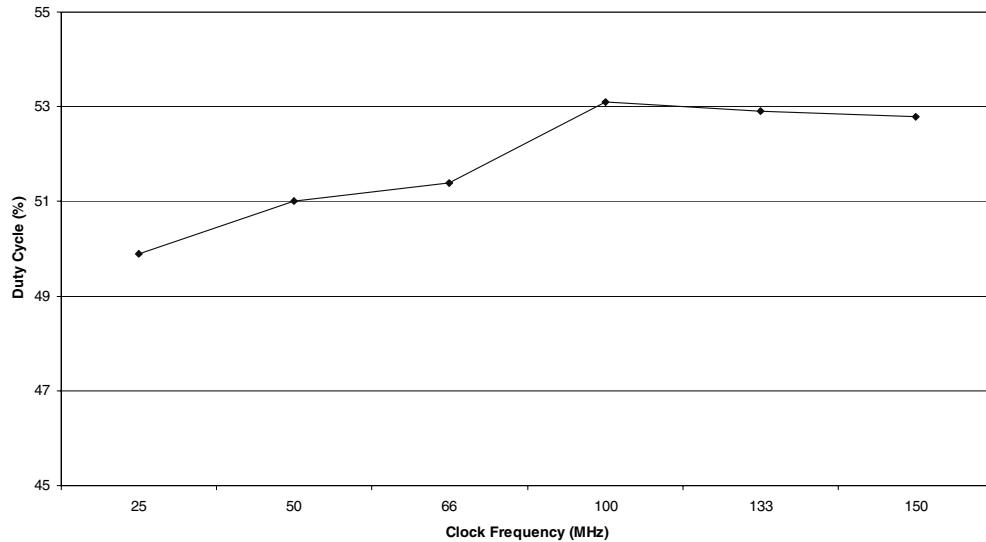


Analog Supply Current vs. Clock Frequency
AV_{DD} and V_{DD} = 3.3V
Ta = 25C

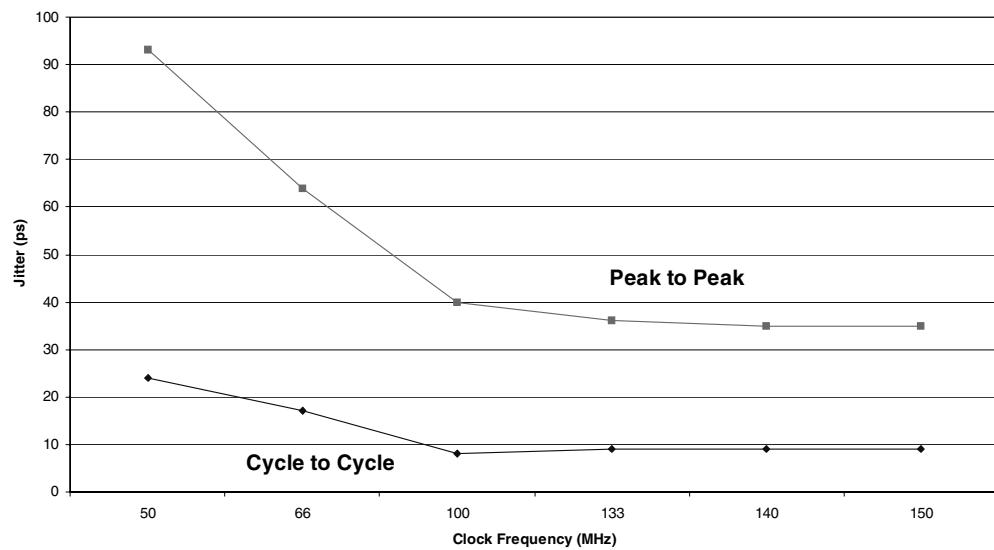


TYPICAL CHARACTERISTICS (CONT.)

Output Duty Cycle vs Clock Frequency
AV_{DD} and V_{DD} = 3.3V
Ta = 25C



Jitter vs Clock Frequency
Avcc and Vcc = 3.3V
Ta = 25C



ORDERING INFORMATION

CSP	<u>XXXXX</u>	<u>XX</u>	<u>X</u>	
Device Type	Package	Process		
			Blank	0°C to +85°C (standard)
			I	-40°C to +85°C (Industrial)
		PG		Thin Shrink Small Outline Package
		PGG		TSSOP - Green
	2510C			Phase-Lock Loop Clock Driver

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.