

CD4073BMS, CD4081BMS, CD4082BMS

CMOS AND Gate

FN3324  
Rev 1.00  
October 2015

**Features**

- High-Voltage Types (20V Rating)
- CD4073BMS Triple 3-Input AND Gate (No longer available or supported)
- CD4081BMS Quad 2-Input AND Gate
- CD4082BMS Dual 4-Input AND Gate (No longer available or supported)
- Medium Speed Operation:
  - tPLH, tPHL = 60ns (typ) at VDD = 10V
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

**Description**

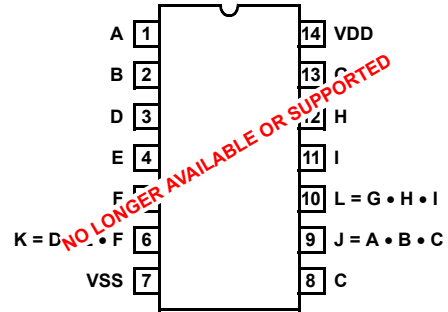
CD4073BMS, CD4081BMS and CD4082BMS AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of CMOS gates.

The CD4073BMS, CD4081BMS and CD4082BMS are supplied in these 14 lead outline packages:

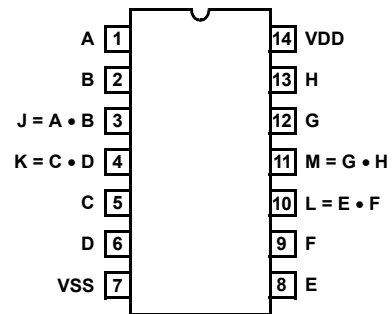
Braze Seal DIP	*H4Q	†H4H
Frit Seal DIP	*H1B	
Ceramic Flatpack	*H3W	
*CD4073B, CD4081B	†CD4082B	

**Pinout**

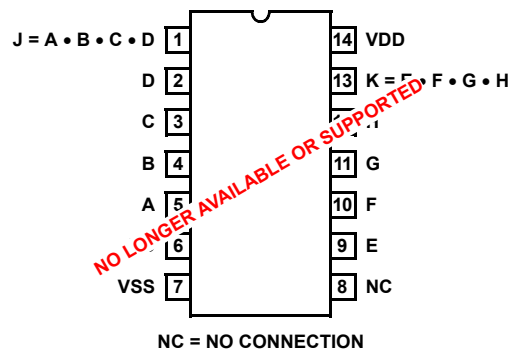
CD4073BMS  
TOP VIEW



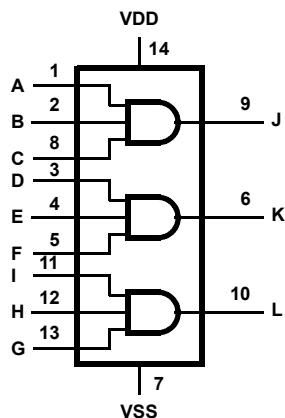
CD4081BMS  
TOP VIEW



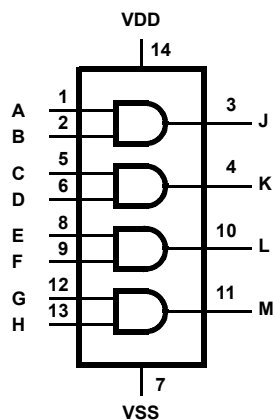
CD4082BMS  
TOP VIEW



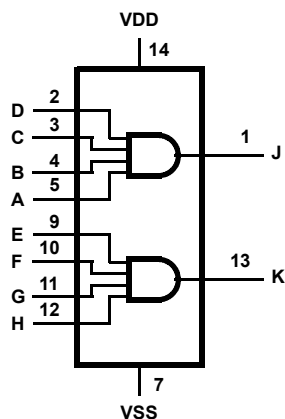
**Functional Diagram**



**CD4073BMS**



**CD4081BMS**



**CD4082BMS**

**Absolute Maximum Ratings**

DC Supply Voltage Range, (VDD).....-0.5V to +20V  
 (Voltage Referenced to VSS Terminals)  
 Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V  
 DC Input Current, Any One Input .....±10mA  
 Operating Temperature Range ..... -55°C to +125°C  
 Package Types D, F, K, H  
 Storage Temperature Range (TSTG) ..... -65°C to +150°C  
 Lead Temperature (During Soldering).....+265°C  
 At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s  
 Maximum

**Reliability Information**

Thermal Resistance .....  $\theta_{ja}$   $\theta_{jc}$   
 Ceramic DIP and FRIT Package..... 80°C/W 20°C/W  
 Flatpack Package ..... 70°C/W 20°C/W  
 Maximum Package Power Dissipation (PD) at +125°C  
 For TA = -55°C to +100°C (Package Type D, F, K) ..... 500mW  
 For TA = +100°C to +125°C (Package Type D, F, K)..... Derate  
 Linearity at 12mW/°C to 200mW  
 Device Dissipation per Output Transistor ..... 100mW  
 For TA = Full Package Temperature Range (All Package Types)  
 Junction Temperature..... +175°C

**TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
			VDD = 18V	2	+125°C	-1000	-	nA
				3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
			VDD = 18V	2	+125°C	-	1000	nA
				3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.  
 2. Go/No Go test with limits applied to inputs.  
 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

**TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	.25	μA
				+125°C	-	7.5	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	.5	μA
				+125°C	-	15	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	.5	μA
				+125°C	-	30	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
	TTLH	VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

**TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

- NOTES: 1. All voltages referenced to device GND. 2. CL = 50pF, RL = 200K, Input TR, TF < 20ns. 3. See Table 2 for +25°C limit. 4. Read and Record

**TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C**

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

**TABLE 6. APPLICABLE SUBGROUPS**

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	
Group A	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

**TABLE 6. APPLICABLE SUBGROUPS (Continued)**

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2, 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

**TABLE 7. TOTAL DOSE IRRADIATION**

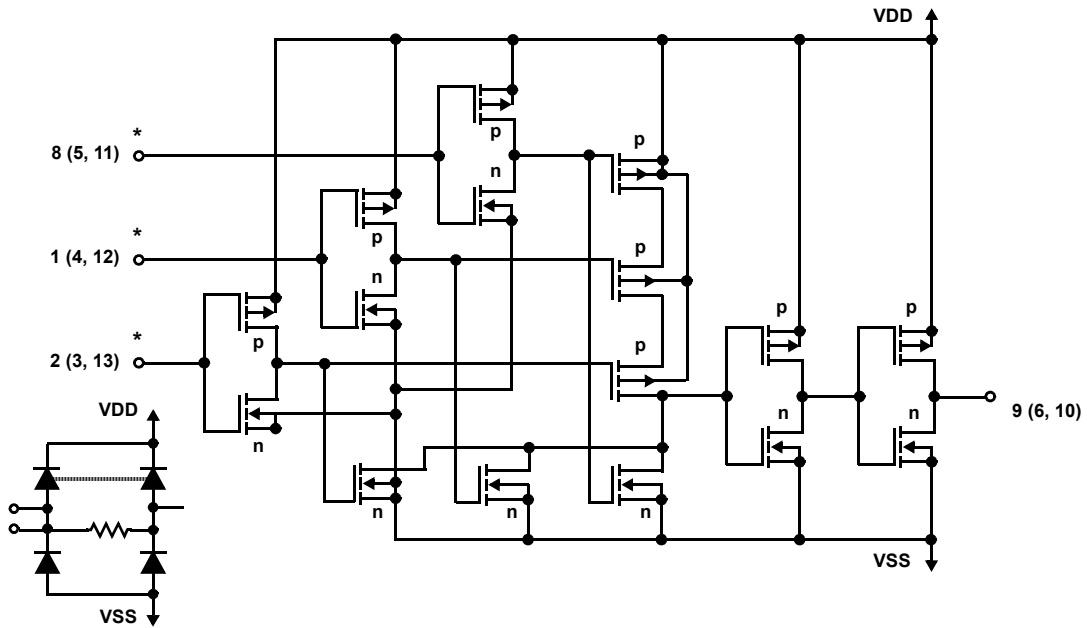
CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

**TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS**

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4073BMS						
Static Burn-In 1 Note 1	6, 9, 10	1 - 5, 7, 8, 11 - 13	14			
Static Burn-In 2 Note 1	6, 9, 10	7	1 - 5, 8, 11 - 14			
Dynamic Burn-In Note 1	-	7	14	6, 9, 10	1, 5, 8, 11 - 13	
Irradiation Note 2	6, 9, 10	7	1 - 5, 8, 11 - 14			
PART NUMBER CD4081BMS						
Static Burn-In 1 Note 1	3, 4, 10, 11	1, 2, 5 - 9, 12, 13	14			
Static Burn-In 2 Note 1	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14			
Dynamic Burn-In Note 1	-	7	14	3, 4, 10, 11	1, 2, 5, 6, 8, 9, 12, 13	
Irradiation Note 2	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14			
PART NUMBER CD4082BMS						
Static Burn-In 1 Note 1	1, 6, 8, 13	2 - 5, 7, 9 - 12	14			
Static Burn-In 2 Note 1	1, 6, 8, 13	7	2 - 5, 9 - 12, 14			
Dynamic Burn-In Note 1	6, 8	7	14	1, 3	2 - 5, 9 - 12	
Irradiation Note 2	1, 6, 8, 13	7	2 - 5, 9 - 12, 14			

NOTE:

- Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
- Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V



ALL INPUTS PROTECTED BY CMOS PROTECTION NETWORK

FIGURE 1. SCHEMATIC DIAGRAM FOR CD4073BMS (1 OF 3 IDENTICAL GATES)

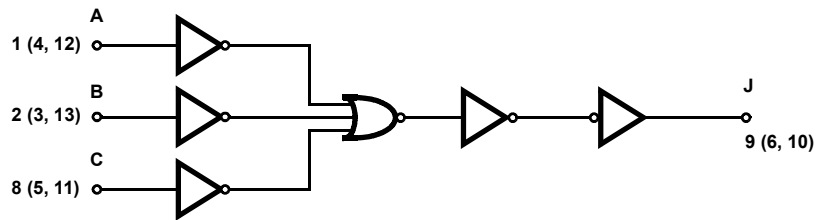
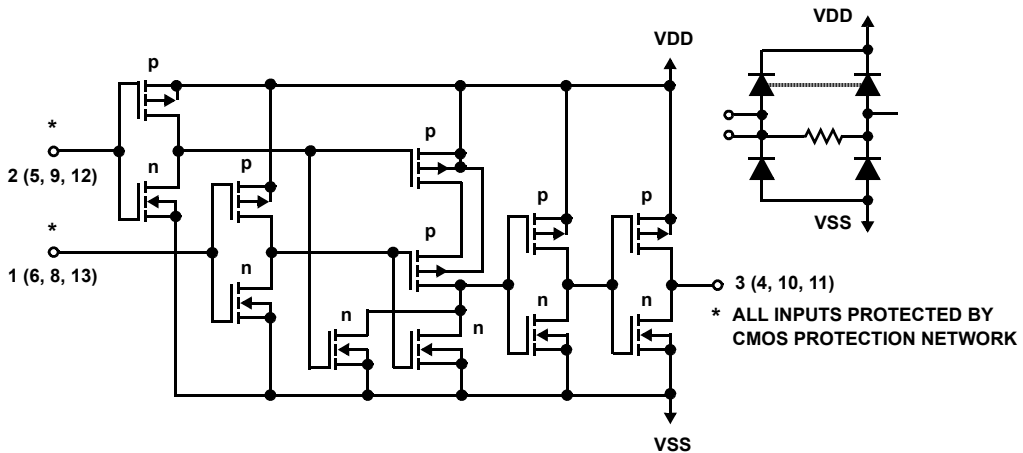


FIGURE 2. LOGIC DIAGRAM FOR CD4073BMS (1 OF 3 IDENTICAL GATES)



\* ALL INPUTS PROTECTED BY CMOS PROTECTION NETWORK

FIGURE 3. SCHEMATIC DIAGRAM FOR CD4081BMS (1 OF 4 IDENTICAL GATES)

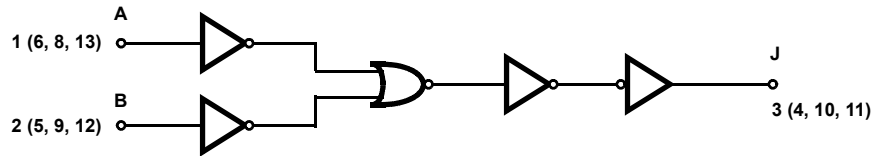


FIGURE 4. LOGIC DIAGRAM FOR CD4081BMS (1 OF 4 IDENTICAL GATES)

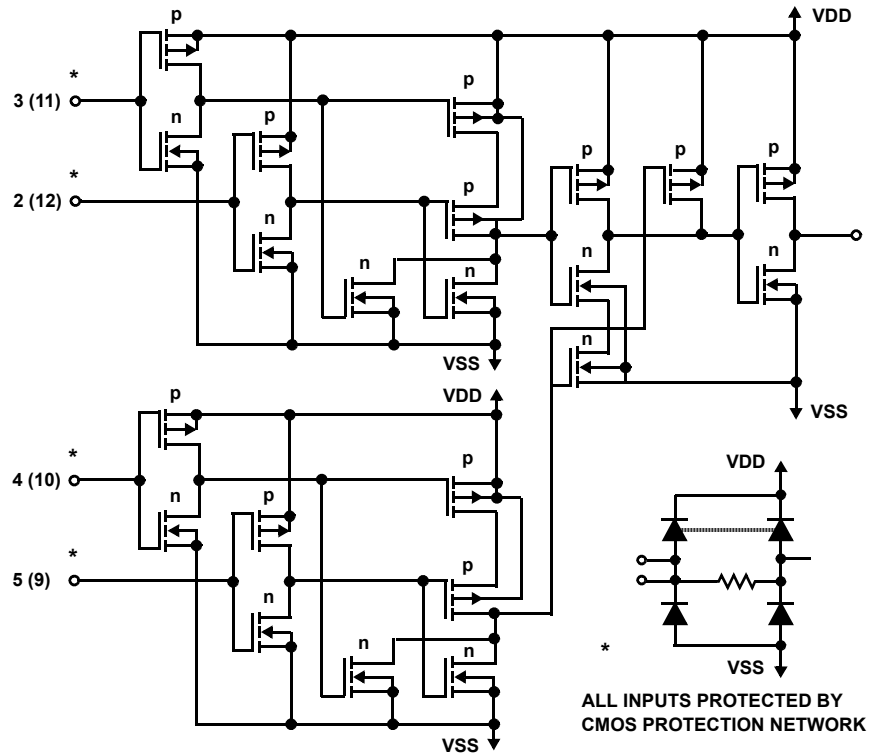


FIGURE 5. SCHEMATIC DIAGRAM FOR CD4082BMS (1 OF 2 IDENTICAL GATES)

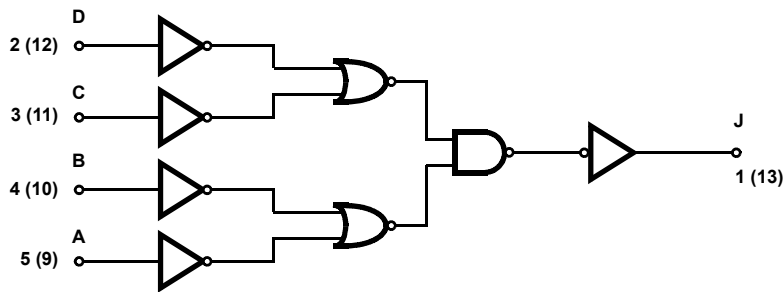


FIGURE 6. LOGIC DIAGRAM FOR CD4082BMS (1 OF 2 IDENTICAL GATES)



### Typical Performance Characteristics

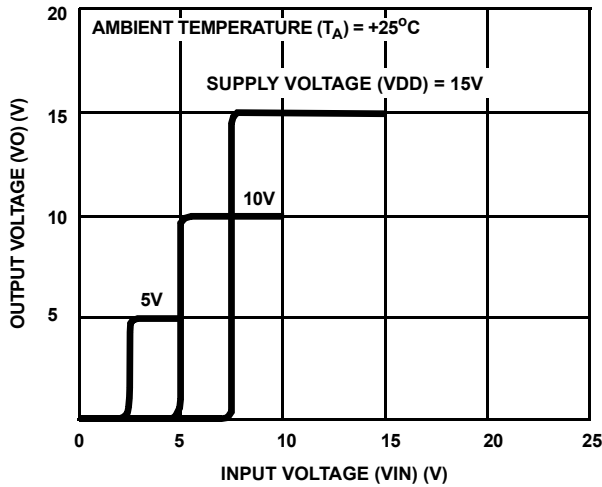


FIGURE 7. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

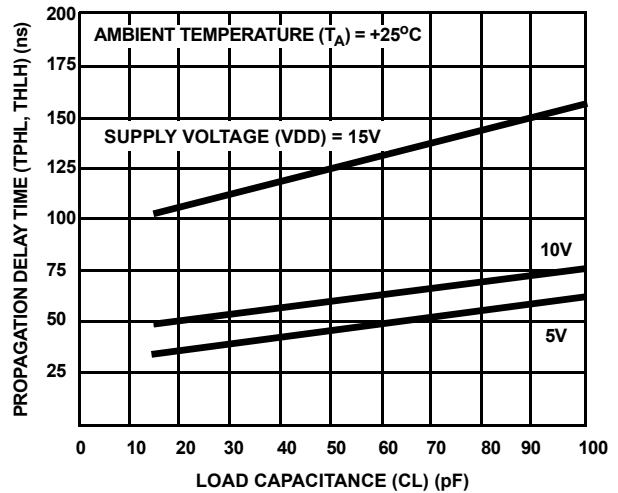


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

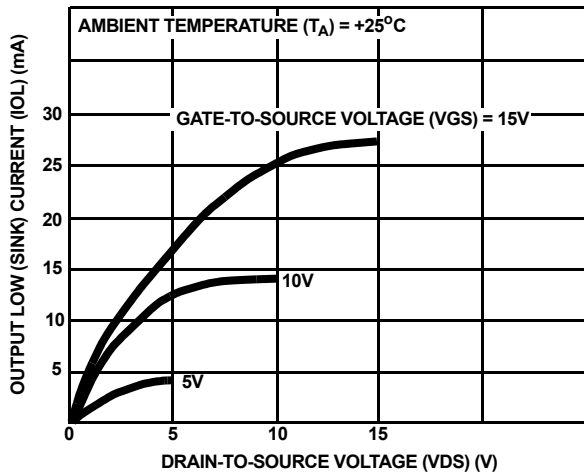


FIGURE 9. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

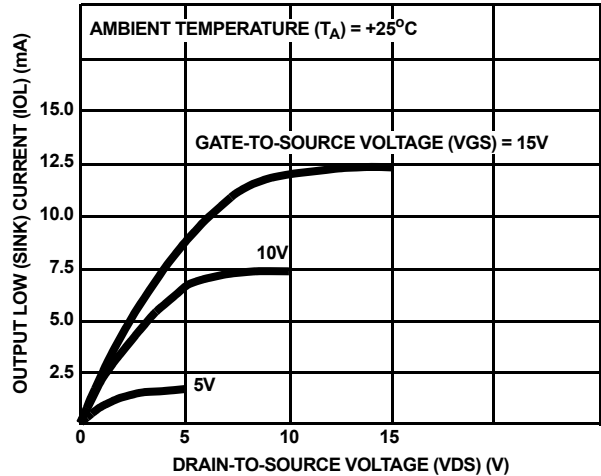


FIGURE 10. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

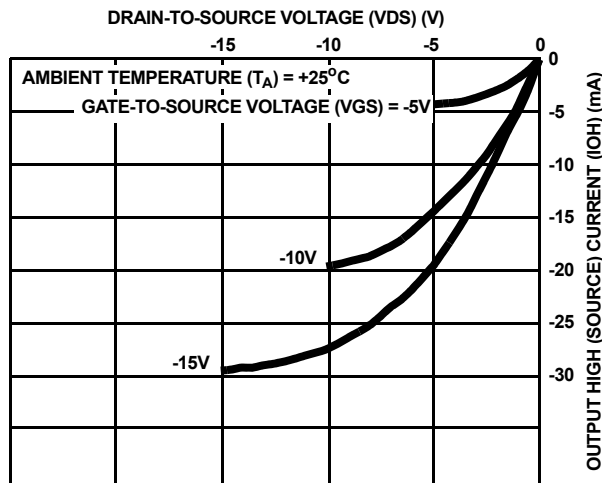


FIGURE 11. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

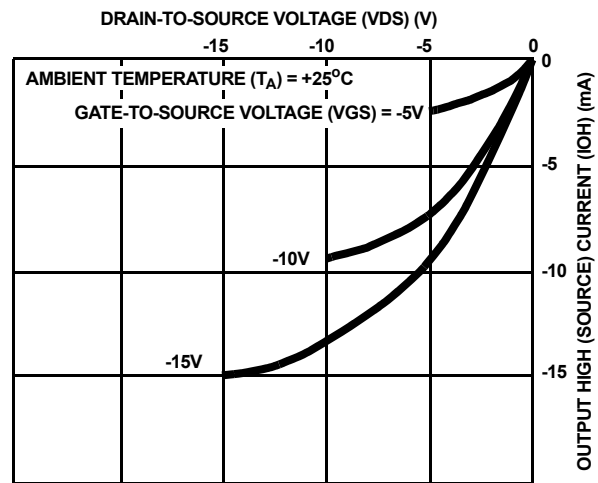


FIGURE 12. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

**Typical Performance Characteristics (Continued)**

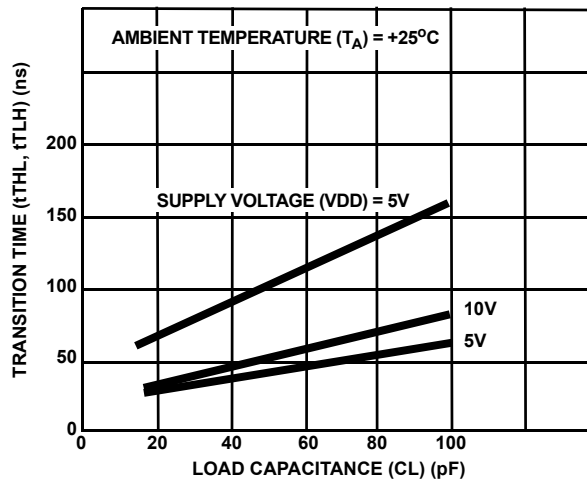


FIGURE 13. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

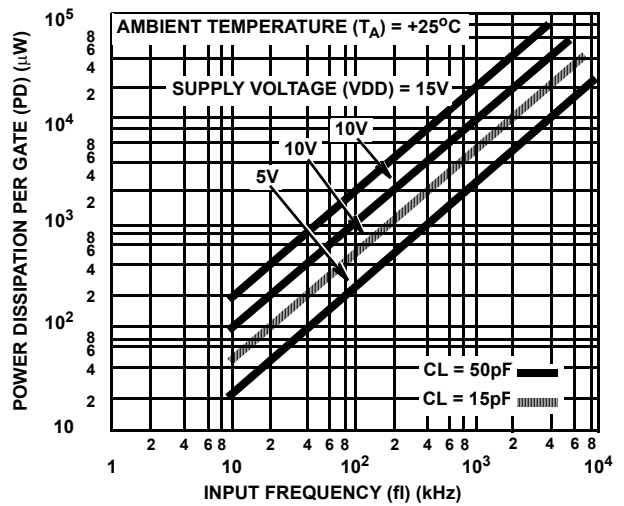
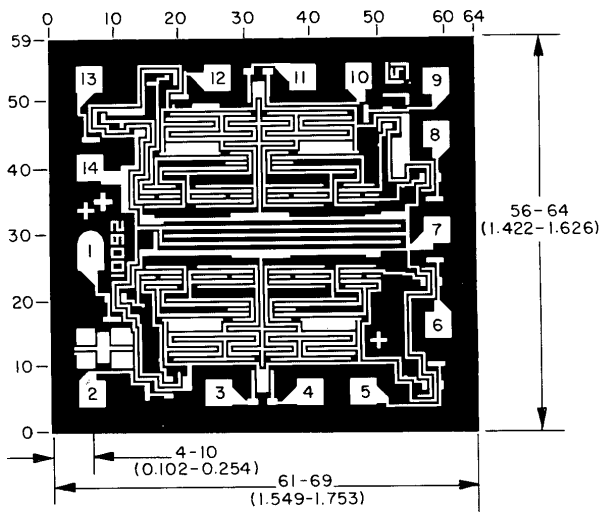
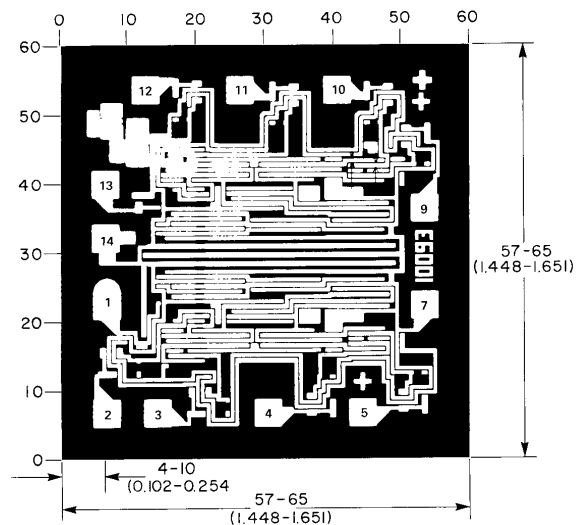


FIGURE 14. TYPICAL DYNAMIC POWER DISSIPATION PER GATE AS A FUNCTION OF FREQUENCY

**Chip Dimensions and Pad Layouts**

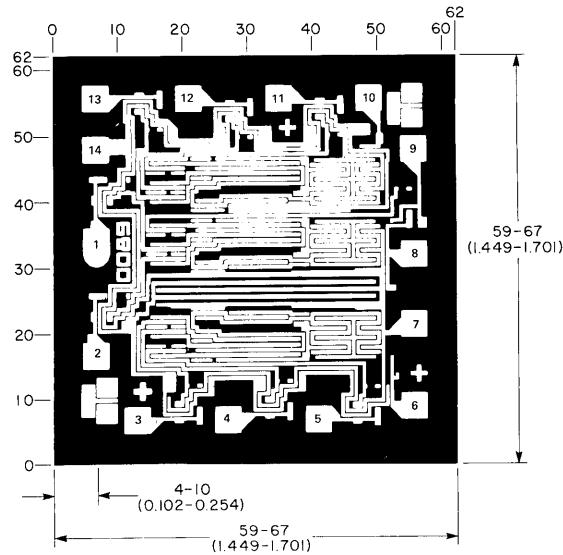


CD4081BMS



CD4082BMS

## Chip Dimensions and Pad Layouts



**CD4073BMS**

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.  
Grid graduations are in mils ( $10^{-3}$  inch)

- METALLIZATION:** Thickness:  $11\text{k}\text{\AA}$  –  $14\text{k}\text{\AA}$ , AL.
- PASSIVATION:**  $10.4\text{k}\text{\AA}$  -  $15.6\text{k}\text{\AA}$ , Silane
- BOND PADS:** 0.004 inches X 0.004 inches MIN
- DIE THICKNESS:** 0.0198 inches - 0.0218 inches

© Copyright Intersil Americas LLC 1999-2015. All Rights Reserved.  
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see [www.intersil.com/en/products.html](http://www.intersil.com/en/products.html)

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at [www.intersil.com/en/support/qualandreliability.html](http://www.intersil.com/en/support/qualandreliability.html)

*Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)