CCE4503

IO-Link Device Transceiver

The CCE4503 is an easy-to-use device side IO-Link compliant transceiver. It combines IO-Link compliant communication capability with advanced protection circuitry and additional features while keeping the application small and simple. Controlled by an UART interface (TXD, RXD, TXEN), the output drivers can be configured as PNP, NPN or Push-Pull. Three LDO options and an automatic wake-up detection simplify the overall system requirements and reduce the need for additional external circuitry. The integrated protection features such as reverse-polarity protection, overcurrent protection, undervoltage detection and thermal protection ensure a robust functionality and communication. With the small 3mm x 3mm DFN10 package size, it is especially suitable for space limited sensor and actuator applications.

Features

- IO-Link Compliant Transceiver
- One IO-Link channel with up to 250 mA permanent driving current
- 350 mA peak (typ.)
- Configurable PNP-, NPN- and
- Push-Pull mode
- Configurable current limit
- Configurable slew rate limitation for optimized EMC
- Wake-up detection
- Small DFN 10-pin package
- 3 LDO Options with up to 20 mA
- 3.3V LDO output
- 5V LDO output
- External LDO
- Reverse-polarity protection
- Overcurrent detection
- Undervoltage detection
- Overtemperature detection

Applications

- IO-Link Sensors
- IO-Link Actuators
- High voltage level shifter
- Industrial automation

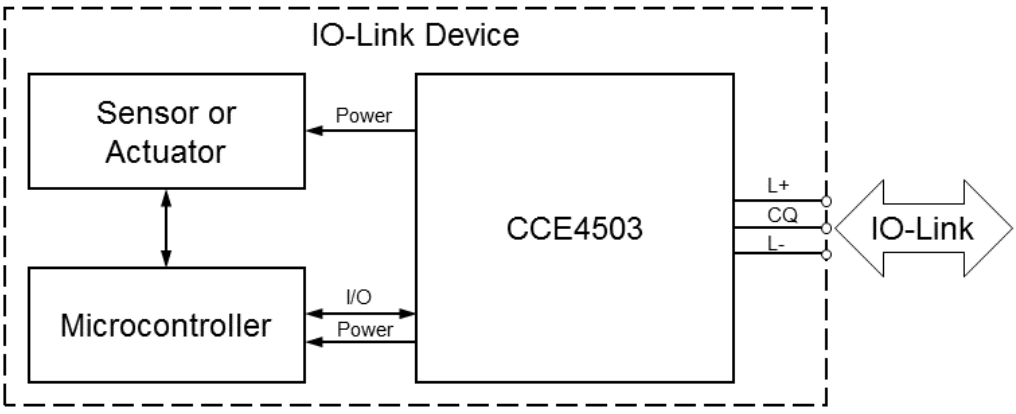


Figure 1. Application Diagram

Contents

1. Overview

1.1 Block Diagram

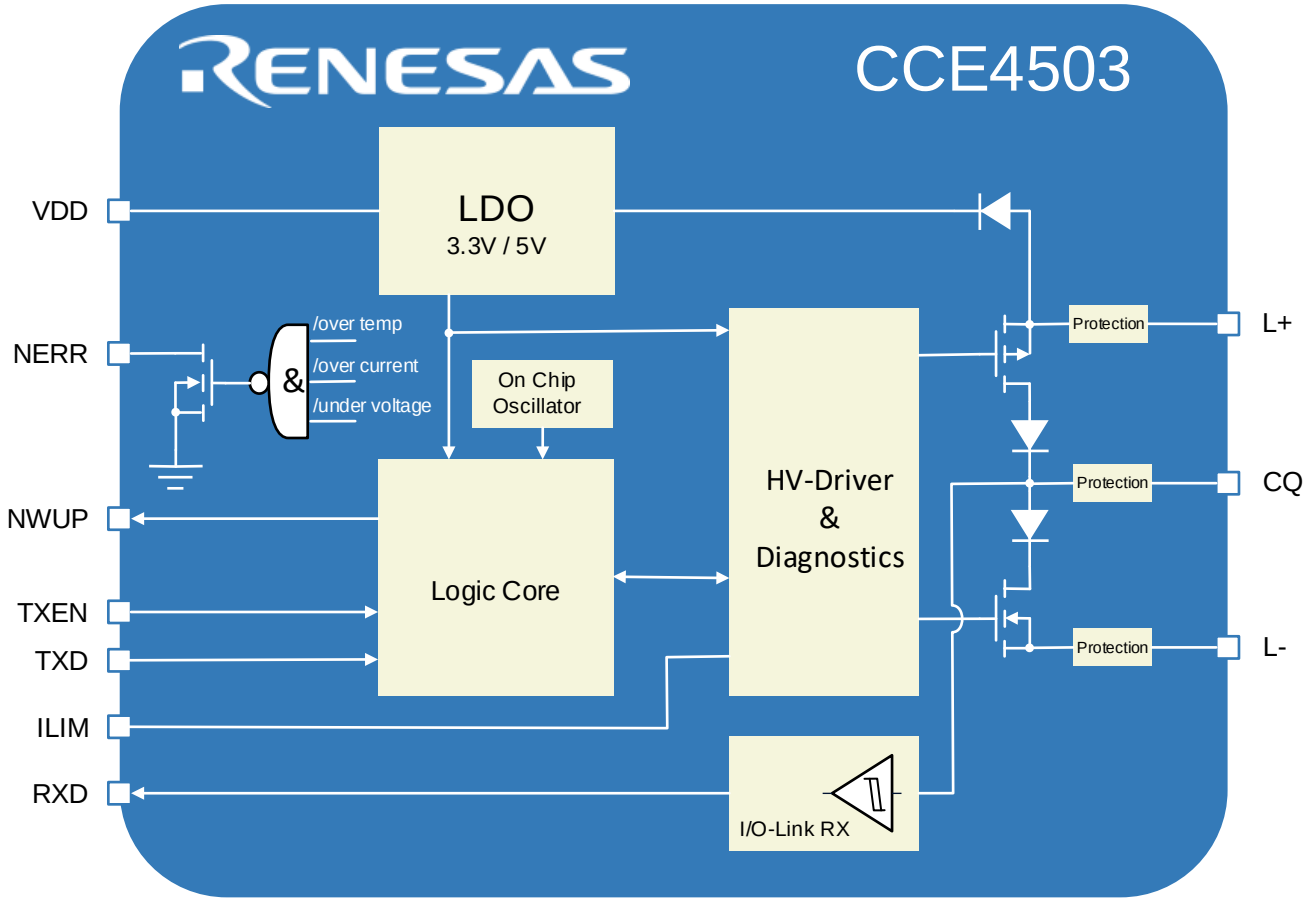


Figure 2: Block Diagram

2. Pin Information

2.1 Pin Assignment

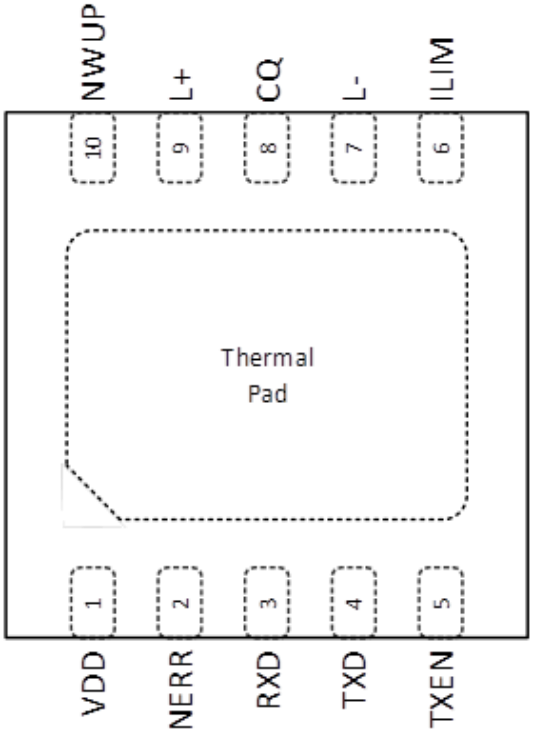


Figure 3: DFN10 Pinout Diagram (Top View)

2.2 Pin Descriptions

Pin Number	Pin Name	Type	Rest State	Description
1	VDD	PWR		3.3V - 5V Supply Voltage Input / Output
2	NERR	OD	High-Z	Error Output (Overcurrent detection, Undervoltage detection, Overtemperature detection
3	RXD	DO		Channel signal output
4	TXD	DI, PU		Channel signal input
5	TXEN	DI, PD		Channel driver enable
6	ILIM	AI		Current Limit configuration
7	L-	PWR		Ground supply (IO-Link)
8	CQ	DIO		IO-Link data
9	L+	PWR		Positive supply (IO-Link)
10	NWUP	OD	High-Z	Wake-up detection (Channel short detection)
PAD	Thermal Pad	GND		Thermal Pad, connect to VSS or leave open

2.3 Pin Type Definition

Pin Type	Description
DI	Digital input
DO	Digital output
DIO	Digital input/output
OD	Digital Output open drain
PU	Pull-up resistor (fixed)
PD	Pull-down resistor (fixed)
PWR	Power
AI	Analog input
AO	Analog output
AIO	Analog input/output
BP	Back drive protection
SPU	Switchable pull-up resistor
SPD	Switchable pull-down resistor
GND	Ground

3. Characteristics

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Conditions	Name	Min	Max	Unit
Supply Voltage	Static, referenced to V_{L-}	V_{L+} - V_{L-}	-40	40	V
Supply Voltage	Dynamic (t ≤ 100 µs)	V_{L+} - V_{L-_pulse}	-42	42	V
Storage Temperature		$T_{storage}$	-55	+175	°C
Voltage at pin CQ	Referenced to V_{L-}: V_{CQ} - V_{L-}	$V_{CQ,max}$	V_{L-} -1V	V_{L+} +1V	V
Voltage at all other pins	Referenced to V_{L-}	V_{IOmax}	-0.7	V_{DD} +0.7	V
Logic Level Supply Voltage		VDD_{max}		6	V
Output current	At pin RXD, NWUP, NERR	I_{OutMax}	-5	5	mA

3.2 ESD Ratings

ESD Model/Test	Rating	Unit
Human Body Model (Tested per JS-001-2012 HBM)	4 (8[1])	kV
ESD Contact Discharge (Tested per IEC61000-4-2)[2]	16	kV
Electrical Fast Transient (Burst) (Tested per IEC61000-4-4) [3]	TBD	kV
Surge (Tested per IEC61000-4-5, adapted to 500 Ω 1.2/50 µs)[4]	0.8 (5[5])	kV
Latch-Up (Tested per JESD78E; Class 1 & 2)	100	mA

[1] Higher Rating for L+, L- and CQ
[2] Valid for L+, L- and CQ
[3] Valid for L+, L- and CQ
[4] Valid for L+, L- and CQ; 100 nF between L+ and L-, 1 µF between VDD and GND
[5] Up to 5 kV with TVS Diodes (e.g. SMAJ33A) connected between L+, L- and CQ (higher Voltages have not been tested)

3.3 Recommended Operating Conditions

Parameter	Conditions	Pin	Name	Min	Typ	Max	Unit
Main Supply Voltage		7, 9	V_{L+}	7		36	V
Supply Voltage Ripple	F_{ripple} = DC … 100kHz V_{L+} > 12 V	9	ΔV_{L+}			1	V
Voltage CQ	Receiver mode	8	V_{CQ_MAX}	V_{L-}		V_{L+}	V
Logic Level Supply Voltage	External Supply	1	VDD	3		5.5	V
Operating Temperature	Ambient temperature		T_{amb}	-40		+125	°C
Junction Temperature			T_j	-40		+150	°C
LDO Output Current	3.3V LDO or 5V LDO	1	I_{VDD}			20	mA
ILIM External Resistor	To L-	6	R_{ILIM}	0		100	kΩ
LDO External Capacitor	To L-	1	C_{LDO}	0.8	1	1.2	µF

3.4 Electrical Characteristics

The electrical parameters are valid for the entire range of operating conditions as specified under 3.3 “Recommended Operating conditions” unless noted otherwise.

3.4.1. Input / Output CQ

Parameter	Conditions	Pin	Name	Min	Typ	Max	Unit
Output voltage low level	active pull down, I_{OL}=-200mA	8	V_{OL}	0		1.5	V
Output voltage high level	active pull up, I_{OH}=+200mA	8	V_{OH}	V_{L+} - 1.5		V_{L+}	V
Leakage current	input enabled 0 ≤ V_{CQ} ≤ V_{L+} - 0.1 V	8	I_{leak}	-2		2	µA
Maximum Permanent Output Current	Current of CQ channel	8	I_{CQmax}	-250		250	mA
Output source current limit	R_{ILIM} = 0 or hZ R_{ILIM} = 100 kΩ	8	I_{limP}	300 35	350 50	400 70	mA
Output sink current limit	R_{ILIM} = 0 or hZ R_{ILIM} = 100 kΩ	8	I_{limN}	-400 -70	-350 -50	-300 -35	mA
Load capacitance		8	C_L			5	nF
Output rise/fall time (20% to 80%)	Open load, R_{ILIM} = 0 or hZ	8	$t_{r,f}$			869	ns
Switch On Time		8	t_{DLY_LH}			4	µs

Switch Off Time		8	t_{DLY_HL}			4	µs
Short circuit detection time		8	T_{SHORT}			300	µs
Short circuit disable time	RILIM ≠ hZ	8	T_{SHORT_DIS}		15		ms
Wake-up detection time start		8	T_{WAKE_S}	38	56	70	µs
Wake-up detection time end		8	T_{WAKE_E}	89	112	150	µs
Wake-up detection time delay		8	T_{WAKE_D}			150	µs
Input threshold high level		8	V_{IH}	10.5	11.75	13	V
Input threshold low level		8	V_{IL}	8	9.75	11.5	V
Hysteresis between input thresholds high and low		8	V_{Hyst}		2		V

3.4.2. Digital I/O

Parameter	Conditions	Pin	Name	Min	Typ	Max	Unit
Input							
Input Voltage LOW		4, 5	V_{IN_L}			0.3 * VDD	V
Input Voltage HIGH		4, 5	V_{IN_H}	0.7 * VDD			V
Input Pull-Up current	V_{pin}=0V	4, 5	I_{PU}	4	30	110	µA
Input Pull-Down current	V_{pin}= VDD	4, 5	I_{PD}	-110	-30	-4	µA
Output							
Output Voltage LOW	I_{OUT_LOW} = 2 mA	2, 3, 10	V_{OUT_L}			0.4	V
Output Voltage HIGH	I_{OUT_HIGH} = 2 mA	3	V_{OUT_H}	0.8 * VDD			V

3.4.3. 3.3V / 5V Voltage Regulator

Parameter	Conditions	Pin	Name	Min	Typ	Max	Unit
Output Voltage VDD	3.3V Regulator	1	VDD_{3V3}	3.0	3.3	3.6	V
	5V Regulator	1	VDD_{5V}	4.5	5	5.5	V
Voltage Drop	Load Current = 20 mA	1	V_{DO}			2	V
Output Current VDD		1	I_{VDD}			20	mA
Line regulation	I_{OUT} = 1 mA V_{L+} = 24 V	1	REG			2	mV/V
Load regulation	DC current up to 20 mA V_{L+} = 24 V	1				1	%
Power Supply rejection ratio	100 kHz, I_{OUT} = 20 mA	1	PSRR	40			dB
Power-On Threshold	Only applies to the driver without LDO (CCE4503-0V)	1	V_{RST}	2.7		3.0	V
Undervoltage lockout voltage (V_{L+})		1	$V_{L+,min}$		6		V
Undervoltage lockout voltage (V_{DD})		1	$V_{DD,min}$			3	V
Start-up time		1				5	µs

3.5 Thermal Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{ALARM_H}	Alarm temperature (higher threshold)		150	165	180	°C
T_{ALARM_L}	Alarm temperature (lower threshold)		140	155	170	°C
$T_{WARNING}$	Warning temperature (higher threshold)		125	140	155	°C
R_{tja}	Thermal resistance (junction to ambient)				30	K/W

4. Electrical Specifications

CCE4503 is a fully reverse polarity protected IO-Link device transceiver with one IO-Link channel. The system consists of a high voltage output stage with integrated overcurrent protection, a high voltage input stage with a spike-tolerant filter, a logic core with UART interface, an internal oscillator and an optional LDO. The LDO output voltage is factory programmed and needs to be specified with the order. To simplify the IO-Link protocol handling, a wake-up detection and automatic recovery function are implemented. Additional advanced protection features such as overtemperature detection and undervoltage detection ensure robust functionality in industrial applications. All pins are ESD-protected.

4.1 Output Stage

The output stage switches the output transistors in regard to TXD and TXEN. In IO-Link mode or Push-Pull mode TXEN is used to enable or disable the output stage. If TXEN is set high, the output stage is enabled and the output of CQ can be controlled by TXD (inverted). If TXEN is set low, the output stage is disabled and put into an inactive low-power state. RXD always reflects the current inverted state of CQ.

TXEN and TXD can also be used to configure the device in NPN, PNP and Push-Pull mode. See Table 1. NPN mode can be configured by setting TXD high and using TXEN as control pin. PNP mode can be configured by setting TXD low and using TXEN as control pin.

Table 1. Output stage truth table

Mode	TXEN	TXD	CQ
IO-Link (regular operation) / Push-Pull	0	0	High-Z
	0	1	High-Z
	1	0	1
	1	1	0
NPN	0	1	High-Z
	1	1	0
PNP	0	0	High-Z
	1	0	1

4.2 Current limit and slew rate configuration

The driver slew rate as well as the current limit is configured by a resistor R_{ILIM} connected to ILIM. The value of the resistor intended for configuration is specified between 0Ω and 100 kΩ, where a lower resistor value leads to faster switching and higher maximum currents. The automatic recovery function is only available for R_{ILIM} < 1 MΩ.

Table 2: Current limit and slew rate configuration

Resistor	Current limit	Slew rate	Automatic recovery
0Ω - 100 kΩ	350 mA - 50 mA	Fast - slow	Yes
Open (R_{ILIM} > 4 MΩ)	350 mA	Fast	No

Note: If ILIM is left open (R_{ILIM} > 4 MΩ) the output driver operates as if connected to VSS (R_{ILIM} = 0 Ω), but with automatic recovery disabled.

4.3 Automatic Recovery

If a short is detected, the output stage is automatically disabled after the time t_{SHORT}. The automatic recovery function enables the output again after t_{SHORT_DIS} and checks if the overcurrent is still present (see Figure 4).

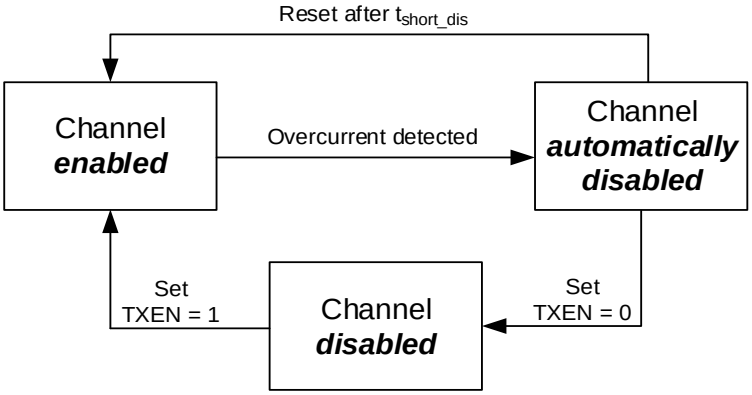


Figure 4: Automatic recovery

4.4 Wake-up detection

An overcurrent pulse of t_{WAKE} will be detected as wake-up pulse. When a wake-up pulse is detected, the output of NWUP will switch from high impedance to low until TXEN is toggled by the microcontroller.

An overcurrent pulse > t_{WAKE} will be detected as overcurrent fault condition.

An overcurrent pulse < t_{WAKE} will not be detected.

4.5 Error output handling

The error output NERR combines the indication of three error sources and will be tied low if any fault condition is detected. The following error sources are indicated by NERR:

- Overtemperature
- Undervoltage
- Overcurrent

The overtemperature and undervoltage detections are combinational outputs and keep the NERR signal low as long as the error is present. The overcurrent detection is latched and will be reset when the CCE4503 leaves the transmit mode (TXEN = 0).

4.6 Overtemperature detection

The overtemperature detection detects 3 thresholds:

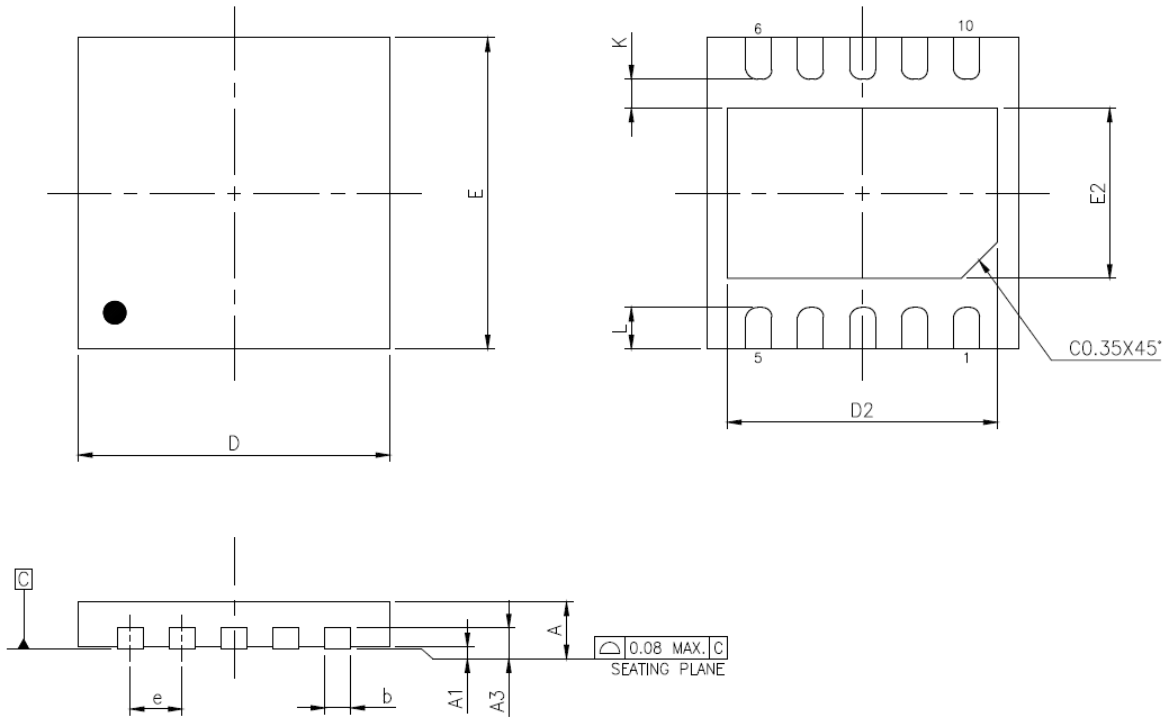
- At $T_{WARNING}$ the output of NERR will be tied low. This is a combinational signal and cannot be reset by the MCU. It will be reset once the temperature drops below $T_{WARNING}$.
- At T_{ALARM_H}, the chip will switch off the outputs. This cannot be reset by the MCU.
- When the temperature drops again below T_{ALARM_L}, the output is released and can be controlled by TXEN and TXD.

4.7 Allowed Reverse polarity connections

The CCE4503 is designed to handle all possible permutations of reverse polarity.

5. Package Information

5.1 Package Outlines



JEDEC OUTLINE	MO-229		
PKG CODE	WDFN(X310)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	3.00 BSC		
E	3.00 BSC		
e	0.50 BSC		
K	0.20	—	—

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE	VDFN	WDFN	UDFN
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF				
73*X98* MIL	2.20	2.30	2.35	1.55	1.65	1.70	0.30	0.40	0.50	V	V	(V)W3030D-5	V	V	—

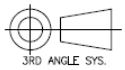
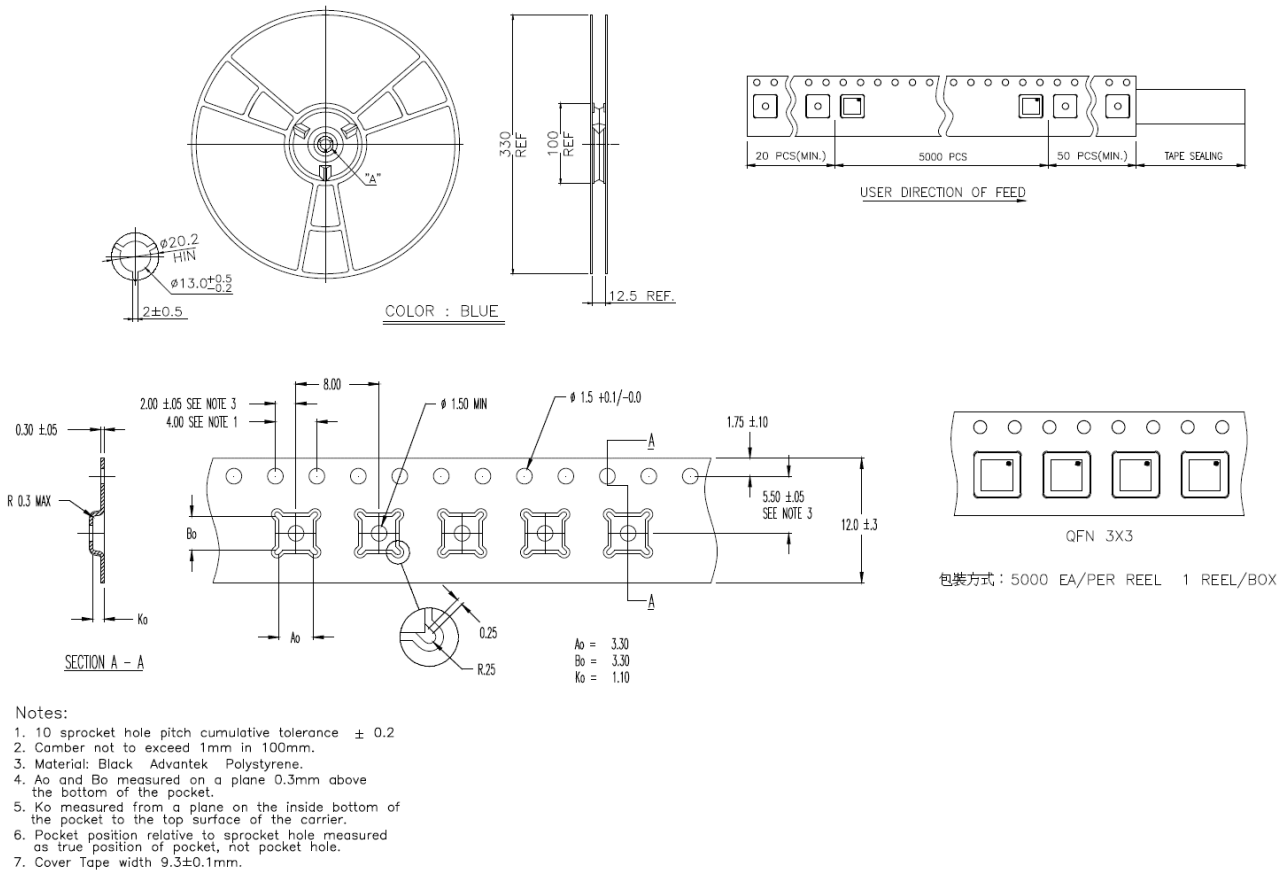


Figure 5: DFN10 Package Outline Drawing

5.2 Tape and Reel Information



Notes:
1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. Cover Tape width 9.3±0.1mm.

Figure 6: Tape and Reel Information

5.3 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

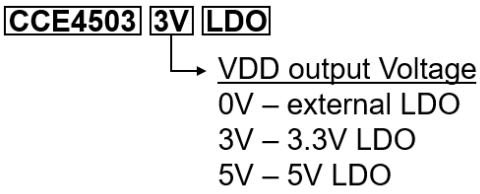
6. Ordering Information

The ordering number consists of the part number followed by a suffix (shown as "xx") indicating the LDO option. For details and availability, please consult your Renesas Electronics local sales representative.

Table 3: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
CCE4503 xx LDO	DFN10	3 x 3	T&R	4000

Part Number Legend:



7. Application Information

The CCE4503 may need to be connected to some external components depending on the desired operating environment:

- If an LDO is selected (5V or 3.3V), a 1 µF capacitor from VDD to L- must be provided by the customer
- Outputs NERR and NWUP are open-drain outputs. Usually, the internal pull-up resistors of the MCU can be used. If no pull-up resistors can be configured, the customer needs to connect external resistors.
- A resistor RLIM may be used to set the overcurrent limit and slew rate. For maximum slew rate and overcurrent limit, the pin can be connected to VSS or left open.

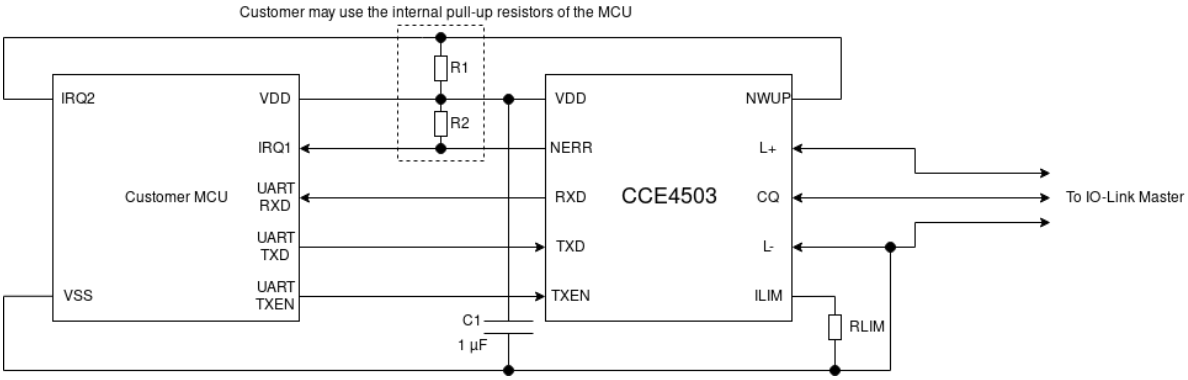


Figure 7: CCE4503 application

8. Revision History

Revision	Date	Description
2.8	04-Jan-2024	Moved Operating Temperature from Absolute Maximum Ratings to Recommended Operating Conditions Moved Junction Temperature from Absolute Maximum Ratings to Recommended Operating Conditions
2.7	15-Dez-2023	Added information about RXD in Output Stage Updated Voltage at pin CQ in Recommended Operating Conditions Updated Wake-up detection time T_{WAKE} in Input / Output CQ Changed specification for V_{OUT_L}, V_{OUT_H}, V_{IN_L}, V_{IN_H}, I_{PU} in Digital I/O Removed inductive load from Input / Output CQ Removed voltage limitation from condition of LDO output current in Recommended Operating Conditions Changed Tape and Reel Information (change of pin 1 location)
2.6	09-May-2023	Corrected part naming Updated Absolut Maximum Ratings Updated ESD Ratings
2.5	25-Jan-2023	Corrected formatting of document Added Chapter ESD Ratings
2.4	06-Dec-2022	Updated to Renesas Added Tape and Reel Information
2.3	23-Jul-2020	Changed Ordering Information
2.2	27-May-2020	Corrected Electrical Characteristics
2.1	26-May-2020	Corrected Electrical Characteristics Added Errata sheet note
2.0	20-Feb-2020	Initial version. Preliminary

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