



# Contents

Description	1
PCIe Clocking Architectures	1
Typical Applications	1
Output Features	1
Features	1
Key Specifications	1
Block Diagram	1
Pin Configuration	3
Power Management	3
PLL Operating Mode	3
Power Connections (for pin compatibility with 9ZML12xxB)	3
Power Connections	3
Skew Programming	3
Pin Descriptions	4
Absolute Maximum Ratings	6
Electrical Characteristics	6
DIF_IN Clock Input Parameters	6
SMBus	6
Input/Supply/Common Parameters	7
DIF HCSL/LP-HCSL Outputs	8
Current Consumption	8
Skew and Differential Jitter Parameters	9
Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures	10
Filtered Phase Jitter Parameters - PCIe Separate Reference Independent Spread (SRIS) Architectures	11
Filtered Phase Jitter Parameters - QPI/UPI	11
Unfiltered Phase Jitter Parameters - 12kHz to 20MHz	12
Clock Periods—Differential Outputs with Spread Spectrum Disabled	12
Clock Periods—Differential Outputs with Spread Spectrum Enabled	12
Test Loads	12
Alternate Terminations	12
General SMBus Serial Interface Information	13
Package Outline Drawings	16
Ordering Information	16
Marking Diagrams	16
Revision History	17

	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	
VDDA	1																		54 ^OE7#
GND A	2																		53 ^OE6#
^SEL_A_B#	3																		52 VDDIO
vHIBW_BYPM_LOBW#	4																		51 GND
CKPWRGD_PD#	5																		50 DIF_7#
DIF_INB	6																		49 DIF_7
DIF_INB#	7																		48 DIF_6#
GND	8																		47 DIF_6
VDDR	9																		46 GND
DIF_INA	10																		45 VDD
DIF_INA#	11																		44 DIF_5#
vSADR0_tri	12																		43 DIF_5
SMBDAT	13																		42 DIF_4#
SMBCLK	14																		41 DIF_4
vSADR1_tri	15																		40 VDDIO
NC	16																		39 GND
FBOUT_NC#	17																		38 ^OE5#
FBOUT_NC	18																		37 ^OE4#
	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	
	^OE0#	^OE1#	NC	GND	DIF_0	DIF_0#	DIF_1	DIF_1#	GND	VDD	DIF_2	DIF_2#	DIF_3	DIF_3#	NC	GND	^OE2#	^OE3#	

## Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDA	PWR	Power supply for PLL core.
2	GNDA	GND	Ground pin for the PLL core.
3	^SEL_A_B#	IN	Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor. 0 = Input B selected, 1 = Input A selected.
4	^vHIBW_BYPM_LOBW#	LATCHED IN	Tri-level input to select High BW, Bypass or Low BW mode. This pin is biased to VDD/2 (Bypass mode) with internal pull up/pull down resistors. See PLL Operating Mode Table for Details.
5	CKPWRGD_PD#	IN	3.3V input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
6	DIF_INB	IN	True input of differential clock
7	DIF_INB#	IN	Complement input of differential clock
8	GND	GND	Ground pin.
9	VDDR	PWR	Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
10	DIF_INA	IN	True input of differential clock
11	DIF_INA#	IN	Complement input of differential clock
12	vSADR0_tri	IN	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal pull down resistor. See the SMBus Address Selection Table.
13	SMBDAT	I/O	Data pin of SMBUS circuitry
14	SMBCLK	IN	Clock pin of SMBUS circuitry
15	vSADR1_tri	IN	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal pull down resistor. See the SMBus Address Selection Table.
16	NC	N/A	No connection.
17	FBOUT_NC#	OUT	Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
18	FBOUT_NC	OUT	True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
19	^OE0#	IN	Active low input for enabling output 0. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
20	^OE1#	IN	Active low input for enabling output 1. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
21	NC	N/A	No connection.
22	GND	GND	Ground pin.
23	DIF_0	OUT	HCSL true clock output.
24	DIF_0#	OUT	HCSL complementary clock output.
25	DIF_1	OUT	HCSL true clock output.
26	DIF_1#	OUT	HCSL complementary clock output.
27	GND	GND	Ground pin.
28	VDD	PWR	Power supply, nominally 3.3V.
29	DIF_2	OUT	HCSL true clock output.
30	DIF_2#	OUT	HCSL complementary clock output.
31	DIF_3	OUT	HCSL true clock output.
32	DIF_3#	OUT	HCSL complementary clock output.
33	NC	N/A	No connection.
34	GND	GND	Ground pin.
35	^OE2#	IN	Active low input for enabling output 2. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
36	^OE3#	IN	Active low input for enabling output 3. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
37	^OE4#	IN	Active low input for enabling output 4. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
38	^OE5#	IN	Active low input for enabling output 5. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
39	GND	GND	Ground pin.
40	VDDIO	PWR	Power supply for differential outputs.
41	DIF_4	OUT	HCSL true clock output.
42	DIF_4#	OUT	HCSL complementary clock output.
43	DIF_5	OUT	HCSL true clock output.
44	DIF_5#	OUT	HCSL complementary clock output.
45	VDD	PWR	Power supply, nominally 3.3V.
46	GND	GND	Ground pin.
47	DIF_6	OUT	HCSL true clock output.
48	DIF_6#	OUT	HCSL complementary clock output.
49	DIF_7	OUT	HCSL true clock output.
50	DIF_7#	OUT	HCSL complementary clock output.
51	GND	GND	Ground pin.
52	VDDIO	PWR	Power supply for differential outputs.
53	^OE6#	IN	Active low input for enabling output 6. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
54	^OE7#	IN	Active low input for enabling output 7. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
55	^OE8#	IN	Active low input for enabling output 8. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
56	^OE9#	IN	Active low input for enabling output 9. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
57	NC	N/A	No connection.
58	GND	GND	Ground pin.
59	DIF_8	OUT	HCSL true clock output.
60	DIF_8#	OUT	HCSL complementary clock output.
61	DIF_9	OUT	HCSL true clock output.
62	DIF_9#	OUT	HCSL complementary clock output.
63	GND	GND	Ground pin.
64	VDD	PWR	Power supply, nominally 3.3V.
65	DIF_10	OUT	HCSL true clock output.
66	DIF_10#	OUT	HCSL complementary clock output.
67	DIF_11	OUT	HCSL true clock output.
68	DIF_11#	OUT	HCSL complementary clock output.
69	NC	N/A	No connection.
70	GND	GND	Ground pin.
71	^OE10#	IN	Active low input for enabling output 10. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
72	^OE11#	IN	Active low input for enabling output 11. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
73	epad	GND	Connect to ground

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZML1232E/9ZML1252E. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx				3.9	V	1,2
Input Low Voltage	V <sub>IL</sub>		GND-0.5			V	1
Input High Voltage	V <sub>IH</sub>	Except for SMBus interface			V <sub>DD</sub> +0.5	V	1,3
Input High Voltage	V <sub>IHSMB</sub>	SMBus clock and data pins			3.9	V	1
Storage Temperature	T <sub>s</sub>		-65		150	°C	1
Junction Temperature	T <sub>j</sub>				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

<sup>3</sup>Not to exceed 3.9V.

## Electrical Characteristics

### DIF\_IN Clock Input Parameters

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Crossover Voltage	V <sub>CROSS</sub>	Cross Over Voltage	150		900	mV	1
Input Swing - DIF_IN	V <sub>SWING</sub>	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.35		8	V/ns	1,2
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND	-5		5	uA	
Input Duty Cycle	d <sub>tin</sub>	Measurement from differential waveform	45		55	%	1
Input Jitter - Cycle to Cycle	J <sub>DIFIN</sub>	Differential Measurement	0		125	ps	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Slew rate measured through +/-75mV window centered around differential zero

### SMBus

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SMBus Input Low Voltage	V <sub>ILSMB</sub>				0.8	V	
SMBus Input High Voltage	V <sub>IHSMB</sub>		2.1		V <sub>DDSMB</sub>	V	
SMBus Output Low Voltage	V <sub>OLSMB</sub>	@ I <sub>PULLUP</sub>			0.4	V	
SMBus Sink Current	I <sub>PULLUP</sub>	@ V <sub>OL</sub>	4			mA	
Nominal Bus Voltage	V <sub>DDSMB</sub>		2.7		3.6	V	1
SCLK/SDATA Rise Time	t <sub>RSMB</sub>	(Max V <sub>IL</sub> - 0.15) to (Min V <sub>IH</sub> + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t <sub>FSMB</sub>	(Min V <sub>IH</sub> + 0.15) to (Max V <sub>IL</sub> - 0.15)			300	ns	1
SMBus Operating Frequency	f <sub>MAXSMB</sub>	Maximum SMBus operating frequency			400	kHz	5

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup>DIF\_IN input

<sup>5</sup>The differential input clock must be running for the SMBus to be active

# Input/Supply/Common Parameters

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx	Supply voltage for core and analog	3.135	3.3	3.465	V	
	VDDIO	Supply voltage for differential outputs	3.135	3.3	3.465	V	
Ambient Operating Temperature	T <sub>AMB</sub>	Industrial range	-40		85	°C	
Input High Voltage	V <sub>IH</sub>	Single-ended inputs, except SMBus, tri-level inputs	2		V <sub>DD</sub> + 0.3	V	
Input Low Voltage	V <sub>IL</sub>	Single-ended inputs, except SMBus, tri-level inputs	GND - 0.3		0.8	V	
Input High Voltage	V <sub>IH</sub>	Tri-Level Inputs (_tri suffix)	2.2		V <sub>DD</sub> + 0.3	V	
Input Mid Voltage	V <sub>IL</sub>	Tri-Level Inputs (_tri suffix)	1.2	VDD/2	1.8	V	
Input Low Voltage	V <sub>IL</sub>	Tri-Level Inputs (_tri suffix)	GND - 0.3		0.8	V	
Input Current	I <sub>IN</sub>	Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD	-5		5	uA	
	I <sub>INP</sub>	Single-ended inputs V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors V <sub>IN</sub> = VDD; Inputs with internal pull-down resistors	-100		100	uA	
Input Frequency	F <sub>ibyp</sub>	V <sub>DD</sub> = 3.3 V, Bypass mode	1		400	MHz	
	F <sub>ipll</sub>	V <sub>DD</sub> = 3.3 V, 100MHz PLL mode	98.5	100.00	102	MHz	5
Pin Inductance	L <sub>pin</sub>				7	nH	1
Capacitance	C <sub>IN</sub>	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C <sub>INDIF_IN</sub>	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C <sub>OUT</sub>	Output pin capacitance			6	pF	1
Clk Stabilization	T <sub>STAB</sub>	From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		1.2	1.8	ms	1,2
Input SS Modulation Frequency PCIe	f <sub>MODINPCIe</sub>	Allowable Frequency for PCIe Applications (Triangular Modulation)	30	31.6	33	kHz	
OE# Latency	t <sub>LATOE#</sub>	DIF start after OE# assertion DIF stop after OE# deassertion	4	5	10	clocks	1,2,3
Tdrive_PD#	t <sub>DRVPD</sub>	DIF output enable after PD# de-assertion		85	300	us	1,3
Tfall	t <sub>F</sub>	Fall time of control inputs			5	ns	2
Trise	t <sub>R</sub>	Rise time of control inputs			5	ns	2

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV, PLL mode.

<sup>4</sup>DIF\_IN input

<sup>5</sup> This parameter reflects the operating range after locking to a 100MHz input.

## DIF HCSL/LP-HCSL Outputs

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on	2.0	2.8	4.0	0.6 - 4.0	V/ns	1,2,3
Slew rate matching	$\Delta dV/dt$	Slew rate matching, Scope averaging on		4	15	20	%	1,2,4,7
Max Voltage	V <sub>max</sub>	Measurement on single ended signal using absolute value. (Scope averaging off)	660	794	870	1150	mV	7,8
Min Voltage	V <sub>min</sub>		-111	-49		-300		7,8
Crossing Voltage (abs)	V <sub>cross_abs</sub>	Scope averaging off	302	367	453	250 - 550	mV	1,5,7
Crossing Voltage (var)	$\Delta V_{cross}$	Scope averaging off		32	74	140	mV	1,6,7

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Slew rate is measured through the V<sub>swing</sub> voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

<sup>5</sup> V<sub>cross</sub> is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all V<sub>cross</sub> measurements in any particular system. Note that this is a subset of V<sub>cross\_min/max</sub> (V<sub>cross</sub> absolute) allowed. The intent is to limit V<sub>cross</sub> induced modulation by setting  $\Delta V_{cross}$  to be smaller than V<sub>cross</sub> absolute.

<sup>7</sup> At default SMBus settings.

<sup>8</sup> If driving a receiver with input terminations, the V<sub>max</sub> and V<sub>min</sub> values will be halved.

## Current Consumption

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I <sub>DDx</sub>	All other VDD pins, All outputs @100MHz, CL = 2pF; Z <sub>o</sub> =85Ω		22	30	mA	2
	I <sub>DDA+R</sub>	VDDA+VDDR pins, All outputs @100MHz, CL = 2pF; Z <sub>o</sub> =85Ω		56	65	mA	1,2
	I <sub>DDO</sub>	VDDIO pins, All outputs @100MHz, CL = 2pF; Z <sub>o</sub> =85Ω		84	100	mA	2
Powerdown Current	I <sub>DDx</sub>	All other VDD pins, all outputs Low/Low		0.9	2	mA	1,2
	I <sub>DDA+R</sub>	VDDA+VDDR pins, all outputs Low/Low		4.3	6	mA	1,2
	I <sub>DDO</sub>	VDDIO pins, all outputs Low/Low		0.1	0.2	mA	1,2

<sup>1</sup>. Includes VDDR if applicable



# Skew and Differential Jitter Parameters

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
CLK_IN, DIF[x:0]	$t_{\text{SKEW\_PLL}}$	Input-to-Output Skew in PLL mode @100MHz, nominal temperature and voltage	-100	-4	100	ps	1,2,4,5,6,8
CLK_IN, DIF[x:0]	$t_{\text{PD\_BYP}}$	Input-to-Output Skew in Bypass mode @100MHz, nominal temperature and voltage	2.2	2.9	3.6	ns	1,2,3,8
CLK_IN, DIF[x:0]	$t_{\text{DSPO\_PLL}}$	Input-to-Output Skew Variation in PLL mode @100MHz, across voltage and temperature	-50	0.0	50	ps	1,2,3,8
CLK_IN, DIF[x:0]	$t_{\text{DSPO\_BYP}}$	Input-to-Output Skew Variation in Bypass mode @100MHz, across voltage and temperature, $T_{\text{AMB}} = 0\text{C to } 70\text{C}$ , default slew rate	-250	0.0	250	ps	1,2,3,8
		Input-to-Output Skew Variation in Bypass mode @100MHz, across voltage and temperature, $T_{\text{AMB}} = -40\text{C to } 85\text{C}$ , default slew rate	-350	0.0	350	ps	1,2,3,8
DIF[x:0]	$t_{\text{SKEW\_ALL}}$	Output-to-Output Skew across all outputs, common to PLL and Bypass mode, @100MHz, default slew rate		30	50	ps	1,2,3,8
PLL Jitter Peaking	$j_{\text{peak-hibw}}$	LOBW#_BYPASS_HIBW = 1	0	1.3	2.5	dB	7,8
PLL Jitter Peaking	$j_{\text{peak-lobw}}$	LOBW#_BYPASS_HIBW = 0	0	1.3	2	dB	7,8
PLL Bandwidth	$\text{pll}_{\text{HIBW}}$	LOBW#_BYPASS_HIBW = 1	2	2.6	4	MHz	8,9
PLL Bandwidth	$\text{pll}_{\text{LOBW}}$	LOBW#_BYPASS_HIBW = 0	0.7	1.0	1.4	MHz	8,9
Duty Cycle	$t_{\text{DC}}$	Measured differentially, PLL Mode	45	50	55	%	1
Duty Cycle Distortion	$t_{\text{DCD}}$	Measured differentially, Bypass Mode @100MHz	-1	-0.2	0	%	1,10
Jitter, Cycle to cycle	$t_{\text{jcy-cyc}}$	PLL mode		13	50	ps	1,11
		Additive Jitter in Bypass Mode		0.2	5	ps	1,11

<sup>1</sup> Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

<sup>2</sup> Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

<sup>3</sup> All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

<sup>4</sup> This parameter is deterministic for a given device

<sup>5</sup> Measured with scope averaging on to find mean value.

<sup>6</sup> This value is programmable, see I2O Programming Table.

<sup>7</sup> Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

<sup>8</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>9</sup> Measured at 3 db down or half power point.

<sup>10</sup> Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

<sup>11</sup> Measured from differential waveform.

# Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCleG1-CC}$	PCIe Gen 1		13	30	86	ps (p-p)	1,2,3
	$t_{jphPCleG2-CC}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.3	0.7	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		1.0	1.6	3.1	ps (rms)	1,2
	$t_{jphPCleG3-CC}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.24	0.35	1	ps (rms)	1,2
	$t_{jphPCleG4-CC}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.24	0.30	0.5	ps (rms)	1,2
Additive Phase Jitter, Bypass mode	$t_{jphPCleG1-CC}$	PCIe Gen 1		0.01	0.05	n/a	ps (p-p)	1,2
	$t_{jphPCleG2-CC}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.01	0.05		ps (rms)	1,2,4
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.000	0.05		ps (rms)	1,2,4
	$t_{jphPCleG3-CC}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.01	0.05		ps (rms)	1,2,4
	$t_{jphPCleG4-CC}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.01	0.05		ps (rms)	1,2,4

<sup>1</sup> Applies to all outputs, when driven by 9SQL4958 or equivalent.

<sup>2</sup> Based on PCIe Base Specification Rev 7.0 version. See <http://www.pcisig.com> for latest specifications.

<sup>3</sup> Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of  $1^{-12}$ .

<sup>4</sup> For RMS values additive jitter is calculated by solving the following equation for b [ $a^2 + b^2 = c^2$ ] where "a" is rms input jitter and "c" is rms total jitter.

## Filtered Phase Jitter Parameters - PCIe Separate Reference Independent Spread (SRIS) Architectures

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	t <sub>jphPCleG1-SRIS</sub>	PCIe Gen 1	n/a			n/a	ps (p-p)	1,2,3
	t <sub>jphPCleG2-SRIS</sub>	PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz)		0.8	1.2	2	ps (rms)	1,2
	t <sub>jphPCleG3-SRIS</sub>	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.6	0.68	0.7	ps (rms)	1,2
	t <sub>jphPCleG4-SRIS</sub>	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)	n/a			n/a	ps (rms)	1,2
Additive Phase Jitter, Bypass mode	t <sub>jphPCleG1-SRIS</sub>	PCIe Gen 1	n/a			n/a	ps (p-p)	1,2,5
	t <sub>jphPCleG2-SRIS</sub>	PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz)		0.0	0.02		ps (rms)	1,2,4
	t <sub>jphPCleG3-SRIS</sub>	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.0	0.02		ps (rms)	1,2,4
	t <sub>jphPCleG4-SRIS</sub>	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)	n/a				ps (rms)	1,2,4,5

<sup>1</sup> Applies to all outputs, when driven by 9SQL4958 or equivalent

<sup>2</sup> Based on PCIe Base Specification Rev 7.0. These filters are different than Common Clock filters. See <http://www.pcisig.com> for latest specifications. 0.7ps is the Intel specified limit, which may differ from the PCI SIG limit.

<sup>3</sup> Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of  $10^{-12}$ .

<sup>4</sup> For RMS values, additive jitter is calculated by solving the following equation for b [ $a^2 + b^2 = c^2$ ] where "a" is rms input jitter and "c" is rms total jitter.

<sup>5</sup> SRIS is not currently defined for PCIe Gen1 and Gen4.

## Filtered Phase Jitter Parameters - QPI/UPI

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	IND.LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphQPI\_UPI}$	QPI & SMI (100MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.15	0.3	0.5	ps (rms)	1,2
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.08	0.1	0.3	ps (rms)	1,2
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.07	0.1	0.2	ps (rms)	1,2
Additive Phase Jitter, Bypass mode	$t_{jphQPI\_UPI}$	QPI & SMI (100MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.00	0.05	n/a	ps (rms)	1,2,3
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.02	0.09		ps (rms)	1,2,3
		QPI & SMI (100MHz, ? 9.6Gb/s, 12UI)		0.02	0.08		ps (rms)	1,2,3

<sup>1</sup> Applies to all outputs, when driven by 9SQL4958 or equivalent

<sup>2</sup> Calculated from Intel-supplied Clock Jitter Tool

<sup>3</sup> For RMS values additive jitter is calculated by solving the following equation for b [ $a^2 + b^2 = c^2$ ] where "a" is rms input jitter and "c" is rms total jitter.

## Unfiltered Phase Jitter Parameters - 12kHz to 20MHz

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	IND.LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jph12k-20MHi}$	PLL High BW, SSC OFF, 100MHz		171	250	n/a	fs (rms)	1,2
Phase Jitter, PLL Mode	$t_{jph12k-20MLo}$	PLL Low BW, SSC OFF, 100MHz		183	250	n/a	fs (rms)	1,2
Additive Phase Jitter, Bypass mode	$t_{jph12k-20MByp}$	Bypass Mode, SSC OFF, 100MHz		109	150	n/a	fs (rms)	1,2,3

<sup>1</sup> Applies to all outputs. Wenzel clock source.

<sup>2</sup> 12kHz to 20MHz brick wall filter.

<sup>3</sup> For RMS values additive jitter is calculated by solving the following equation for b [ $a^2 + b^2 = c^2$ ] where "a" is rms input jitter and "c" is rms total jitter.

## Clock Periods–Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2,3

## Clock Periods–Differential Outputs with Spread Spectrum Enabled

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2,3

Notes:

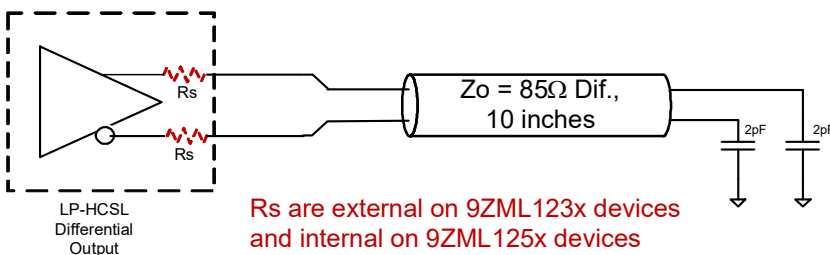
<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ accuracy requirements (+/-100ppm). The 9ZML12xx does not contribute to ppm error.

<sup>3</sup> Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode

## Test Loads

9ZML Differential Test Loads



Differential Output Terminations\*

Device	DIF Zo (Ω)	Rs (Ω)
9ZML123x	85	27
9ZML123x	100	33
9ZML125x	85	Internal
9ZML125x	100	7.5

\*Contact factory for versions of this device with Zo=100Ω

## Alternate Terminations

The output can easily drive other logic families. See “AN-891 Driving LVPECL, LVDS, CML, and SSTL Logic with Universal Low-Power HCSL Outputs” for LVPECL, LVDS, CML, and SSTL.

# General SMBus Serial Interface Information

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation				
Controller (Host)			Renesas (Slave/Receiver)	
T	starT bit			
Slave Address				
WR	WRite			
			ACK	
Beginning Byte = N				
			ACK	
Data Byte Count = X				
			ACK	
Beginning Byte N			X Byte	
		ACK		
O				
O		O		
O		O		
		O		
Byte N + X - 1				
			ACK	
P	stoP bit			

## 9ZML1232E/9ZML1252E SMBus Addressing

SMB_A(1:0) tri	SMBus Address (Rd/Wrt bit = 0)
00	D8
0M	DA
01	DE
M0	C2
MM	C4
M1	C6
10	CA
1M	CC
11	CE

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte N+X-1
- Renesas clock sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			Renesas
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
			Beginning Byte N
ACK			
		0	
0		0	
0		0	
0			
		Byte N + X - 1	
N	Not acknowledge		
P	stoP bit		

**SMBusTable: PLL Mode, and Frequency Select Register**

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		PLL Mode bit [1]	PLL Operating Mode Rd back 1	R	See PLL Operating Mode Readback Table		Latch
Bit 6		PLL Mode bit [0]	PLL Operating Mode Rd back 0	R			Latch
Bit 5		SEL_A_B#	Input Select Readback	R	DIF_INB	DIF_INA	Pin
Bit 4		Reserved					0
Bit 3		PLL_InSEL_SW_EN	Enable S/W control of PLL BW and Input select	RW	Pin Control	SMBus Control	0
Bit 2		PLL Mode bit [1]	PLL Operating Mode 1	RW	See PLL Operating Mode Readback Table <sup>1</sup>		1
Bit 1		PLL Mode bit [0]	PLL Operating Mode 1	RW			1
Bit 0		SEL_A_B#	Input Select Status or Control	RW	DIF_INB	DIF_INA	1

Note: Setting bit 3 to '1' allows the user to override the latch value from pin 5 via use of bits 2 and 1. The system may require a warm system reset if the user changes these bits. The clock itself does not require a reset. Setting bit 3 to a '1' also allows the user to use bit 0 to control the input select.

**SMBusTable: Output Disable Register**

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		DIF_7_En	Output Control overrides OE# pin	RW	Low/Low	Pin Control	1
Bit 6		DIF_6_En	Output Control overrides OE# pin	RW			1
Bit 5		DIF_5_En	Output Control overrides OE# pin	RW			1
Bit 4		DIF_4_En	Output Control overrides OE# pin	RW			1
Bit 3		DIF_3_En	Output Control overrides OE# pin	RW			1
Bit 2		DIF_2_En	Output Control overrides OE# pin	RW			1
Bit 1		DIF_1_En	Output Control overrides OE# pin	RW			1
Bit 0		DIF_0_En	Output Control overrides OE# pin	RW			1

**SMBusTable: Output Disable Register**

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		DIF_11_En	Output Control overrides OE# pin	RW	Low/Low	Pin Control	1
Bit 2		DIF_10_En	Output Control overrides OE# pin	RW			1
Bit 1		DIF_9_En	Output Control overrides OE# pin	RW			1
Bit 0		DIF_8_En	Output Control overrides OE# pin	RW			1

**SMBusTable: Reserved Register**

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

**SMBusTable: Reserved Register**

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

**SMBusTable: Vendor & Revision ID Register**

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	E rev = 0100		0
Bit 6	-	RID2		R			1
Bit 5	-	RID1		R			0
Bit 4	-	RID0		R			0
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

**SMBusTable: DEVICE ID**

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Device ID 7 (MSB)		R	9ZML1232=EC 9ZML1233=ED 9ZML1252=FC 9ZML1253=FD		1
Bit 6	-	Device ID 6		R			1
Bit 5	-	Device ID 5		R			1
Bit 4	-	Device ID 4		R			X
Bit 3	-	Device ID 3		R			1
Bit 2	-	Device ID 2		R			1
Bit 1	-	Device ID 1		R			0
Bit 0	-	Device ID 0		R			X

**SMBusTable: Byte Count Register**

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4	-	BC4	Writing to this register configures how many bytes will be read back.	RW	Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default.		0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			0

**SMBusTable:Output Skew RegisterA (when Input Clock A is selected)**

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		I2O_FB_ASkew2	Channel A Output delay programming (early)		Binary value of number of VCO periods that outputs will be pulled earlier than input.		0
Bit 1		I2O_FB_ASkew1		RW			0
Bit 0		I2O_FB_ASkew0		RW			0

Note: For example, at 2.4GHz, each VCO period is 416.7ps and there are 24 VCO periods in a 100MHz output. Each write to bits [2:0] will pull the output a early by that number of VCO periods. Writing '110' 4 times would pull the output back in phase with the input. Writing '001' twice will accomplish the same result as writing '010' once - pulling the output 2 VCO periods earlier.

**SMBusTable:Output Skew RegisterA (when Input Clock B is selected)**

Byte 9	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		I2O_FB_BSkew2	Channel B Output delay programming (early)	RW	Binary value of number of VCO periods that outputs will be pulled earlier than input. Default is 0.		0
Bit 1		I2O_FB_BSkew1		RW			0
Bit 0		I2O_FB_BSkew0		RW			0

Note: For example, at 2.4GHz, each VCO period is 416.7ps and there are 24 VCO periods in a 100MHz output. Each write to bits [2:0] will pull the output a early by that number of VCO periods. Writing '110' 4 times would pull the output back in phase with the input. Writing '001' twice will accomplish the same result as writing '010' once - pulling the output 2 VCO periods earlier.

## Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

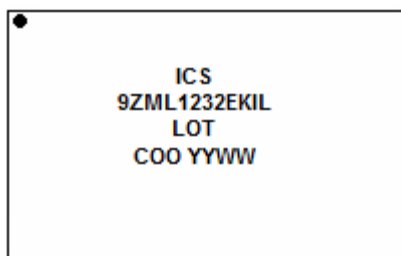
## Ordering Information

Part Number	Package	Carrier Type	Temperature Range
9ZML1232EKILF	10.0 × 10.0 × 0.90 mm, <a href="#">72-VFQFPN</a>	Tray	-40° to +85°C
9ZML1232EKILFT		Tape and Reel	-40° to +85°C
9ZML1252EKILF		Tray	-40° to +85°C
9ZML1252EKILFT		Tape and Reel	-40° to +85°C

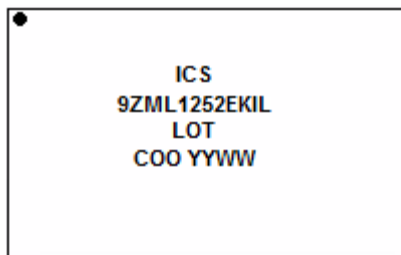
“LF” designates PB-free configuration, RoHS compliant.

“E” is the device revision designator (will not correlate with the datasheet revision).

## Marking Diagrams



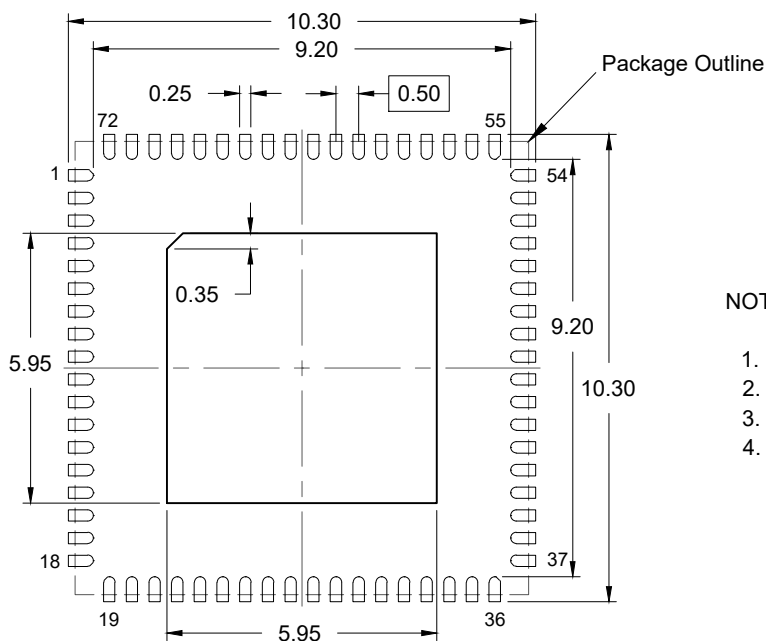
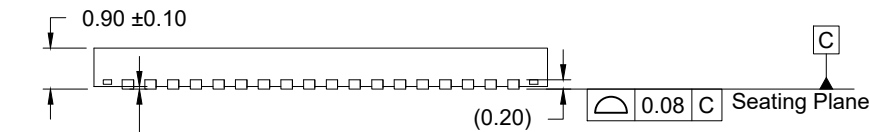
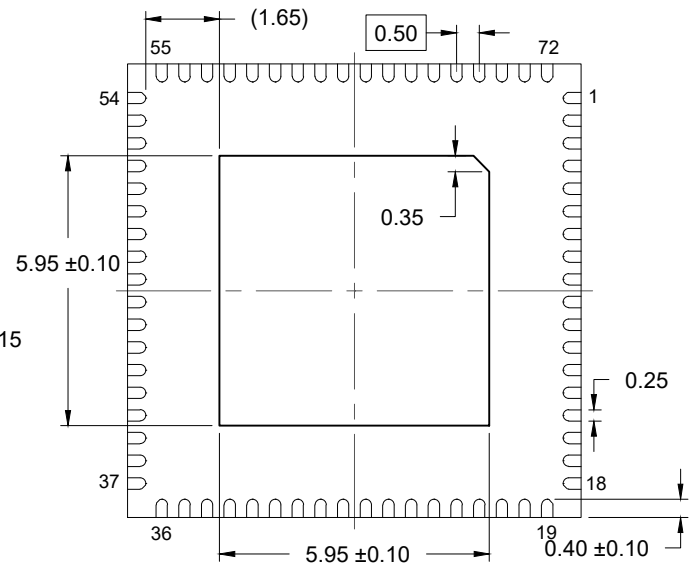
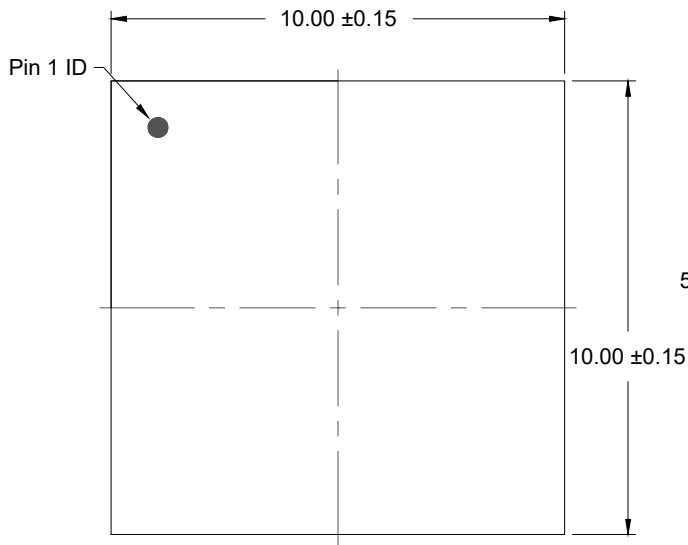
- Line 2: part number.
- Line 3: “LOT” denotes the lot number.
- Line 4: “COO” denotes country of origin; “YYWW” denotes the last two digits of the year and work week the part was assembled.





## Revision History

Revision Date	Description of Change
December 4, 2025	Added <a href="#">Alternate Terminations</a> section.
May 12, 2021	Updates to Byte 0, bit 0 and bit 5 defaults.
May 3, 2021	<ul style="list-style-type: none"> <li>▪ Added missing Byte 0, bit 0. Updated Byte 0 footnote.</li> <li>▪ Updated Package Outline Drawings section.</li> <li>▪ Updated Marking Diagrams section.</li> <li>▪ Updated Ordering Information table.</li> </ul>
April 19, 2017	<ul style="list-style-type: none"> <li>▪ Update Features and Key Specifications.</li> <li>▪ Updated PCIe Common Clocked, PCIe Separate Clocked, and QPI/UPI to latest format, added IF-UPI spec to QPI/UPI tables.</li> <li>▪ Updated Test Loads drawing to latest version.</li> </ul>
April 17, 2017	<ul style="list-style-type: none"> <li>▪ Reverted back to original Device ID Scheme, byte 6 updated accordingly: <ul style="list-style-type: none"> <li>• 9ZML1232 = EC</li> <li>• 9ZML1252 = FC</li> </ul> </li> </ul>
January 31, 2017	<ul style="list-style-type: none"> <li>▪ Finalized electrical tables.</li> <li>▪ Removed Byte 0, bit 0 from SMBus - only Hardware can select A or B input.</li> <li>▪ Added notes about functionality of Byte 0 [2:1].</li> <li>▪ Move to final.</li> </ul>



NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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