## Description

The 9QXL2001B is a 20-output very-low-additive phase jitter fanout buffer for PCIe Gen4, Gen5 and UPI applications. The 9QXL2001B provides two methods to control output enables; standard OE# pins and SMBus enable bits, or a simple 3-wire serial interface that is independent of the SMBus. The OE Control Mode is set via a hardware strap. It offers integrated terminations for 85Ω transmission lines.

## PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

## Typical Applications

- Servers, Storage, Networking, Accelerators

## Key Specifications

- Output-to-output skew: < 50ps
- Additive phase jitter: DB2000Q < 25fs rms
- Additive phase jitter: PCIe Gen4 < 40fs rms
- Additive phase jitter: PCIe Gen5 < 20fs rms

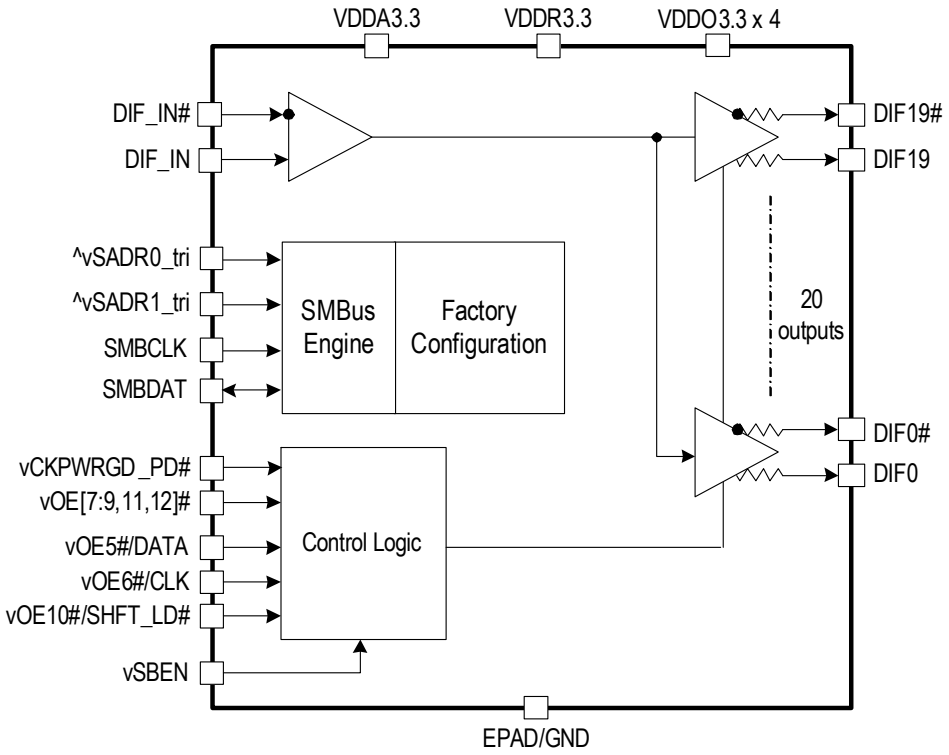
## Features

- Two Output Enable Control modes:
  - Traditional 8 OE# pins allow hardware control of 8 outputs and 20 SMBus bits allow software control of each output
  - Simple 3-wire Side-Band Interface allows real-time control of all 20 outputs
- Outputs remain Low/Low when powered up with floating input clock
- Low-Power HCSL (LP-HCSL) outputs:
  - Zo = 85Ω outputs eliminate 80 resistors, saving 130mm$^2$ of area
  - Power consumption reduced by 50%
- 9 selectable SMBus addresses
- Spread spectrum compatible
- 6 × 6 mm dual-row 80-GQFN

## Output Features

20 Low-Power HCSL (LP-HCSL) 85Ω output pairs

## Block Diagram



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# Pin Assignments

**Figure 1. Pin Assignments for 6 × 6 mm 80-GQFN Package – Top View**

Note: Pins with ^ prefix have internal pull-up resistor.
Pins with v prefix have internal pull-down resistor.
Pins with ^v prefix have internal pull-up/pull-down resistor network biasing input to VDD/2.

# Pin Descriptions

**Table 1. Pin Descriptions**

| Number | | Name | Type | Description |
|---|---|---|---|---|
| A | 1 | DIF17 | Output | Differential true clock output. |
| A | 2 | DIF16# | Output | Differential complementary clock output. |
| A | 3 | DIF16 | Output | Differential true clock output. |
| A | 4 | DIF15# | Output | Differential complementary clock output. |
| A | 5 | DIF15 | Output | Differential true clock output. |
| A | 6 | DIF14# | Output | Differential complementary clock output. |
| A | 7 | DIF14 | Output | Differential true clock output. |
| A | 8 | DIF13# | Output | Differential complementary clock output. |
| A | 9 | DIF13 | Output | Differential true clock output. |
| A | 10 | DIF12# | Output | Differential complementary clock output. |
| A | 11 | DIF12 | Output | Differential true clock output. |
| A | 12 | DIF11# | Output | Differential complementary clock output. |
| B | 1 | DIF17# | Output | Differential complementary clock output. |
| B | 2 | VDDO3.3 | Power | Power supply for outputs. Nominally 3.3V. |
| B | 3 | NC | — | No connection. |
| B | 4 | ^vSADR0_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus addresses. It has internal pull-up/down resistors to bias to $V_{DD}/2$. See the SMBus Address Selection table. |
| B | 5 | NC | — | No connection. |
| B | 6 | VDDA3.3 | Power | 3.3V power for the PLL core. |
| B | 7 | NC | — | No connection. |
| B | 8 | ^vSADR1_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus addresses. It has internal pull-up/down resistors to bias to VDD/2. See the SMBus Address Selection table. |
| B | 9 | NC | — | No connection. |
| B | 10 | vOE12# | Input | Active low input for enabling output 12. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| B | 11 | VDDO3.3 | Power | Power supply for outputs. Nominally 3.3V. |
| B | 12 | DIF11 | Output | Differential true clock output. |
| C | 1 | DIF18 | Output | Differential true clock output. |
| C | 2 | NC | — | No connection. |
| C | 11 | vOE11# | Input | Active low input for enabling output 11. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| C | 12 | DIF10# | Output | Differential complementary clock output. |
| D | 1 | DIF18# | Output | Differential complementary clock output. |
| D | 2 | NC | — | No connection. |

**Table 1. Pin Descriptions (Cont.)**

| Number | | Name | Type | Description |
|---|---|---|---|---|
| D | 11 | NC | — | No connection. |
| D | 12 | DIF10 | Output | Differential true clock output. |
| E | 1 | DIF19 | Output | Differential true clock output. |
| E | 2 | vSBEN | Input | Input that enables the Side-Band Interface for controlling output enables. This pin disables the output enable pins when asserted. It has an internal pull-down resistor.<br>0 = OE pins and SMBus enable bits control outputs, Side-band interface disabled.<br>1 = Side-Band Interface controls output enables, OE pins and SMBus enable bits are disabled. |
| E | 11 | vOE10#/SHFT_LD# | Input | Active low input for enabling output 10 or SHFT_LD# pin for the Side-Band Interface. Refer to the Side-Band Interface section for details. This pin has an internal pull-down.<br>**OE mode**: 1 = disable output, 0 = enable output.<br>**Side-Band Mode**: 1 = enable Side-Band Interface shift register, 0 = disable Side-Band Interface shift register. A falling edge transfers Side-Band shift register contents to output register. |
| E | 12 | vOE9# | Input | Active low input for enabling output 9. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| F | 1 | DIF19# | Output | Differential complementary clock output. |
| F | 2 | NC | — | No connection. |
| F | 11 | NC | — | No connection. |
| F | 12 | DIF9# | Output | Differential complementary clock output. |
| G | 1 | DIF_IN | Input | HCSL true input. |
| G | 2 | NC | — | No connection. |
| G | 11 | NC | — | No connection. |
| G | 12 | DIF9 | Output | Differential true clock output. |
| H | 1 | DIF_IN# | Input | HCSL complementary input. |
| H | 2 | VDDR3.3 | Power | Power supply for differential input clock (receiver). This $V_{DD}$ should be treated as an analog power rail and filtered appropriately. Nominally 3.3V. |
| H | 11 | vOE8# | Input | Active low input for enabling output 8. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| H | 12 | DIF8# | Output | Differential complementary clock output. |
| J | 1 | DIF0 | Output | Differential true clock output. |
| J | 2 | NC | — | No connection. |
| J | 11 | NC | — | No connection. |
| J | 12 | DIF8 | Output | Differential true clock output. |
| K | 1 | DIF0# | Output | Differential complementary clock output. |
| K | 2 | NC | — | No connection. |
| K | 11 | vOE7# | Input | Active low input for enabling output 7. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |

**Table 1. Pin Descriptions (Cont.)**

| Number | | Name | Type | Description |
|---|---|---|---|---|
| K | 12 | DIF7# | Output | Differential complementary clock output. |
| L | 1 | DIF1 | Output | Differential true clock output. |
| L | 2 | VDDO3.3 | Power | Power supply for outputs. Nominally 3.3V. |
| L | 3 | NC | N/A | No connection. |
| L | 4 | SMBDAT | I/O | Data pin of SMBUS circuitry. |
| L | 5 | SMBCLK | Input | Clock pin of SMBUS circuitry. |
| L | 6 | NC | — | No connection. |
| L | 7 | NC | — | No connection. |
| L | 8 | vOE5#/DATA | Input | Active low input for enabling output 5 or the data pin for the Side-Band Interface. Refer to the Side-Band Interface section for details. This pin has an internal pull-down.<br>**OE mode**: 1 = disable output, 0 = enable output.<br>**Side-Band mode**: Data pin. |
| L | 9 | NC | — | No connection. |
| L | 10 | vOE6#/CLK | Input | Active low input for enabling output 6 or the clock pin for the Side-Band Interface shift register. Refer to the Side-Band Interface section for details. This pin has an internal pull-down.<br>**OE mode:** 1 = disable output, 0 = enable output.<br>**Side Band mode**: Clocks data into the Side-Band Interface shift register on the rising edge. |
| L | 11 | VDDO3.3 | Power | Power supply for outputs. Nominally 3.3V. |
| L | 12 | DIF7 | Output | Differential true clock output. |
| M | 1 | DIF1# | Output | Differential complementary clock output. |
| M | 2 | DIF2 | Output | Differential true clock output. |
| M | 3 | DIF2# | Output | Differential complementary clock output. |
| M | 4 | DIF3 | Output | Differential true clock output. |
| M | 5 | DIF3# | Output | Differential complementary clock output. |
| M | 6 | vCKPWRGD_PD# | Input | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down mode, subsequent high assertions exit Power Down mode. This pin has internal pull-down resistor. |
| M | 7 | DIF4 | Output | Differential true clock output. |
| M | 8 | DIF4# | Output | Differential complementary clock output. |
| M | 9 | DIF5 | Output | Differential true clock output. |
| M | 10 | DIF5# | Output | Differential complementary clock output. |
| M | 11 | DIF6 | Output | Differential true clock output. |
| M | 12 | DIF6# | Output | Differential complementary clock output. |
| — | | EPAD | GND | Connect EPAD to ground. |

# Output Control

**Table 2. Output Control (SBEN = 0)**

| | | Traditional Interface | | Side Band Interface | | Outputs |
|---|---|---|---|---|---|---|
| CKPWRGD_PD# | DIF_IN | OEx bit Byte[2:0] | OEx# Pin | MASKx Byte[10:8] | Qx | DIFx |
| 0 | X | X | X | X | X | Low/Low |
| 1 | Running | 0 | X | X | X | Low/Low |
| | | 1 | 0 | X | X | Running |
| | | 1 | 1 | X | X | Low/Low |
| 1 | Stopped | 1 | 0 | X | X | Stopped |
| | | 1 | 1 | X | X | Low/Low |

**Table 3. Output Control (SBEN = 1)**

| | | Traditional Interface | | Side Band Interface | | Outputs |
|---|---|---|---|---|---|---|
| CKPWRGD_PD# | DIF_IN | OEx bit Byte[2:0] | OEx# Pin | MASKx Byte[10:8] | Qx | DIFx |
| 0 | X | X | X | X | X | Low/Low |
| 1 | Running | X | X | 0 | 0 | Low/Low |
| | | X | X | 0 | 1 | Running |
| | | X | X | 1 | X | Running |
| 1 | Stopped | X | X | 0 | 0 | Low/Low |
| | | X | X | 0 | 1 | Stopped |
| | | X | X | 1 | X | Stopped |

# Power Management

**Table 4. Power Connections**

| Pin Number | | Description |
|---|---|---|
| $V_{DD}$ | GND | |
| B6, H2 | EPAD | Analog |
| B2, B11, L2, L11 | EPAD | Outputs |

# Output Enable Control on 9QXL2001B (DB2000QL)

## Traditional Method

The 20-output 9QXL2001B has two methods for enabling and disabling outputs. The first is the traditional method of OE# pins and SMBus output enable bits. Outputs 5 through 12 have dedicated output enable pins and each of the 20 outputs have dedicated SMBus output enable bits in Bytes[0:2] of the SMBus register set.

## Side-Band Interface

The second method is a simple 3-wire serial interface referred to as the Side-Band Interface (SBI). This interface consists of DATA, CLK and SHFT_LD# pins. When the SHFT_LD# pin is high, the rising edge of CLK can shift DATA into the shift register. After shifting data, the falling edge of SHFT_LD# clocks the shift register contents to the Output register.

Both the SBI and the traditional interface feed common output enable/disable synchronization logic ensuring glitch free enable and disable of outputs, regardless of the method used.

Both interfaces are not active at the same time, and the SBEN pin selects which interface is active. Tying the SBEN high enables the SBI. Tying the SBEN pin low enables the traditional OE# pin/SMBus output enable interface. When the SBI is enabled, OE[7:9, 11,12]# are disabled and DATA, CLK and SHFT_LD# are enabled on OE5#, OE6# and OE10# respectively. Additionally, SMBus registers for masking off the disable function of the shift register (0 value of a bit) become active. When set to a one, the mask register forces its respective output to 'enabled'. This prevents accidentally disabling critical outputs when using the SBI.

An SMBus read back bit in Byte 4 indicates which output enable control interface is enabled.

When the SBI is enabled, and power has been applied, the SBI is active, even if the CKPWRGD_PD# pin indicates the part is in power down. This allows loading the shift register and transferring the contents to the output register before the assertion of CKPWRGD. Note that the mask registers are part of the normal SMBus interface and cannot be accessed when the CKPWRGD_PD# is low. Figure 1 provides a functional description of the SBI.

The SBI and the traditional SMBus output enable registers both default to the 'output enabled' state at power-up. The mask registers default to zero at power-up, allowing the shift register bits to disable their respective output. See Figure 2.

**Figure 2. Side Band Interface Control Logic – Functional Description**

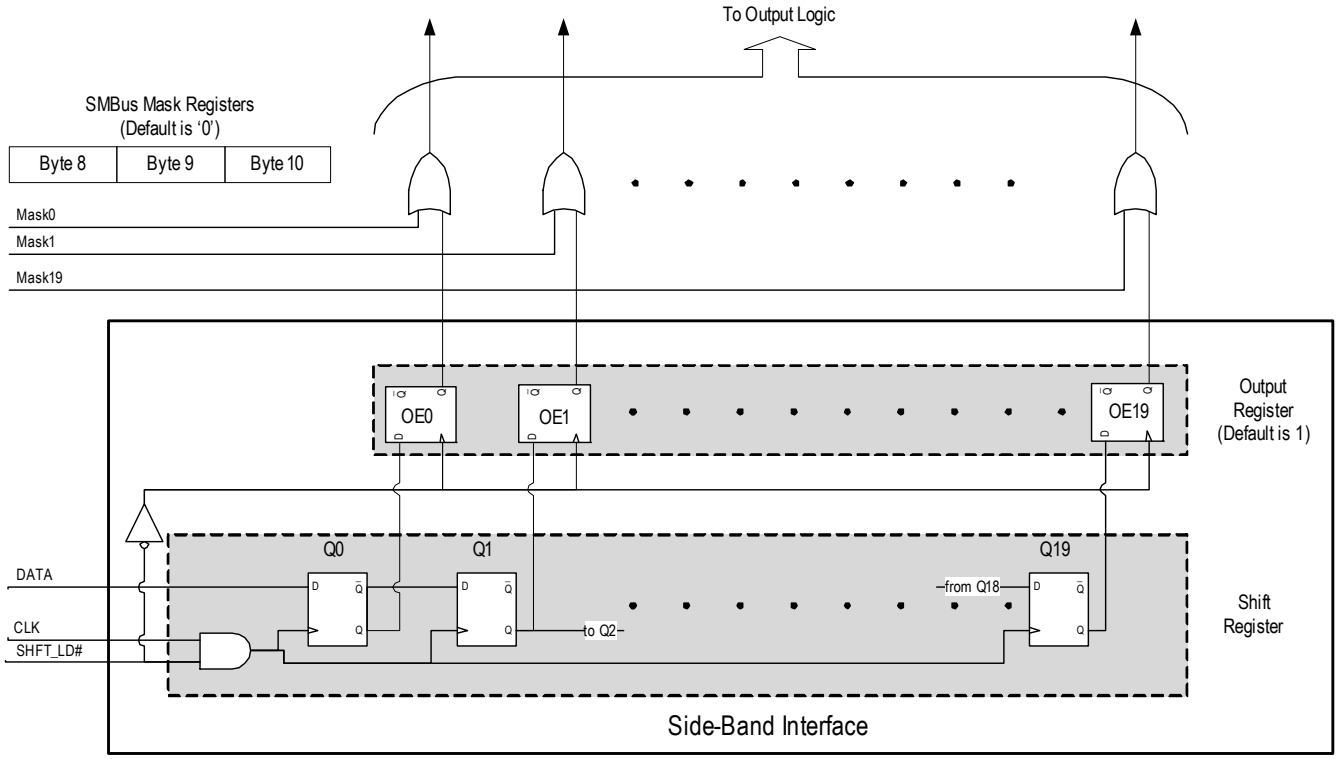
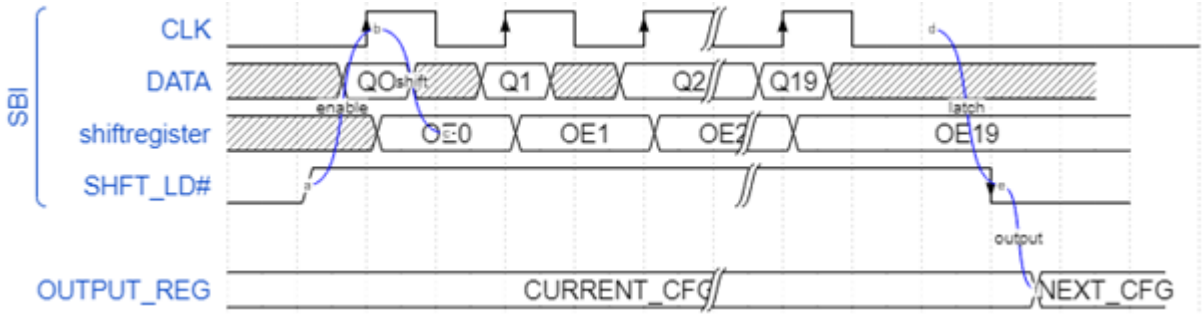



Figure 3 shows the basic timing of the side-band interface. The SHFT_LD# pin goes high to enable the CLK input. Next, the rising edge of CLK clocks enable DATA into the shift register. After the 20th clock for output 19, stop the clock low and drive the SHFT_LD# pin low. The falling edge of SHFT_LD# clocks the shift register contents to the output register, enabling or disabling the outputs. Always shift 20 bits of data into the shift register to control the outputs.

**Figure 3. Side Band Interface Functional Timing**




The SBI interface supports clock rates up to 10MHz. Multiple devices may share CLK and DATA pins. Dedicating a SHFT_LD# pin to each devices allows its use as a chip-select pin. When the SHFT_LD# pin is low, the 9QXL2001 ignores any activity on the CLK and DATA pins.

# Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9QXL2001B at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 5. Absolute Maximum Ratings**

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DDx}$ | | | | 3.9 | V | 1,2 |
| Input Low Voltage | $V_{IL}$ | | GND - 0.5 | | | V | 1 |
| Input High Voltage | $V_{IH}$ | Except for SMBus interface. | | | $V_{DD}$ + 0.5 | V | 1,3 |
| Input High Voltage | $V_{IHSMB}$ | SMBus clock and data pins. | | | 3.9 | V | 1 |
| Storage Temperature | $T_S$ | | -65 | | 150 | °C | 1 |
| Junction Temperature | $T_J$ | Maximum operating junction temperature. | | | 125 | °C | 1 |
| Input ESD Protection | ESD Prot | Human Body Model. | 2500 | | | V | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 3.9V.

# Thermal Characteristics

**Table 6. Thermal Characteristics**

| Parameter | Symbol | Conditions | Package | Typical Value | Units | Notes |
|---|---|---|---|---|---|---|
| Thermal Resistance | $\theta_{JC}$ | Junction to case. | NHG80 | 44 | °C/W | 1 |
| | $\theta_{Jb}$ | Junction to base. | | 2 | °C/W | 1 |
| | $\theta_{JA0}$ | Junction to air, still air. | | 33 | °C/W | 1 |
| | $\theta_{JA1}$ | Junction to air, 1 m/s air flow. | | 29 | °C/W | 1 |
| | $\theta_{JA3}$ | Junction to air, 3 m/s air flow. | | 28 | °C/W | 1 |
| | $\theta_{JA5}$ | Junction to air, 5 m/s air flow. | | 27 | °C/W | 1 |

[1] EPAD soldered to board.

# Electrical Characteristics

$T_A = T_{AMB}$. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

### Table 7. SMBus

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| SMBus Input Low Voltage | $V_{ILSMB}$ | | | | 0.8 | V | |
| SMBus Input High Voltage | $V_{IHSMB}$ | | 2.1 | | $V_{DDSMB}$ | V | |
| SMBus Output Low Voltage | $V_{OLSMB}$ | At $I_{PULLUP.}$ | | | 0.4 | V | |
| SMBus Sink Current | $I_{PULLUP}$ | At $V_{OL.}$ | 4 | | | mA | |
| Nominal Bus Voltage | $V_{DDSMB}$ | | 2.7 | | 3.6 | V | 1 |
| SCLK/SDATA Rise Time | $t_{RSMB}$ | (Max $V_{IL}$ - 0.15V) to (Min $V_{IH}$ + 0.15V). | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | $t_{FSMB}$ | (Min $V_{IH}$ + 0.15V) to (Max $V_{IL}$ - 0.15V). | | | 300 | ns | 1 |
| SMBus Operating Frequency | $f_{SMB}$ | SMBus operating frequency. | | | 400 | kHz | 5 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

[5] The device must be powered up with CKPWRGD_PD# = '1' for the SMBus to be active

### Table 8. DIF_IN Clock Input Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input Crossover Voltage – DIF_IN | $V_{CROSS}$ | Crossover voltage. | 100 | | 900 | mV | 1 |
| Input Swing – DIF_IN | $V_{SWING}$ | Differential value. | 200 | | | mV | 1 |
| Input Slew Rate – DIF_IN | dv/dt | Measured differentially. | 0.7 | | | V/ns | 1,2 |
| Input Leakage Current | $I_{IN}$ | CLK_IN#, $V_{IN}$ = 0.8V,<br>CLK_IN, $V_{IN} = V_{DD.}$ | -150 | | 40 | µA | |
| Input Duty Cycle | $d_{tin}$ | Measurement from differential waveform. | 45 | | 55 | % | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

### Table 9. Input/Supply/Common Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DDx}$ | Supply voltage for core and analog. | 3.135 | 3.3 | 3.465 | V | |
| Ambient Operating Temperature | $T_{AMB}$ | Industrial range. | -40 | 25 | 85 | °C | |
| Input High Voltage | $V_{IH}$ | Single-ended inputs, except SMBus, tri-level inputs. | 2 | | $V_{DD}$ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ | Single-ended inputs, except SMBus, tri-level inputs. | GND - 0.3 | | 0.8 | V | |

**Table 9. Input/Supply/Common Parameters (Cont.)**

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | Tri-level inputs. | 2.2 | | $V_{DD}$ + 0.3 | V | |
| Input Mid Voltage | $V_{IM}$ | Tri-level inputs. | 1.2 | $V_{DD}$/2 | 1.8 | V | |
| Input Low Voltage | $V_{IL}$ | Tri-level inputs. | GND - 0.3 | | 0.8 | V | |
| Input Current | $I_{IN}$ | Single-ended inputs, $V_{IN}$ = GND, $V_{IN}$ = $V_{DD}$. | -5 | | 5 | µA | |
| | $I_{INP}$ | Single-ended inputs.<br>$V_{IN}$ = 0 V; inputs with internal pull-up resistors.<br>$V_{IN}$ = $V_{DD}$; inputs with internal pull-down resistors. | -50 | | 50 | µA | |
| Input Frequency | $F_{IN}$ | $V_{DD}$ = 3.3V. | 1 | | 400 | MHz | |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH | 1 |
| Capacitance | $C_{IN}$ | Logic inputs, except DIF_IN. | 1.5 | | 5 | pF | 1 |
| | $C_{INDIF_IN}$ | DIF_IN differential clock inputs. | 1.5 | | 2.7 | pF | 1,4 |
| | $C_{OUT}$ | Output pin capacitance. | | | 6 | pF | 1 |
| Clk Stabilization | $T_{STAB}$ | From $V_{DD}$ power-up and after input clock stabilization or de-assertion of PD# to 1st clock. | | 1.0 | 1.8 | ms | 1,2 |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion.<br>DIF stop after OE# deassertion. | 4 | 5 | 10 | clocks | 1,2,3 |
| Tdrive_PD# | $t_{DRVPD}$ | DIF output enable after PD# de-assertion. | | 76 | 300 | µs | 1,3 |
| Tfall | $t_F$ | Fall time of control inputs. | | | 5 | ns | 2 |
| Trise | $t_R$ | Rise time of control inputs. | | | 5 | ns | 2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

**Table 10. Side Band Interface**

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Clock Period | $t_{PERIOD}$ | Clock period. | 40 | | | ns | |
| Setup Time to Clock | $t_{SETUP}$ | SHFT setup to CLK rising edge. | 10 | | | ns | |
| Data Setup Time | $t_{DSU}$ | DATA setup to CLK rising edge. | 5 | | | ns | |
| Data Hold Time | $t_{DHOLD}$ | DATA hold after CLK rising edge. | 2 | | | ns | 1 |
| Delay Time | $t_{DELAY}$ | Delay from CLK rising edge to LD# falling edge. | 10 | | | ns | 1 |
| Propagation Delay | $t_{PD}$ | Delay from LD# falling edge to next output configuration taking effect. | 4 | | 10 | clocks | 3 |
| Slew Rate | $t_{SLEW}$ | CLK input (between 20% and 80%). | 0.7 | | 4 | V/ns | 2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Refers to device differential input clock.

### Table 11. LP-HCSL Outputs Driving High Impedance Receiver at 100MHz

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limit | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| Slew Rate | dV/dt | Scope averaging on, fast setting. | 2 | 2.4 | 3.5 | 2 to 4 | V/ns | 1,2,3 |
| Rise/Fall Matching | ΔtR/tF | Single-ended measurement. | | 4.8 | 15 | 20 | % | |
| Maximum Voltage | Vmax | Measurement on single ended signal using absolute value. (scope averaging off). | 700 | 800 | 900 | 660 to 1150 | mV | 7,8 |
| Minimum Voltage | Vmin | | -150 | -43 | 75 | -300 to +150 | | 1,5,7,8 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off. | 250 | 391 | 550 | 250 to 550 | mV | 1,6,7 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off. | | 18 | 50 | 140 | mV | 1,6,7 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

[8] Includes 300mV of overshoot for Vmax and 300mV of undershoot for Vmin.

### Table 12. Current Consumption

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| Operating Supply Current | $I_{DDVDD}$ | Source termination, all outputs 100MHz, $C_L$ = 2pF; Zo = 85Ω. | | 169 | 195 | mA |
| | $I_{DDVDDA/R}$ | | | 5 | 6 | mA |
| Powerdown Current | $I_{DDVDDPD}$ | All differential pairs low-low. | | 1 | 2 | mA |
| | $I_{DDVDDA/RPD}$ | All differential pairs low-low. | | 2 | 3 | mA |

### Table 13. Skew and Differential Jitter Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| CLK_IN, DIF[x:0] | $t_{PD}$ | Input-to-output skew. | 2.3 | 2.7 | 3.3 | ns | 1,2,3,4,5,7 |
| CLK_IN, DIF[x:0] | $t_{PDVARIATION}$ | Input-to-output skew variation for a given device at a given voltage. | | | 2 | ps/°C | 1,2,3,5,8 |
| DIF[x:0] | $t_{SKEW_ALL}$ | Output-to-output skew across all outputs. | | 35 | 50 | ps | 1,2,3,7 |
| Duty Cycle Distortion | $t_{DCD}$ | Measured differentially at 100MHz. | -0.5 | -0.2 | 0.5 | % | 1,6,7 |

[1] Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point.

[3] All input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

[4] Measured with scope averaging on to find mean value.

[5] Guaranteed by design and characterization, not 100% tested in production.

[6] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[7] Measured from differential waveform.

[8] This is the amount of input-to-output delay variation with respect to temperature. This is equivalent to 250ps over the -40°C to +85°C temperature range.

**Table 14. Filtered Phase Jitter Parameters – PCIe Common Clocked (CC) Architectures**

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| Additive Phase Jitter | $t_{jphPCIeG1-CC}$ | PCIe Gen1 | | 0.2 | 5 | Not applicable | ps (p-p) | 1,2,3,4 |
| | $t_{jphPCIeG2-CC}$ | PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz) | | 0.004 | 0.005 | | ps (rms) | 1,2,4,6 |
| | | PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz) | | 0.07 | 0.09 | | ps (rms) | 1,2,4,6 |
| | $t_{jphPCIeG3/4-CC}$ | PCIe Gen3, Gen4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz) | | 0.03 | 0.04 | | ps (rms) | 1,2,4,6 |
| | $t_{jphPCIeG5-CC}$ | PCIe Gen5 (see PCIe Gen5 specifications for details) | | 0.01 | 0.02 | | ps (rms) | 1,2,4,6 |

**Table 15. Filtered Phase Jitter Parameters – PCIe Independent Reference (IR) Architectures**

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| Additive Phase Jitter | $t_{jphPCIeG2-SRIS}$ | PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz) | | 0.09 | 0.11 | Not applicable | ps (rms) | 1,2,4,6 |
| | $t_{jphPCIeG3-SRIS}$ | PCIe Gen3 (PLL BW of 2–4MHz, CDR = 10MHz) | | 0.02 | 0.03 | | ps (rms) | 1,2,4,6 |

**Notes on PCIe Filtered Phase Jitter tables**

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Applies to all outputs when driven by a low phase noise source.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of $1^{-12}$.

[4] Additive jitter for RMS values is calculated by solving the following equation for b [$b = sqrt(c^2 - a^2)$] where "a" is rms input jitter and "c" is rms total jitter.

[5] IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures. According to the PCIe Base Specification Rev4.0 version 1.0, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. The IR filters from the PCIe Base Specification, Rev 3.1a are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 or Gen4 data rates at the time of publication.

[6] Measured using SMA100B signal source, or equivalent, and a phase noise analyzer.

**Table 16. Filtered Phase Jitter Parameters – DB2000Q Filter**

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limit | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| Additive Phase Jitter | $t_{jphDB2000Qadd}$ | 100MHz | | 23 | 25 | 80 | fs (rms) | 1,2,3 |

[1] Measured using SMA100B signal source, or equivalent, and a phase noise analyzer.

[2] After applying DB2000Q filter.

[3] Additive jitter for RMS values is calculated by solving for b where [$b = sqrt(c^2 - a^2)$] where "a"' is rms input jitter and "c" is rms total jitter.

**Table 17. Unfiltered Phase Jitter Parameters – 12kHz to 20MHz**

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| Additive Phase Jitter | $t_{jph12k-20Madd}$ | 100MHz | | 97 | 106 | Not applicable | fs (rms) | 1,2,3 |
| | | 156.25MHz | | 86 | 94 | | | |

[1] Measured using SMA100B signal source, or equivalent, and a phase noise analyzer.

[2] 12kHz-20MHz brick wall filter.

[3] Additive jitter for RMS values is calculated by solving for b where [$b = sqrt(c^2 - a^2)$] where "a"' is rms input jitter and "c" is rms total jitter.

# Test Loads

**Figure 4. AC/DC Test Load for High Impedance Receivers**

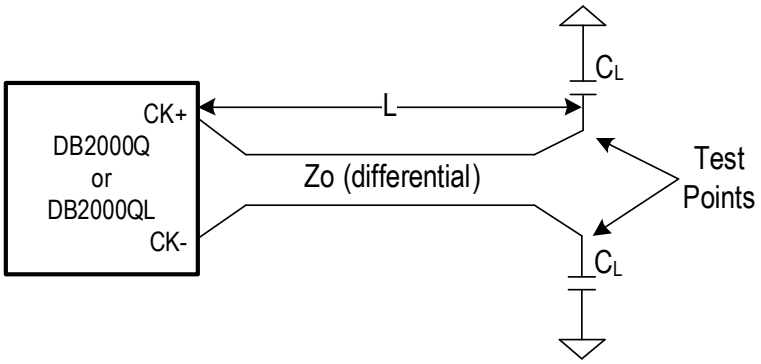



**Figure 5. Test Setup for DB2000Q Additive Phase Jitter Measurement**

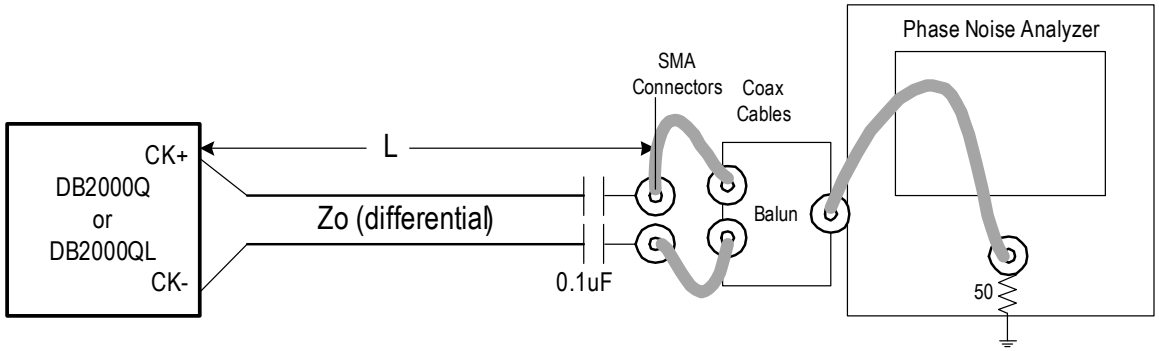


**Table 18. Parameters for Test Loads**

| Rs (Ω) | Zo (Ω) | L (cm) | $C_L$ (pF) |
|---|---|---|---|
| Internal | 85 | 25.4 | 2 |

# Alternate Terminations

The LP-HCSL output can easily drive other logic families. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for termination schemes for LVPECL, LVDS, CML and SSTL.

# SMBus Addressing

**Table 19. SMBus Address Selection**

| SADR(1:0)_tri | SMBus Address (Read/Write bit = 0) |
|---|---|
| 00 | D8 |
| 0M | DA |
| 01 | DE |
| M0 | C2 |
| MM | C4 |
| M1 | C6 |
| 10 | CA |
| 1M | CC |
| 11 | CE |

# General SMBus Serial Interface Information

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **Renesas (Slave/Receiver)** |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **Renesas (Slave/Receiver)** |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count=X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

**SMBus Table: Output Enable Register (Register functional only when SBEN = 0)**

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | DIF_19_En | Output Enable | RW | Low/Low | Enable | 1 |
| Bit 5 | DIF_18_En | Output Enable | RW | Low/Low | Enable | 1 |
| Bit 4 | DIF_17_En | Output Enable | RW | Low/Low | Enable | 1 |
| Bit 3 | DIF_16_En | Output Enable | RW | Low/Low | Enable | 1 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | Reserved | | | | | 0 |

**SMBus Table: Output Enable Register (Register functional only when SBEN = 0)**

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | DIF_7_En | Output Enable | RW | Disabled Low/Low | OE7# Controls | 1 |
| Bit 6 | DIF_6_En | Output Enable | RW | | OE6# Controls | 1 |
| Bit 5 | DIF_5_En | Output Enable | RW | | OE5# Controls | 1 |
| Bit 4 | DIF_4_En | Output Enable | RW | | Enabled | 1 |
| Bit 3 | DIF_3_En | Output Enable | RW | | Enabled | 1 |
| Bit 2 | DIF_2_En | Output Enable | RW | | Enabled | 1 |
| Bit 1 | DIF_1_En | Output Enable | RW | | Enabled | 1 |
| Bit 0 | DIF_0_En | Output Enable | RW | | Enabled | 1 |

**SMBus Table: Output Enable Register (Register functional only when SBEN = 0)**

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | DIF_15_En | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 6 | DIF_14_En | Output Enable | RW | | Enabled | 1 |
| Bit 5 | DIF_13_En | Output Enable | RW | | Enabled | 1 |
| Bit 4 | DIF_12_En | Output Enable | RW | | OE12# Controls | 1 |
| Bit 3 | DIF_11_En | Output Enable | RW | | OE11# Controls | 1 |
| Bit 2 | DIF_10_En | Output Enable | RW | | OE10# Controls | 1 |
| Bit 1 | DIF_9_En | Output Enable | RW | | OE9# Controls | 1 |
| Bit 0 | DIF_8_En | Output Enable | RW | | OE8# Controls | 1 |

### SMBus Table: OE# Pin Readback Register

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | RB_OE12 | Status of OE12# | R | Pin Low | Pin High | Real-time |
| Bit 6 | RB_OE11 | Status of OE11# | R | | | Real-time |
| Bit 5 | RB_OE10 | Status of OE10# | R | | | Real-time |
| Bit 4 | RB_OE9 | Status of OE9# | R | | | Real-time |
| Bit 3 | RB_OE8 | Status of OE8# | R | | | Real-time |
| Bit 2 | RB_OE7 | Status of OE7# | R | | | Real-time |
| Bit 1 | RB_OE6 | Status of OE6# | R | | | Real-time |
| Bit 0 | RB_OE5 | Status of OE5# | R | | | Real-time |

### SMBus Table: SBEN Readback Register

| Byte 4 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | RB_SBEN | Status of SBEN | R | Pin Low | Pin High | Real-time |

### SMBus Table: Vendor & Revision ID Register

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | RID3 | REVISION ID | R | B rev is 0001 | | 0 |
| Bit 6 | RID2 | | R | | | 0 |
| Bit 5 | RID1 | | R | | | x |
| Bit 4 | RID0 | | R | | | x |
| Bit 3 | VID3 | VENDOR ID | R | IDT/ICS | | 0 |
| Bit 2 | VID2 | | R | | | 0 |
| Bit 1 | VID1 | | R | | | 0 |
| Bit 0 | VID0 | | R | | | 1 |

### SMBus Table: Device ID

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Device ID 7 (MSB) | | R | C9 | | 1 |
| Bit 6 | Device ID 6 | | R | | | 1 |
| Bit 5 | Device ID 5 | | R | | | 0 |
| Bit 4 | Device ID 4 | | R | | | 0 |
| Bit 3 | Device ID 3 | | R | | | 1 |
| Bit 2 | Device ID 2 | | R | | | 0 |
| Bit 1 | Device ID 1 | | R | | | x |
| Bit 0 | Device ID 0 | | R | | | 1 |

### SMBus Table: Byte Count Register

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | BC4 | Writing to this register configures how many bytes will be read back. | RW | Default value is 7. | | 0 |
| Bit 3 | BC3 | | RW | | | 0 |
| Bit 2 | BC2 | | RW | | | 1 |
| Bit 1 | BC1 | | RW | | | 1 |
| Bit 0 | BC0 | | RW | | | 1 |

### SMBus Table: Side Band Mask Register (Register functional only when SBEN = 1)

| Byte8 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Mask7 | Masks off Side-band Disable | RW | Side-band shift register may disable the output | Forces output to always be enabled regardless of side-band shift register value | 0 |
| Bit 6 | Mask6 | Masks off Side-band Disable | RW | | | 0 |
| Bit 5 | Mask5 | Masks off Side-band Disable | RW | | | 0 |
| Bit 4 | Mask4 | Masks off Side-band Disable | RW | | | 0 |
| Bit 3 | Mask3 | Masks off Side-band Disable | RW | | | 0 |
| Bit 2 | Mask2 | Masks off Side-band Disable | RW | | | 0 |
| Bit 1 | Mask1 | Masks off Side-band Disable | RW | | | 0 |
| Bit 0 | Mask0 | Masks off Side-band Disable | RW | | | 0 |

### SMBus Table: Side Band Mask Register (Register functional only when SBEN = 1)

| Byte 9 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Mask15 | Masks off Side-band Disable | RW | Side-band shift register may disable the output | Forces output to always be enabled regardless of side-band shift register value | 0 |
| Bit 6 | Mask14 | Masks off Side-band Disable | RW | | | 0 |
| Bit 5 | Mask13 | Masks off Side-band Disable | RW | | | 0 |
| Bit 4 | Mask12 | Masks off Side-band Disable | RW | | | 0 |
| Bit 3 | Mask11 | Masks off Side-band Disable | RW | | | 0 |
| Bit 2 | Mask10 | Masks off Side-band Disable | RW | | | 0 |
| Bit 1 | Mask9 | Masks off Side-band Disable | RW | | | 0 |
| Bit 0 | Mask8 | Masks off Side-band Disable | RW | | | 0 |

### SMBus Table: Side Band Mask Register (Register functional only when SBEN = 1)

| Byte 10 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Mask19 | Masks off Side-band Disable | RW | Side-band shift register may disable the output | Forces output to always be enabled regardless of side-band shift register value | 0 |
| Bit 2 | Mask18 | Masks off Side-band Disable | RW | | | 0 |
| Bit 1 | Mask17 | Masks off Side-band Disable | RW | | | 0 |
| Bit 0 | Mask16 | Masks off Side-band Disable | RW | | | 0 |

### SMBus Table: Output Impedance and Slew Rate Trim Register

| Byte 11 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | ZUP_DIF_19 | Impedance Trim DIF_19 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 6 | ZDWN_DIF_19 | | RW | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | ZUP_DIF_18 | Impedance Trim DIF_18 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 3 | ZDWN_DIF_18 | | RW | | | 0 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | ZUP_DIF_17 | Impedance Trim DIF_17 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 0 | ZDWN_DIF_17 | | RW | | | 0 |

### SMBus Table: Output Configuration Register

| Byte 12 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | ZUP_DIF_16 | Impedance Trim DIF_16 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 5 | ZDWN_DIF_16 | | RW | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | ZUP_DIF_15 | Impedance Trim DIF_15 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 2 | ZDWN_DIF_15 | | RW | | | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | Reserved | | | | | 0 |

### SMBus Table: Output Configuration Register

| Byte 13 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | ZUP_DIF_14 | Impedance Trim DIF_14 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 6 | ZDWN_DIF_14 | | RW | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | ZUP_DIF_13 | Impedance Trim DIF_13 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 3 | ZDWN_DIF_13 | | RW | | | 0 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | ZUP_DIF_12 | Impedance Trim DIF_12 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 0 | ZDWN_DIF_12 | | RW | | | 0 |

### SMBus Table: Output Configuration Register

| Byte 14 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | ZUP_DIF_11 | Impedance Trim DIF_11 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 5 | ZDWN_DIF_11 | | RW | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | ZUP_DIF_10 | Impedance Trim DIF_10 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 2 | ZDWN_DIF_10 | | RW | | | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | Reserved | | | | | 0 |

### SMBus Table: Output Configuration Register

| Byte 15 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | ZUP_DIF_9 | Impedance Trim DIF_9 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 6 | ZDWN_DIF_9 | | RW | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | ZUP_DIF_8 | Impedance Trim DIF_8 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 3 | ZDWN_DIF_8 | | RW | | | 0 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | ZUP_DIF_7 | Impedance Trim DIF_7 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 0 | ZDWN_DIF_7 | | RW | | | 0 |

### SMBus Table: Output Configuration Register

| Byte 16 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | ZUP_DIF_6 | Impedance Trim DIF_6 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 5 | ZDWN_DIF_6 | | RW | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | ZUP_DIF_5 | Impedance Trim DIF_5 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 2 | ZDWN_DIF_5 | | RW | | | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | Reserved | | | | | 0 |

### SMBus Table: Output Configuration Register

| Byte 17 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | ZUP_DIF_4 | Impedance Trim DIF_4 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 6 | ZDWN_DIF_4 | | RW | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | ZUP_DIF_3 | Impedance Trim DIF_3 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 3 | ZDWN_DIF_3 | | RW | | | 0 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | ZUP_DIF_2 | Impedance Trim DIF_2 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 0 | ZDWN_DIF_2 | | RW | | | 0 |

### SMBus Table: Output Configuration Register

| Byte 18 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | ZUP_DIF_1 | Impedance Trim DIF_1 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 5 | ZDWN_DIF_1 | | RW | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | ZUP_DIF_0 | Impedance Trim DIF_0 | RW | 00 or 11 = Nominal<br>01 = -5%, 10 = +5% | | 0 |
| Bit 2 | ZDWN_DIF_0 | | RW | | | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | Reserved | | | | | 0 |

**Byte 19 is Reserved.**

### SMBus Table: Stop State Configuration Register

| Byte 20 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | AMP[2] | Global Differential output Control | RW | 0.3V–1V<br>100mV/step<br>Default=750mV | | 1 |
| Bit 6 | AMP[1] | | RW | | | 0 |
| Bit 5 | AMP[0] | | RW | | | 1 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | STOPST[1] | Differential Stop Mode State | RW | 00 = Low/Low | 10 = High/Low | 0 |
| Bit 0 | STOPST[0] | | RW | 01 = HiZ/HiZ | 11 = Low/High | 0 |

### SMBus Table: PD_RESTORE

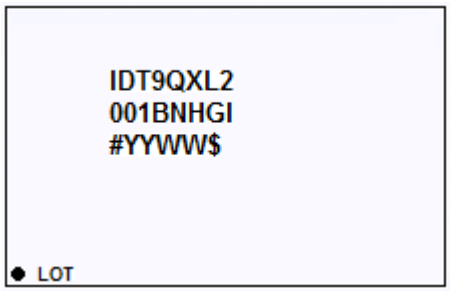
| Byte 21 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | PD_RESTORE# | Save Configuration in Power Down | RW | Config Cleared | Config Saved | 1 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | Reserved | | | | | 0 |

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/nhg80-package-outline-600x600mm-body-050mm050mm-pitch-gqfn

## Marking Diagram




- Lines 1 and 2: part number
  - "I" denotes industrial temperature.
- Line 3:
  - "#" denotes the stepping number.
  - "YYWW" is the last digits of the year and work week that the part was assembled.
  - "$" denotes mark code.
- "LOT" denotes the lot sequence code.

## Ordering Information

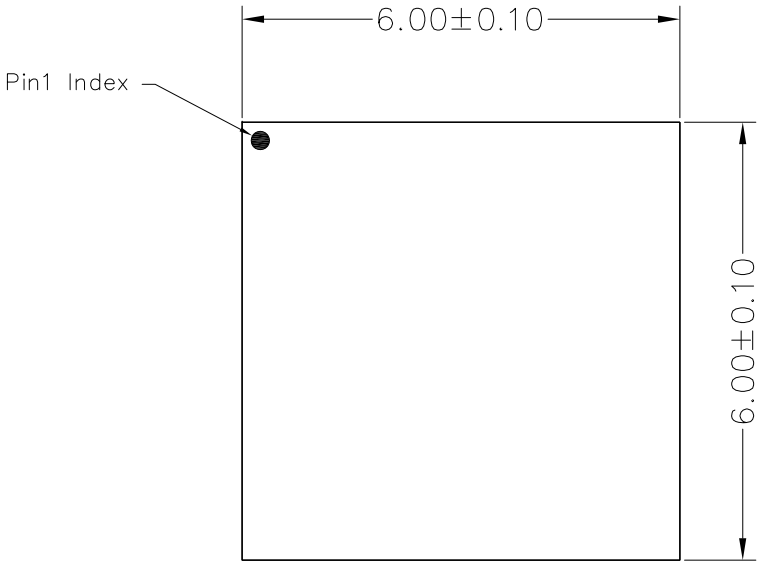
| Orderable Part Number | Package | Carrier Type | Temperature |
|---|---|---|---|
| 9QXL2001BNHGI | 6 × 6 mm, 0.5mm pitch 80-GQFN | Tray | -40° to +85°C |
| 9QXL2001BNHGI8 | 6 × 6 mm, 0.5mm pitch 80-GQFN | Tape and Reel | -40° to +85°C |

"G" designates PB-free configuration, RoHS compliant.
"B" is the device revision designator (will not correlate with the datasheet revision).

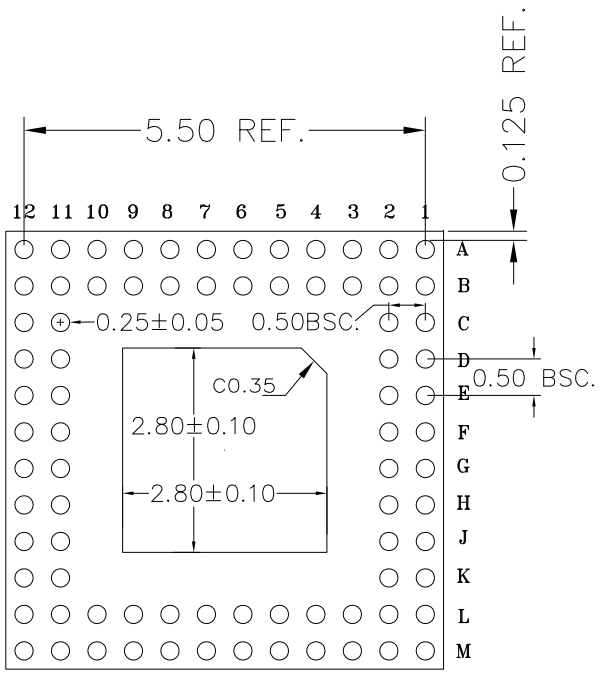
## Revision History

| Revision Date | Description of Change |
|---|---|
| December 1, 2020 | Updated "Simple 3-wire Side-Band Interface..." Features sub-bullet on front page. |
| August 25, 2020 | Updated DB2000Q specifications in *Key Specifications* section on front page. |
| May 6, 2020 | ▪ Added $t_{PDVARIATION}$ specification to Table 13. Footnote 8 added.<br>▪ Adjusted Input to output skew minimum and maximum values in Table 13.<br>▪ Changed Slew Rate Matching to Rise/Fall Matching in Table 11.<br>▪ Updated maximum slew rate from 4V/ns to 3.5V/ns in Table 11. |
| January 7, 2020 | Updated Bytes 0, 1, and 2 register tables to SBEN = 0. |
| June 10, 2019 | Updated Marking Diagram notes. |
| May 28, 2019 | Updated $I_{DDVDD}$ typical value from 143mA to 169mA. |
| February 26, 2019 | Added Thermal Characteristics table. |
| February 15, 2019 | Initial release. |

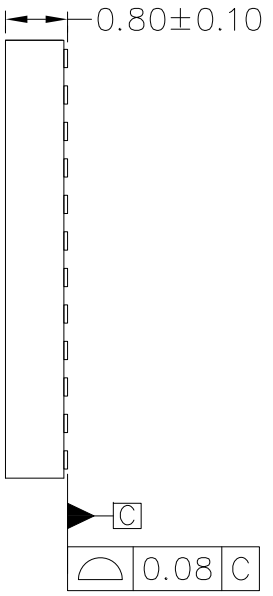
| DATE CREATED | REVISIONS | | |
|---|---|---|---|
| | REV | DESCRIPTION | AUTHOR |
| 05/26/15 | 00 | INITIAL RELEASE | JH |
| 05/26/16 | 01 | UPDATE LAND PATTERN DIMENSION | JH |
| 03/29/17 | 02 | UPDATE PACKAGE THICKNESS | JH |
| 04/01/17 | 03 | UPDATE PACKAGE THICKNESS WITH TOLERANCE RANGE | JH |
| NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE | | | |




TOP VIEW




BOTTOM VIEW




SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.

| | | |
|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± 0.05 ±<br>XXX± 0.012<br>XXXX± | IDT™ www.IDT.com | 6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138<br>PHONE: (408) 284–8200<br>FAX: (408) 284–3572 |
| | TITLE NHG80 PACKAGE OUTLINE 6.00x6.00mm BODY 0.50mm/0.50mm PITCH GQFN | |
| | SIZE C / DRAWING No. PSC–4496 / REV 03 | |
| | DO NOT SCALE DRAWING | SHEET 1 OF 2 |

| DATE CREATED | REVISIONS | | |
|---|---|---|---|
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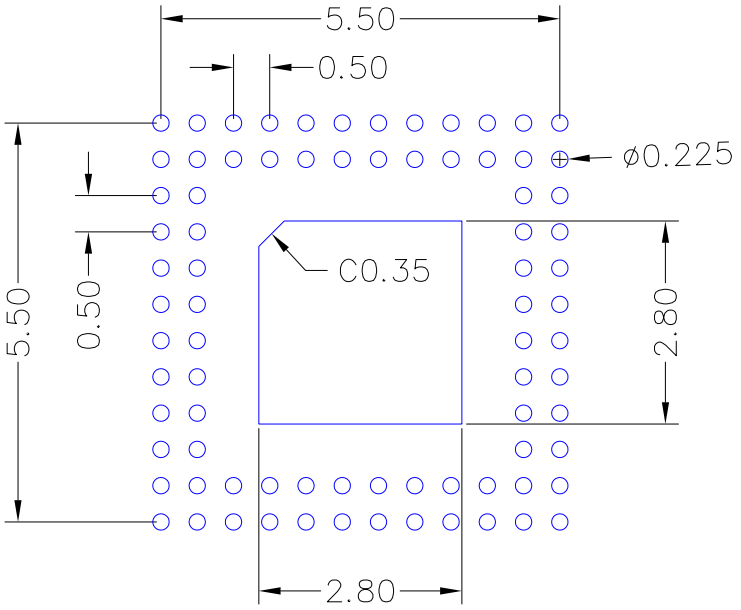


RECOMMENDED LAND PATTERN

NOTE:

1) ALL dimensions are in mm, Angles in degrees.
2) Top down view, as view on PCB.
3) NSMD Land Pattern Assumed.
4) Land Pattern Recommendation as per IPC-7351B generic requirement for surface mount design and Land Pattern.

| | | |
|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± 0.05 ±<br>XXX± 0.012<br>XXXX± | IDT™ www.IDT.com | 6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138<br>PHONE: (408) 284-8200<br>FAX: (408) 284-3572 |
| | TITLE NHG80 PACKAGE OUTLINE 6.00x6.00mm BODY 0.50mm/0.50mm PITCH GQFN | |
| | SIZE C / DRAWING No. PSC-4496 / REV 03 | |
| | DO NOT SCALE DRAWING | SHEET 2 OF 2 |

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(Rev.1.0 Mar 2020)


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