32-pin CK505 for Intel Systems

ICS9LRS4103

Recommended Application:

Main clock for Intel 5/6 series desktop/embedded chipsets

Output Features:

- 1 - Low power push-pull CPU pair
- 1 - Low power push-pull SRC pair
- 1 - Low power push-pull 120MHz DISP/100MHz SRC pair
- 1 - Low power push-pull SATA/100MHz SRC pair
- 1 - Low power push-pull DOT96M pair
- 1 - 14.318M 3.3V REF output

Features/Benefits:

- CPU synchronous with SRC/CPU and SRC can be interchanged for board routing
- Default 0.5% down spread modulation/Reduces EMI
- External 14.318M XTAL/allows precise frequency tuning
- Fully integrated VREG for low power outputs/reduces board space
- Integrated 33ohm Rs on differential outputs/reduces external component cost
- SMBus Interface/unused outputs can be disabled

Key Specifications:

- CPU cycle to cycle jitter <85ps
- SRC cycle to cycle jitter <85ps
- PCIe Gen2 compliant

Table 1: CPU Frequency Select Table

FS_LC B0b7	CPU MHz	SRC MHz	REF MHz	DOT MHz
0 (Default)	133.33	100.00	14.318	96.00
1	100.00			

1. FS_LC is a low-threshold input.Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.

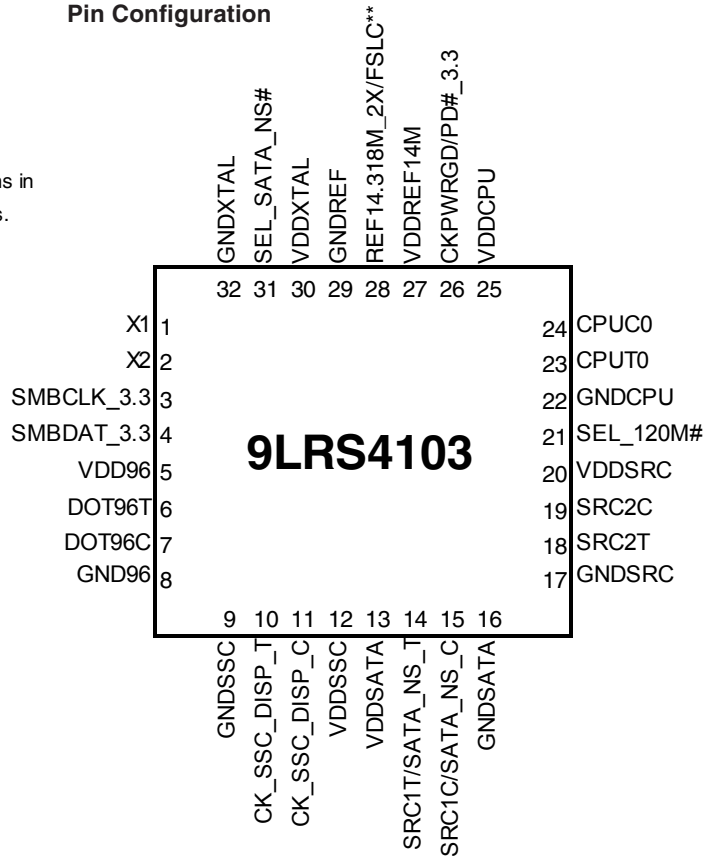
SEL_120M#

Pin# 21	Pin# 10/11
Pulled Low	120MHz
Pulled High	100MHz

SEL_SATA_NS#

Pin# 31	Pin# 14/15
0	100MHz_nonSS
1	100MHz_SS

Pin Configuration



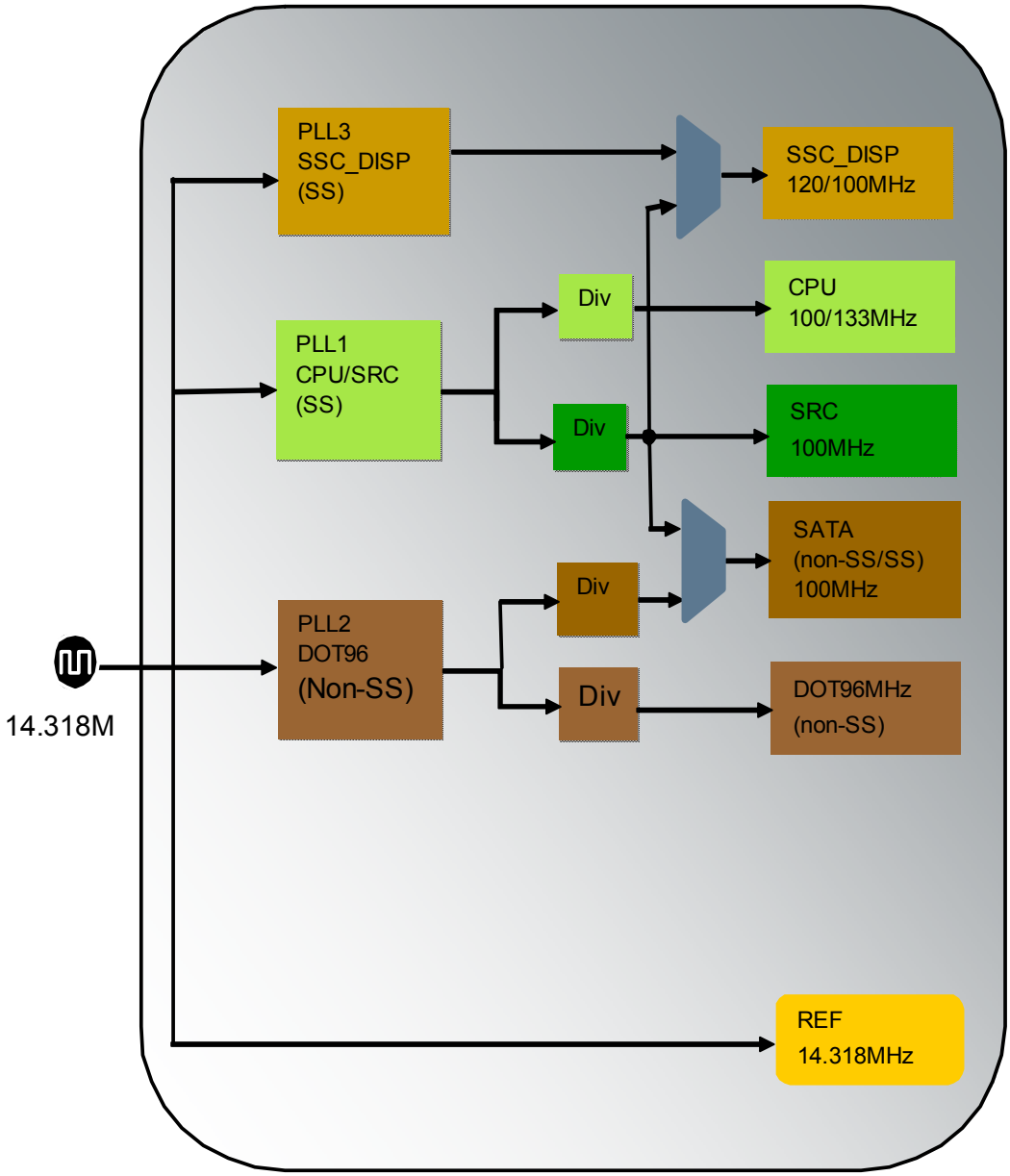
Pin Description

Pin#	Pin Name	Type	Pin Description
1	X1	IN	Crystal input, Nominally 14.318MHzMHz.
2	X2	OUT	Crystal output, Nominally 14.318MHzMHz.
3	SMBCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
4	SMBDAT_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
5	VDD96	PWR	Power pin for the DOT96MHz output 3.3V.
6	DOT96T	OUT	True clock DOT96 output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
7	DOT96C	OUT	Complementary clock DOT96 output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
8	GND96	PWR	Ground pin for the DOT96MHz output.
9	GNDSSC	PWR	Ground pin for the CK_SSC_DISP output.
10	CK_SSC_DISP_T	OUT	True clock of CK_SSC_DISP (100MHz or 120MHz) output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
11	CK_SSC_DISP_C	OUT	Complementary clock of CK_SSC_DISP (100MHz or 120MHz) output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
12	VDDSSC	PWR	Power pin for the CK_SSC_DISP output 3.3V
13	VDDSATA	PWR	Power pin for the SATA output 3.3V
14	SRC1T/SATA_NS_T	OUT	True clock of differential 0.8V push-pull SRC/SATA output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
15	SRC1C/SATA_NS_C	OUT	Complementary clock of differential 0.8V push-pull SRC/SATA output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
16	GNDSATA	PWR	Ground pin for the SATA output.
17	GNDSRC	PWR	Ground pin for the SRC output.
18	SRC2T	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
19	SRC2C	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
20	VDDSRC	PWR	Power pin for the SRC output 3.3V.
21	SEL_120M#	IN	Selects pins #10/11 to be 120MHz or 100MHz. "0" = 120MHz, "1" = 100MHz.
22	GNDCPU	PWR	Ground pin for the CPU output.
23	CPUT0	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
24	CPUC0	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
25	VDDCPU	PWR	Power pin for the CPU output 3.3V
26	CKPWRGD/PD#_3.3	IN	Notifies CK505 to sample latched inputs, or iAMT entry/exit, or PWRDWN# mode
27	VDDREF14M	PWR	Power pin for the REF output 3.3V
28	REF14.318M_2X/FSLC**	I/O	Reference 14.318 MHz clock, which drives 3 loads on default / 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
29	GNDREF	PWR	Ground pin for the REF output.
30	VDDXTAL	PWR	Power pin for XTAL 3.3V
31	SEL_SATA_NS#	IN	Selects pin #14/15 to be SRC1 or SATA_NS. "0" = SATA_NS, "1" = SRC1
32	GNDXTAL	PWR	Ground pin for XTAL.

General Description

The **9LRS4103** is compatible with the Intel CK505 Yellow Cover specification. This clock synthesizer provides a single chip solution for Intel 5 series and newer chipsets. ICS9LRS4103 is driven with a 14.318MHz crystal.

Block Diagram



Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Maximum Supply Voltage	VDDxxx	Core/Logic Supply			4.6	V	1,7
Maximum Supply Voltage	VDDxxx_IO	Low Voltage Differential I/O Supply			3.8	V	1,7
Maximum Input Voltage	V_{IH}	3.3V LVTTL Inputs			4.6	V	1,7,8
Minimum Input Voltage	V_{IL}	Any Input	GND - 0.5			V	1,7
Storage Temperature	Ts	-	-65		150	°C	1,7
Case Temperature	Tcase	-			115	°C	1,7
Input ESD protection	ESD prot	Human Body Model	2000			V	1,7

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Ambient Operating Temp	Tambient	-	0	70	70	°C	1
Supply Voltage	VDDxxx	Supply Voltage	3.135	3.3	3.465	V	1
Input High Voltage	V_{IHSE}	Single-ended inputs	2	4		V	1
Input Low Voltage	V_{ILSE}	Single-ended inputs			0.8	V	1
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5	1	5	uA	1
Input Leakage Current	I_{INRES}	Inputs with pull or pull down resistors $V_{IN} = V_{DD}$, V_{IN} = GND	-200	100	200	uA	1
Output High Voltage	V_{OHSE}	Single-ended outputs, I_{OH} = -1mA	2.4	3.2		V	1
Output Low Voltage	V_{OLSE}	Single-ended outputs, I_{OL} = 1 mA		0.2	0.4	V	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		VDD + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Supply Current	I_{DD}	3.3V supply		87	100	mA	1
Power Down Current	$I_{DD\_PD3.3}$	3.3V supply, Power Down Mode		5	6	mA	1
iAMT Mode Current	$I_{DD\_iAMT3.3}$	3.3V supply, iAMT Mode		49	55	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		14.31818		MHz	2
Pin Inductance	L_{pin}			5	7	nH	1
Input Capacitance	C_{IN}	Logic Inputs	1.5	3	5	pF	1
	C_{OUT}	Output pin capacitance		3	6	pF	1
	C_{INX}	X1 & X2 pins		4	6	pF	1
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30	32.5	33	kHz	1

AC Electrical Characteristics - Input/Common Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Clk Stabilization	TSTAB	From VDD Power-Up or de-assertion of PD# to 1st clock		1	1.8	ms	1
Tfall_PD#	TFALL	Fall/rise time of PD#, PCI_STOP# and CPU_STOP# inputs			5	ns	1
Trise_PD#	TRISE				5	ns	1

AC Electrical Characteristics - Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Slew Rate	tSLR	Differential Measurement	2.5	3.5	4	V/ns	1,2
Falling Edge Slew Rate	tFLR	Differential Measurement	2.5	3.5	4	V/ns	1,2
Slew Rate Variation	tSLVAR	Single-ended Measurement		14	20	%	1
Maximum Output Voltage	VHIGH	Includes overshoot		935	1150	mV	1
Minimum Output Voltage	VLOW	Includes undershoot	-300	-144		mV	1
Differential Voltage Swing	VSWING	Differential Measurement	300	699		mV	1
Crossing Point Voltage	VXABS	Single-ended Measurement	300	438	550	mV	1,3,4
Crossing Point Variation	VXABSVAR	Single-ended Measurement		60	140	mV	1,3,5
Duty Cycle	DCYC	Differential Measurement	45	50.4	55	%	1
CPU Jitter - Cycle to Cycle	CPUJC2C	Differential Measurement		52	85	ps	1
SRC Jitter - Cycle to Cycle	SRCJC2C	Differential Measurement		62	85	ps	1
DOT Jitter - Cycle to Cycle	DOTJC2C	Differential Measurement		150	250	ps	1
SRC Skew	SRCSKEW	Differential Measurement, all SRC from same PLL		93	200	ps	1

Electrical Characteristics - Phase Jitter

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNITS	NOTES
Jitter, Phase	$t_{jphPCIe1}$	PCIe Gen 1 REFCLK phase jitter		43	86	ps	1,2,3
	$t_{jphPCIe2Lo}$	PCIe Gen 2 REFCLK phase jitter Lo-band content		1.8	3	ps (RMS)	1,2,3
	$t_{jphPCIe2Hi}$	PCIe Gen 2 REFCLK phase jitter Hi-band content		2.5	3.1	ps (RMS)	1,2,3

Notes on Phase Jitter:

[1] See http://www.pcisig.com for complete specs. Guaranteed by design and characterization, not tested in production.

[2] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1^{-12}

[3] Applies to output pairs 10/11, 14/15, 18/19, and 23/24 when pins 21 and 31 are set to 1, and CPU is 100MHz.

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	0	0	0	ppm	1,6
Clock period	Tperiod	14.318180 MHz output nominal	69.8413	69.8413	69.8413	ns	6
Absolute min/max period	Tabs	14.318180 MHz including cycle to cycle jitter	68.8413	69.8413	70.84128	ns	6
Output High Voltage	VOH	IOH = -1 mA	2.4	3		V	1
Output Low Voltage	VOL	IOL = 1 mA		0.2	0.4	V	1
Output High Current	IOH	VOH @MIN = 1.0 V, VOH@MAX = 3.135 V	-33	-33	-33	mA	1
Output Low Current	IOL	VOL @MIN = 1.95 V, VOL @MAX = 0.4 V	30	38	38	mA	1
Rising Edge Slew Rate	tSLR	Measured from 0.8 to 2.0 V	1	2.5	4	V/ns	1
Falling Edge Slew Rate	tFLR	Measured from 2.0 to 0.8 V	1	2.5	4	V/ns	1
Duty Cycle	dt1	VT = 1.5 V	45	52	55	%	1
Jitter	tjcyc-cyc	VT = 1.5 V		100	1000	ps	1

Electrical Characteristics - SMBus Interface

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
SMBus Voltage	V_{DD}		2.7	3.3	5.5	V	1
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}		0.3	0.4	V	1
Current sinking at V_{OLSMB} = 0.4 V	I_{PULLUP}	SMB Data Pin	4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
Maximum SMBus Operating Frequency	F_{SMBUS}	Block Mode		400	100	kHz	1

Notes on Electrical Characteristics:

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#. The average cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[6] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF has been tuned to exactly 14.318180 MHz

[7] Operation under these conditions is neither implied, nor guaranteed.

[8] Maximum input voltage is not to exceed maximum VDD

Differential Clock Tolerances

	CPU	SRC/SATA	DOT96	CK_SSC_DISP	
PPM tolerance	100	100	100	100	**ppm**
Cycle to Cycle Jitter	85	85	250	125	**ps**
Spread	-0.50%	-0.50%	0	-0.50%	%

Clock Periods - Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
CPU	100.00	9.91400		9.99900	10.00000	10.00100		10.08600	ns	1,2
	133.33	7.41425		7.49925	7.50000	7.50075		7.58575	ns	1,2
SATA	100.00	9.91400		9.99900	10.00000	10.00100		10.08600	ns	1,2
SRC	100.00	9.91400		9.99900	10.00000	10.00100		10.08600	ns	1,2
CK_SSC_DISP	120.00	8.20750		8.33250	8.33333	8.33417		8.45917	ns	1,2
DOT96	96.00	10.16563		10.41563	10.41667	10.41771		10.66771	ns	1,2

Clock Periods - Differential Outputs with Spread Spectrum Enabled

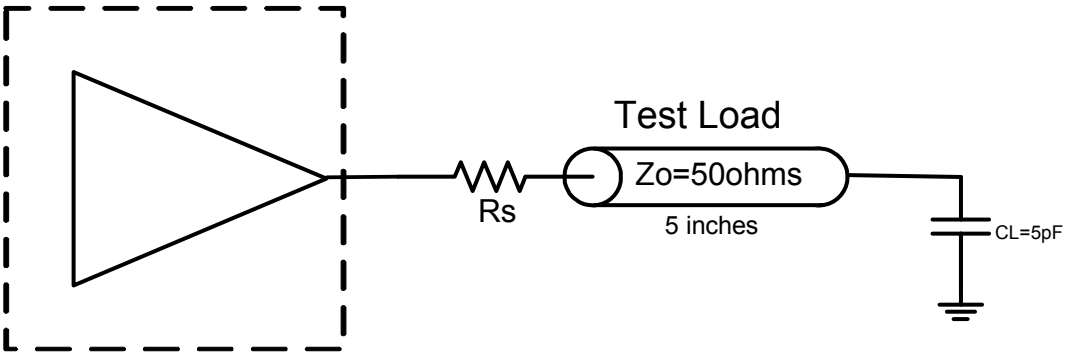
SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
CPU	99.75	9.91406	9.99906	10.02406	10.02506	10.02607	10.05107	10.13607	ns	1,2
	133.00	7.41430	7.49930	7.51805	7.51880	7.51955	7.53830	7.62330	ns	1,2
SRC	99.75	9.91406	9.99906	10.02406	10.02506	10.02607	10.05107	10.13607	ns	1,2
CK_SSC_DISP	119.70	8.20755	8.33255	8.35338	8.35422	8.35505	8.37589	8.50089	ns	1,2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the crystal input is tuned to exactly 14.31818MHz.

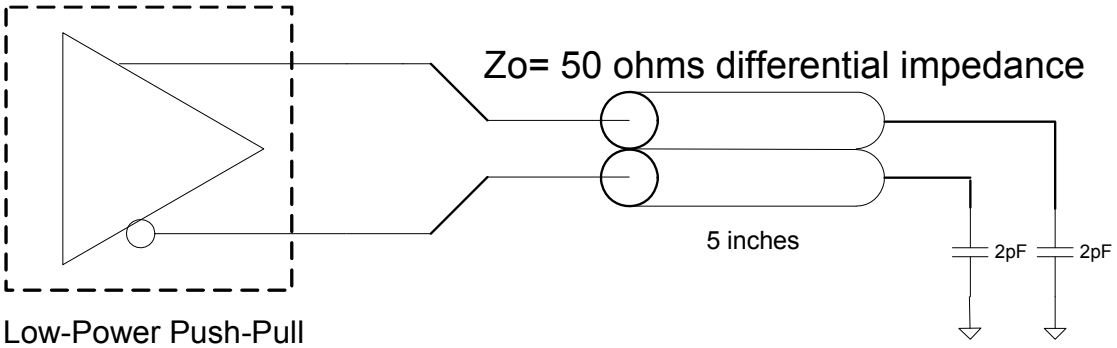
PD# Power Management

	Single-ended Clocks		Differential Clocks	CPU0
Device State	**w/o Latched input**	**w/Latched input**		
Latches Open	Low	Hi-Z	CK= Pull down, CK# = Low	CK= Pull down, CK# = Low
Power Down			CK= Pull down CK# = Low	CK= Pull down CK# = Low
M1			CK= Pull down CK# = Low	Running
Virtual Power Cycle to Latches Open			CK= Pull down, CK# = Low	CK= Pull down, CK# = Low



Single-ended
Output

Low-Power Differential Output (w/Integrated Rs) Test Load



Low-Power Push-Pull
Output w/Rs
(HCSL Compatible)

Table 2: IO_Vout select table

B9b2	B9b1	B9b0	IO_ Vout
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V
1	1	0	0.9V
1	1	1	1.0V

Table 3: Device ID table

B8b7	B8b6	B8b5	B8b4	Comment
0	0	0	0	56 pin TSSOP
0	0	0	1	64 pin TSSOP
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	72 pin QFN
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	32 pin QFN
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Table 4: Series Resistors for REF Output

D.C.Drive Strength	Number of Loads to Drive	REF Strength	Rs	
	1	1x	33Ω [39Ω]	
	1	**2x**	**39Ω [43Ω]**	**Test Load**
	2	2x	27Ω [33Ω]	

Notes:

1. Preferred drive strengths using CK505 clock sources.
2. Desktop/Mobile Platforms with Zo = 50/55 ohms use the first resistor value.
3. Systems with Zo = 60 ohms use the resistor values in brackets [ ].

General SMBus serial interface information for the ICS9LRS4103

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- IDT clock will ***acknowledge***
- Controller (host) sends the beginning byte location = N
- IDT clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- IDT clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- IDT clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- IDT clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- IDT clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- IDT clock will ***acknowledge***
- IDT clock will send the data byte count = X
- IDT clock sends ***Byte N + X -1***
- IDT clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
◇			
◇			◇
◇			◇
			◇
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		IDT (Slave/Receiver)	
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			◇
◇			◇
◇			◇
◇			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Byte 0 FS Readback and PLL Selection Register

Bit	Pin	Name	Description	Type	0	1	Default
7		FSLC	CPU Freq. Sel. Bit	**R**			Latch
6		Reserved	Reserved	RW	-	-	0
5		Reserved	Reserved	RW	-	-	1
4		iAMT_EN	Set via SMBus	RW (Sticky 1)	Legacy Mode	iAMT Enabled	0
3		Reserved	Reserved	RW			0
2		SEL_120M#	Selects pins #10/11 to be 120MHz or 100MHz	**R**	DISP (120MHz)	SRC (100MHz)	Latch
1		SEL_SATA_NS#	Select source for SATA clock	**R**	SATA (100MHz_nonSS)	SRC1 (100MHz SS)	Latch
0		PD_Restore	1 = on Power Down de-assert return to last known state 0 = clear all SMBus configurations as if cold power-on and go to latches open state This bit is ignored and treated at '1' if device is in iAMT mode.	RW	Configuration Not Saved	Configuration Saved	1

Byte 1 CPU/SRC Spread Selection Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	0
6		CK505 PLL1_SSC_SEL	Select 0.5% down or center SSC	RW	Down spread	Center spread	0
5		Reserved	Reserved	RW	-	-	0
4		Reserved	Reserved	RW	-	-	0
3		Reserved	Reserved	RW	-	-	0
2		Reserved	Reserved	RW	-	-	0
1		Reserved	Reserved	RW	-	-	1
0		Reserved	Reserved	RW	-	-	1

Byte 2 Output Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		REF_3L_OE	Output enable for REF0	RW	Output Disabled	Output Enabled	1
6		Reserved	Reserved	RW	-	-	1
5		Reserved	Reserved	RW	-	-	1
4		Reserved	Reserved	RW	-	-	1
3		Reserved	Reserved	RW	-	-	1
2		Reserved	Reserved	RW	-	-	1
1		Reserved	Reserved	RW	-	-	1
0		Reserved	Reserved	RW	-	-	1

Byte 3 Reserved Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	1
6		Reserved	Reserved	RW	-	-	1
5		Reserved	Reserved	RW	-	-	1
4		Reserved	Reserved	RW	-	-	1
3		Reserved	Reserved	RW	-	-	1
2		Reserved	Reserved	RW	-	-	1
1		Reserved	Reserved	RW			1
0		Reserved	Reserved	RW	-	-	1

Byte 4 Output and Spread Spectrum Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		CK_SSC_DISP_OE	Output enable for CK_SSC_DISP	RW	Output Disabled	Output Enabled	1
6		SATA/SRC1_OE	Output enable for SATA/SRC1	RW	Output Disabled	Output Enabled	1
5		SRC2_OE	Output enable for SRC2	RW	Output Disabled	Output Enabled	1
4		DOT96_OE	Output enable for DOT96	RW	Output Disabled	Output Enabled	1
3		Reserved	Reserved	RW	-	-	1
2		CPU0_OE	Output enable for CPU0	RW	Output Disabled	Output Enabled	1
1		PLL1_SSC_ON	Enable PLL1's spread modulation	RW	Spread Disabled	Spread Enabled	1
0		PLL3_SSC_ON	Enable PLL3's spread modulation	RW	Spread Disabled	Spread Enabled	1

Byte 5 Reserved Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	0
6		Reserved	Reserved	RW	-	-	0
5		Reserved	Reserved	RW	-	-	0
4		Reserved	Reserved	RW	-	-	0
3		Reserved	Reserved	RW	-	-	0
2		Reserved	Reserved	RW	-	-	0
1		Reserved	Reserved	RW	-	-	0
0		Reserved	Reserved	RW	-	-	0

Byte 6 Reserved Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	0
6		Reserved	Reserved	RW	-	-	0
5		Reserved	Reserved	RW	-	-	0
4		Reserved	Reserved	RW	-	-	0
3		Reserved	Reserved	RW	-	-	0
2		Reserved	Reserved	RW	-	-	0
1		Reserved	Reserved	RW	-	-	0
0		Reserved	Reserved	RW	-	-	0

Byte 7 Vendor ID/ Revision ID

Bit	Pin	Name	Description	Type	0	1	Default
7		Rev Code Bit 3	Revision ID	R	Vendor specific		X
6		Rev Code Bit 2		R			X
5		Rev Code Bit 1		R			X
4		Rev Code Bit 0		R			X
3		Vendor ID bit 3	Vendor ID ICS is 0001, binary	R			0
2		Vendor ID bit 2		R			0
1		Vendor ID bit 1		R			0
0		Vendor ID bit 0		R			1

Byte 8 Device ID and Output Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		**Device_ID3**	**Table of Device identifier codes, used for differentiating between CK505 package options, etc.**	**R**	**32-pin device**		**1**
6		**Device_ID2**		**R**			**0**
5		**Device_ID1**		**R**			**0**
4		**Device_ID0**		**R**			**0**
3		Reserved	Reserved	RW	-	-	0
2		Reserved	Reserved	RW	-	-	0
1		Reserved	Reserved	RW	-	-	0
0		Reserved	Reserved	RW	-	-	0

Byte 9 Amplitude Control Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	0
6		Reserved	Reserved	**R**	-	-	0
5		REF Strength	Sets the REF output drive strength	RW	1 Load	2 Loads	1
4		Reserved	Reserved	RW	-	-	0
3		Reserved	Reserved	RW	-	-	0
2		IO_VOUT2	IO Output Voltage Select (Most Significant Bit)	RW	See Table 2: V_IO Selection (Default is 0.8V)		1
1		IO_VOUT1	IO Output Voltage Select	RW			0
0		IO_VOUT0	IO Output Voltage Select (Least Significant Bit)	RW			1

Byte 10 Reserved Register

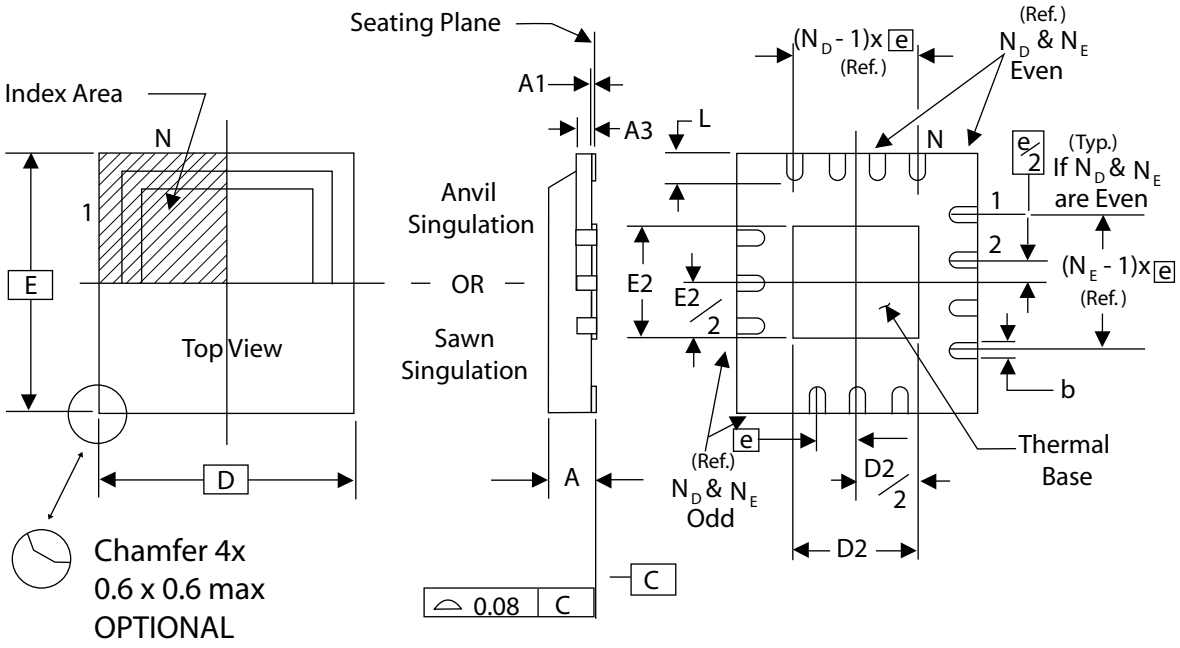
Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	0
6		Reserved	Reserved	RW	-	-	0
5		Reserved	Reserved	RW	-	-	0
4		Reserved	Reserved	RW	-	-	0
3		Reserved	Reserved	RW	-	-	0
2		Reserved	Reserved	RW	-	-	0
1		Reserved	Reserved	RW	-	-	1
0		Reserved	Reserved	RW	-	-	1

Byte 11 iAMT Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW			0
6		Reserved	Reserved	RW			0
5		Reserved	Reserved	RW			0
4		Reserved	Reserved	RW			1
3		Reserved	Reserved	RW	-	-	0
2		CPU0_AMT_EN	M1 mode clk enable	RW	Disable	Enable	1
1		PCI-E_GEN2	Determines if PCI-E Gen2 compliant	R	non-Gen2	PCI-E Gen2 Compliant	1
0		Reserved	Reserved	RW	-	-	1

Byte 12 Byte Count Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved		RW			0
6		Reserved		RW			0
5		BC5	Read Back byte count register, max bytes = 32	RW			0
4		BC4		RW			0
3		BC3		RW			1
2		BC2		RW			1
1		BC1		RW			0
0		BC0		RW			1



THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

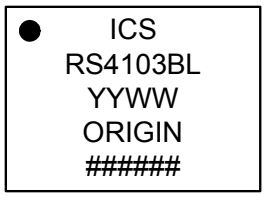
DIMENSIONS

SYMBOL	32L
N	32
N_D	8
N_E	8

DIMENSIONS (mm)

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	5.00 x 5.00	
D2 MIN. / MAX.	3.0	3.3
E2 MIN. / MAX.	3.0	3.3
L MIN. / MAX.	0.3	0.5

Marking Diagram



Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9LRS4103BKLF	Tray	32-pin MLF	0 to +70°C
9LRS4103BKLFT	Tape and Reel	32-pin MLF	0 to +70°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
"B" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Issue Date	WHO	Description	Page #
A	03/15/10	RDW	1. Updated electrical characteristics per char data 2. Added Table 4: Series Resistor values for REF 3. Corrected SMBus reference to REF strength. REF is 1 load/2load strength. 4. Release to final	Various
B	04/08/10	RDW	Update part ordering to "B" rev.	
C	12/09/10	RDW	Removed "Tubes" from ordering info; replaced with "Tray".	
D	01/06/11	RDW	1. Added test loads. 2. Updated electrical tables to include typical values and improved SRC cycle to cycle jitter spec from 125ps to 85ps. 3. Added phase jitter table for PCIe Gen2. 4. Revised text on front page 5. Corrected typographical errors.	Various

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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