Description

The 9FGV1002C / 9FGV1006C are members of the Renesas PhiClock™ programmable clock generator family. These devices are optimized for low phase noise spread-spectrum applications such as PCIe Express. The 9FGV1002C is a four-output device while the 9FGV1006C is a smaller two-output version. Four user-defined configurations may be selected via two hardware select pins or two I2C bits, allowing easy software selection of the desired configuration. Any one of the four OTP configurations may be specified as the default when operating in I2C mode. Four unique I2C addresses are available, allowing easy I2C access to multiple components.

Typical Applications

- High-performance Computing (HPC)
- Enterprise Storage including eSSDs
- 10G / 25G / 100G Ethernet
- Fiber Optic Modules
- NVLink

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference without spread spectrum (SRnS)
- Independent Reference with spread spectrum (SRIS)

Output Features

- 9FGV1002: 4 programmable output pairs plus 2 LVCMOS REF outputs
- 9FGV1006: 2 programmable output pairs plus 1 LVCMOS REF output
- 1 integer, fractional or spread spectrum output frequency per configuration
- 1MHz–325MHz LVDS or LP-HCSL outputs

Features

- 1.8V to 3.3V power supplies
- Individual 1.8V to 3.3V V_{DDO} for each output pair
- Supports HCSL, LVDS and LVCMOS I/O standards
- HCSL utilizes Renesas' LP-HCSL technology for improved performance, lower power and higher integration:
  - Programmable output impedance of 85Ω or 100Ω
- Supports LVPECL and CML logic with easy AC coupling – see application note AN-891 for alternate terminations
- On-board OTP supports up to 4 complete configurations
- Configuration selected via strapping pins or I^2C
- Internal crystal load capacitors
- < 125mW at 1.8V with LP-HCSL outputs at 100MHz (9FGV1002C)
- < 100mW at 1.8V with LP-HCSL outputs at 100MHz (9FGV1006C)
- 4 programmable I^2C addresses: D0, D2, D4, D6
- Easily configured with Renesas Timing Commander™ software or Web Configuration tool
- 4 × 4 mm 24-VFQFPN with integrated crystal option (9FGV1002CQ)
- 3 × 3 mm 16-LGA with integrated crystal option (9FGV1006CQ)
- Programmable spread spectrum modulation frequency and amount

Key Specifications

- 12kHz–20MHz typical phase jitter at 156.25M (SSC off) 276ps RMS
- PCIe Gen4 jitter (CC) < 0.23ps RMS
- PCIe Gen5 jitter (CC) < 0.08ps RMS
- PCIe Gen5 jitter (SRIS) < 0.07ps RMS

9FGV1002C / 9FGV1006C Block Diagram

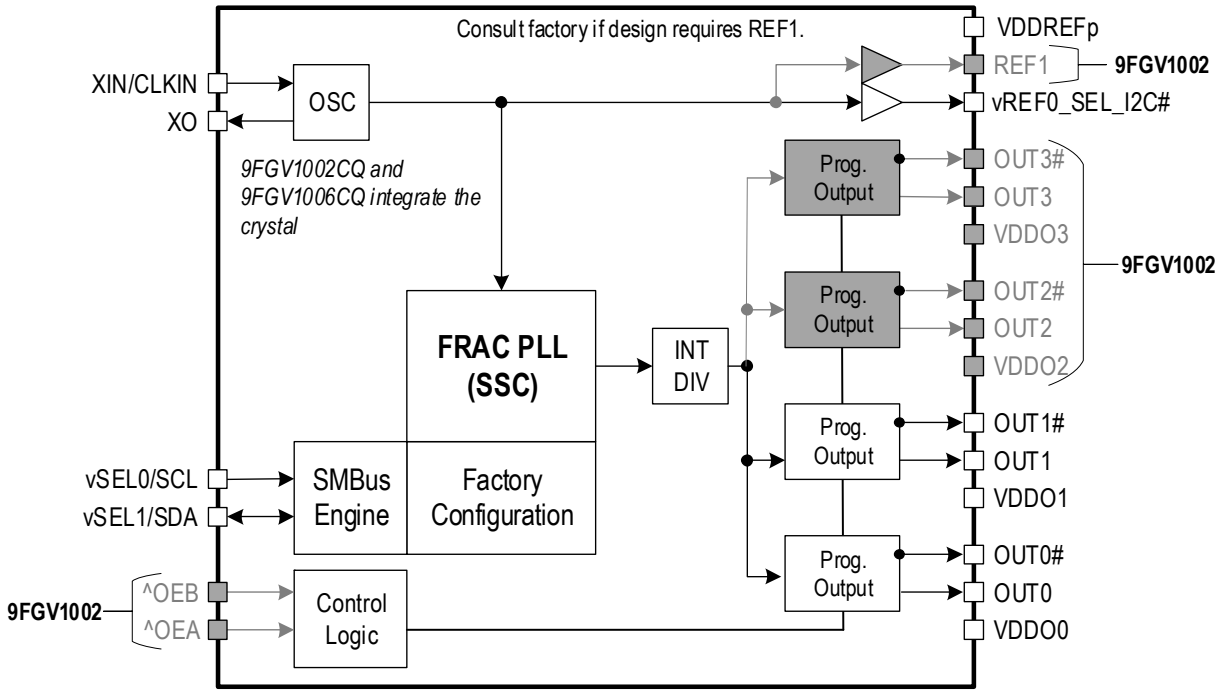


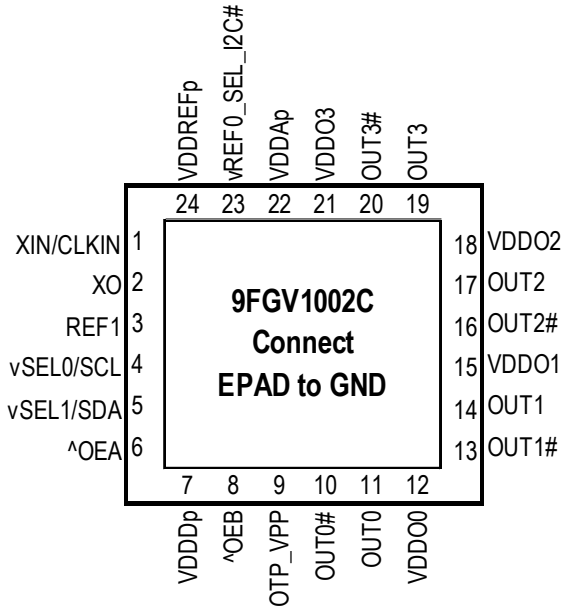
Table 1. OE Mapping

OE[B:A]	OUT0	OUT1	OUT2	OUT3	REF0	REF1
00	Running	Stopped	Stopped	Stopped	Running	Running
01	Running	Running	Stopped	Stopped	Running	Running
10	Running	Running	Running	Stopped	Running	Running
11	Running	Running	Running	Running	Running	Running

Contents

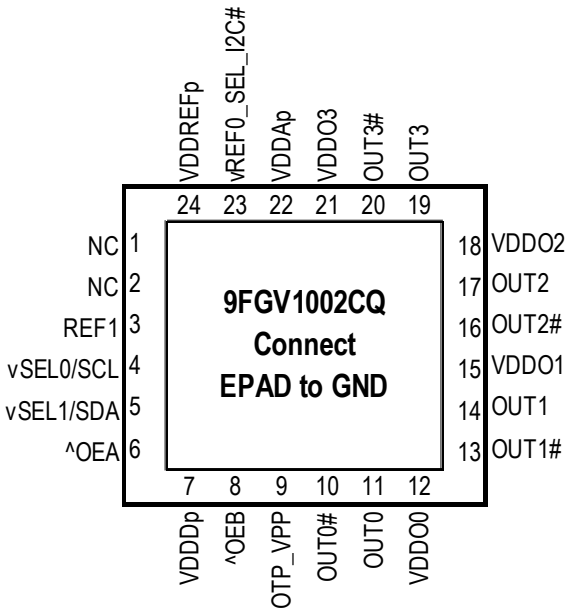
Pin Assignments

Figure 1. Pin Assignments for 9FGV1002C 4 x 4 mm 24-VFQFPN and 24-LGA Packages – Top View



4 × 4 mm 24-QFN, 0.5mm pitch

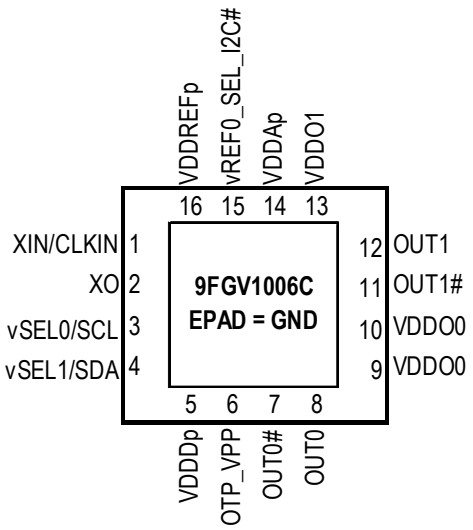
^ prefix indicates internal pull-up
v prefix indicates internal pull-down resistor
Note: The order of OUT3 is reversed from OUT[0:2]



4 × 4 mm 24-LGA, 0.5mm pitch

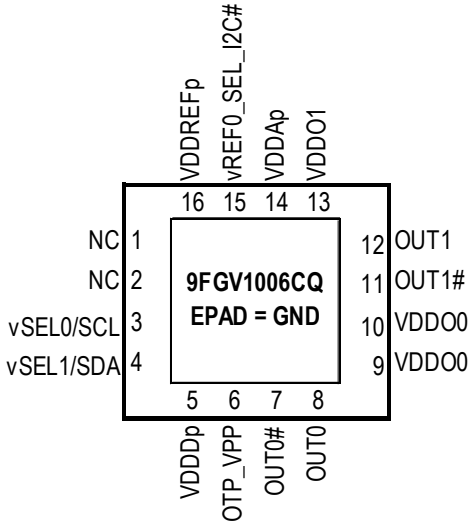
^ prefix indicates internal pull-up resistor
v prefix indicates internal pull-down resistor
Note: The order of OUT3 is reversed from OUT[0:2]

Figure 2. Pin Assignments for 9FGV1006C 3 x 3 mm 16-LGA Package – Top View



16-LGA 3 x 3 mm, 0.5mm pitch

^ prefix indicates internal pull-up resistor
v prefix indicates internal pull-down resistor



16-LGA 3 x 3 mm, 0.5mm pitch

^ prefix indicates internal pull-up resistor
v prefix indicates internal pull-down resistor

9FGV1002C Pin Descriptions

Note: Unused outputs can be programmed off and left floating. Output supplies V_{DDREF} and V_{DDO2} have to be connected. If OUT0 is used, V_{DDO1} must also be connected.

Table 2. 9FGV1002C Pin Descriptions

Number	Name	Type	Description
1[a]	XIN/CLKIN	Input	Crystal input or reference clock input.
2[a]	XO	Output	Crystal output.
3	REF1	Output	LVCMOS reference output.
4	vSEL0/SCL	Input	Select pin for internal frequency configurations/I^2C clock pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
5	vSEL1/SDA	I/O	Select pin for internal frequency configurations/I^2C data pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
6	^OEA	Input	Active high input for enabling outputs. This pin has an internal pull-up resistor. 0 = disable outputs, 1 = enable outputs.
7	VDDDp	Power	Digital power. Connect to 1.8V, 2.5V or 3.3V.
8	^OEB	Input	Active high input for enabling outputs. This pin has an internal pull-up resistor. 0 = disable outputs, 1 = enable outputs.
9	OTP_VPP	Power	Voltage for programming OTP. During normal operation, this pin should be connected to the same power rail as V_{DDD}.
10	OUT0#	Output	Complementary output clock 0.
11	OUT0	Output	Output clock 0.
12	VDDO0	Power	Power supply for output 0.
13	OUT1#	Output	Complementary output clock 1.
14	OUT1	Output	Output clock 1.
15	VDDO1	Power	Power supply for output 1.
16	OUT2#	Output	Complementary output clock 2.
17	OUT2	Output	Output clock 2.
18	VDDO2	Power	Power supply for output 2.
19	OUT3	Output	Output clock 3.
20	OUT3#	Output	Complementary output clock 3.
21	VDDO3	Power	Power supply for output 3.
22	VDDAp	Power	Analog power. Connect to same voltage as VDDDp, with proper filtering.
23	vREF0_SEL_I2C#	Latched I/O	Latched input/LVCMOS output. At power-up, the state of this pin is latched to select the state of the I^2C pins. After power-up, the pin acts as an LVCMOS reference output. This pin has an internal pull-down. 1 = SEL0/SEL1. 0 = SCL/SDA.
24	VDDREFp	Power	Power supply for REF outputs and the internal XO. Nominal voltages are 1.8V, 2.5V or 3.3V.
25	EPAD	GND	Connect to ground.

[a] These pins are 'No Connect' on 9FGV1002Q integrated quartz versions and should have no stubs.

9FGV1006C Pin Descriptions

Note: Unused outputs can be programmed off and left floating. Output supplies V_{DDREF} and V_{DDO1} have to be connected. This means that if only one output is to be used, it must be OUT1. If OUT0 is used, both pins 9 and 10 must be connected. They may share the same power filter.

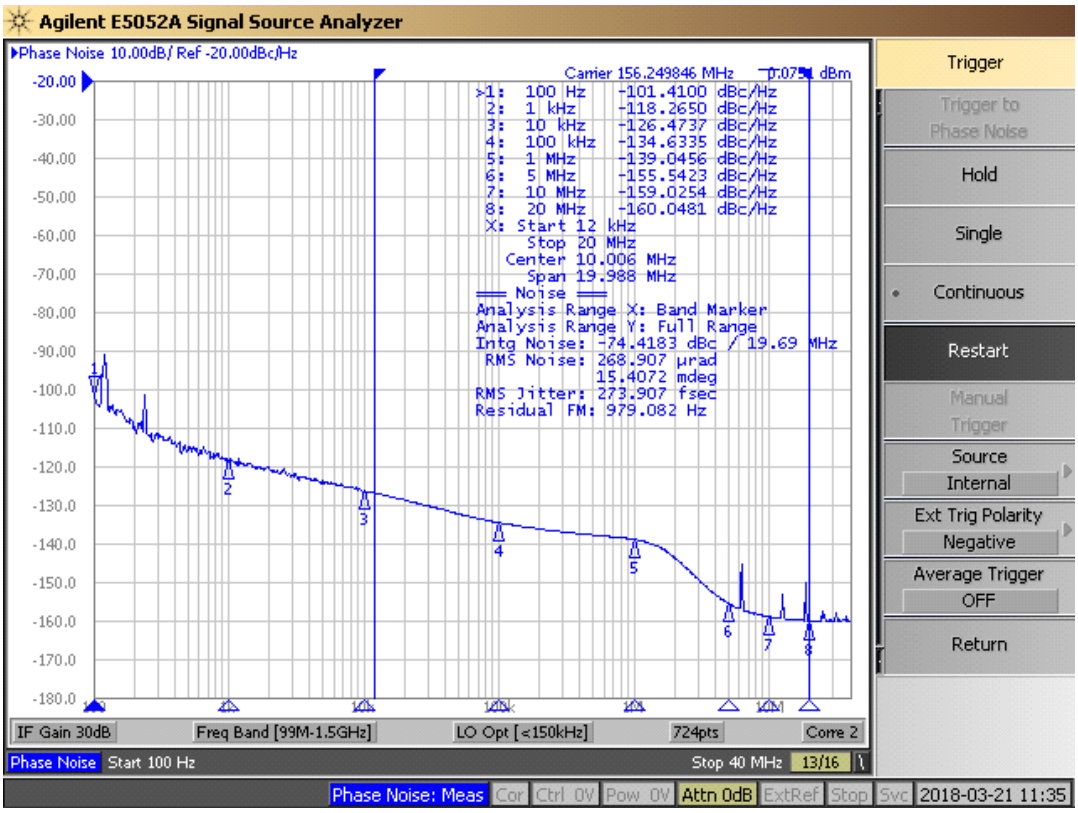
Table 3. 9FGV1006C Pin Descriptions

Number	Name	Type	Description
1[a]	XIN/CLKIN	Input	Crystal input or reference clock input.
2[a]	XO	Output	Crystal output.
3	vSEL0/SCL	Input	Select pin for internal frequency configurations/I^2C Clock pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
4	vSEL1/SDA	I/O	Select pin for internal frequency configurations/I^2C Data pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
5	VDDDp	Power	Digital power. Connect to 1.8V, 2.5V or 3.3V.
6	OTP_VPP	Power	Voltage for programming OTP. During normal operation, this pin should be connected to the same power rail as V_{DDD}.
7	OUT0#	Output	Complementary output clock 0.
8	OUT0	Output	Output clock 0.
9	VDDO0	Power	Power supply for output 0.
10	VDDO0	Power	Power supply for output 0.
11	OUT1#	Output	Complementary output clock 1.
12	OUT1	Output	Output clock 1.
13	VDDO1	Power	Power supply for output 1.
14	VDDAp	Power	Analog power. Connect to same voltage as VDDDp, with proper filtering.
15	vREF0_SEL_I2C#	Latched I/O	Latched input/LVCMOS output. At power-up, the state of this pin is latched to select the state of the I^2C pins. After power-up, the pin acts as an LVCMOS reference output. This pin has an internal pull-down. 1 = SEL0/SEL1. 0 = SCL/SDA.
16	VDDREFp	Power	Power supply for REF outputs and the internal XO. Nominal voltages are 1.8V, 2.5V or 3.3V.
17	EPAD	GND	Connect to ground.

[a] These pins are 'No Connect' on 9FGV1006Q integrated quartz version and should have no stubs.

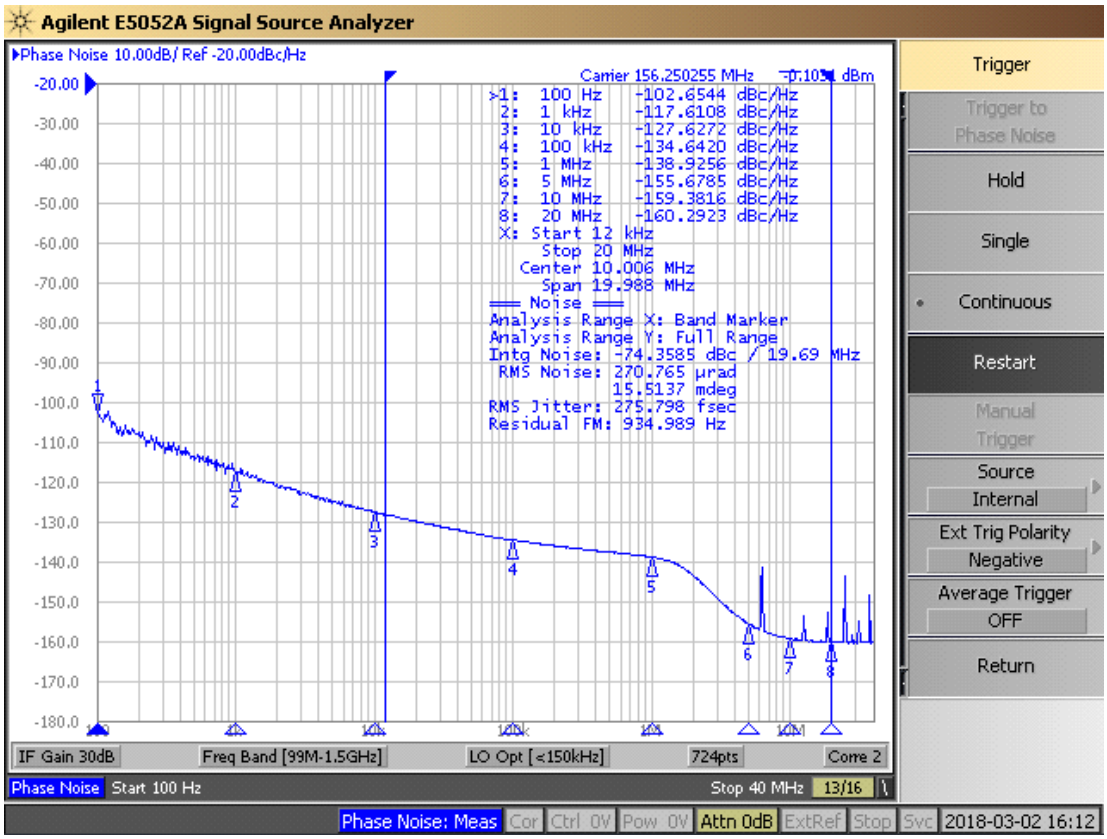
Phase Noise Plots

Figure 3. 9FGV1002C Phase Noise Plot[1], 3.3V, 25°C.



[1] See Test Frequencies for Jitter Measurements table for details.

Figure 4. 9FGV1006C Phase Noise Plot[1], 3.3V, 25°C.



[1] See Test Frequencies for Jitter Measurements table for details.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9FGV1002C / 9FGV1006C at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 4. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage, V_{DDA}, V_{DDD}, V_{DDO}	3.9V
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Human Body Model	2000V
Junction Temperature	125°C
Inputs	
XIN/CLKIN	0V to 1.2V voltage swing
Other Inputs	-0.5V to V_{DDD}
Outputs	
Outputs, V_{DDO} (LVCMOS)	-0.5V to V_{DDO} + 0.5V
Outputs, IO (SDA)	10mA

Thermal Characteristics

Table 5. Thermal Characteristics for 24-pin Devices

Parameter	Symbol	Conditions	Package	Typical Values	Units	Notes
Thermal Resistance (devices with external crystal)	θ_{JC}	Junction to case.	NBG24	52	°C/W	1
	θ_{Jb}	Junction to base.		2.3	°C/W	1
	θ_{JA0}	Junction to air, still air.		44	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		37	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		33	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow.		32	°C/W	1
Thermal Resistance Q-series (devices with internal crystal)	θ_{JC}	Junction to case.	LTG24	57.3	°C/W	1
	θ_{Jb}	Junction to base.		24.3	°C/W	1
	θ_{JA0}	Junction to air, still air.		79.8	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		73.9	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		69.9	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow.		67.3	°C/W	1

[1] EPAD soldered to board.

Table 6. Thermal Characteristics for 16-pin devices

Parameter	Symbol	Conditions	Package	Typical Values	Units	Notes
Thermal Resistance (devices with external crystal)	θ_{JC}	Junction to case.	LTG16	66	°C/W	1
	θ_{Jb}	Junction to base.		5.1	°C/W	1
	θ_{JA0}	Junction to air, still air.		63	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		56	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		51	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow.		49	°C/W	1
Thermal Resistance Q-series (devices with internal crystal)	θ_{JC}	Junction to case.	LTG16	82.1	°C/W	1
	θ_{Jb}	Junction to base.		42.3	°C/W	1
	θ_{JA0}	Junction to air, still air.		93.6	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		87.1	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		83.3	°C/W	1

[1] EPAD soldered to board.

Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DDOx}	Power supply voltage for supporting 1.8V outputs.	1.71	1.8	1.89	V
	Power supply voltage for supporting 2.5V outputs.	2.375	2.5	2.625	V
	Power supply voltage for supporting 3.3V outputs.	3.135	3.3	3.465	V
V_{DDD}	Power supply voltage for core logic functions.	1.71		3.465	V
V_{DDA}	Analog power supply voltage. Use filtered analog power supply if available.	1.71		3.465	V
T_A	Operating temperature, ambient.	-40		85	°C
C_L	Maximum load capacitance (3.3V LVCMOS only).			15	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic).	0.05		5	ms

Electrical Characteristics

V_{DDx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C unless stated otherwise.

Table 8. Common Electrical Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Frequency	f_{IN}	Crystal input frequency.	8		50	MHz	1
		CLKIN input frequency.	1		240	MHz	5
Output Frequency	f_{OUT}	Differential clock output (LVDS/LP-HCSL).	1		325	MHz	
		Single-ended clock output (LVCMOS).	1		200	MHz	
VCO Frequency	f_{VCO}	VCO operating frequency range.	2400	2500	2600	MHz	
Loop Bandwidth	f_{BW}	Input frequency = 25MHz.	0.06		0.9	MHz	
Input High Voltage	V_{IH}	SEL[1:0].	0.7 x V_{DDD}		V_{DDD} + 0.3	V	
Input Low Voltage	V_{IL}	SEL[1:0].	GND - 0.3		0.8	V	
Input High Voltage	V_{IH}	REF/SEL_I2C#.	0.65 x V_{DDREF}		V_{DDREF} + 0.3	V	
Input Low Voltage	V_{IL}	REF/SEL_I2C#.	-0.3		0.4	V	
Input High Voltage	V_{IH}	XIN/CLKIN.	0.8		1.2	V	
Input Low Voltage	V_{IL}	XIN/CLKIN.	-0.3		0.4	V	
Input Rise/Fall Time	T_R/T_F	OEA, OEB (when present)			10	ns	
		SEL1/SDA, SEL0/SCL			300		
Input Capacitance	C_{IN}	SEL[1:0].		3	7	pF	
Internal Pull-up Resistor	R_{UP}		200	237	300	kΩ	
Internal Pull-down Resistor	R_{DOWN}		200	237	300	kΩ	
Programmable Capacitance at XIN and XO (XIN in parallel with XO)	C_L	XIN/CLKIN, XO.	0		8	pF	
Input Duty Cycle	t2	CLKIN, measured at V_{DDREF}/2.	40	50	60	%	
Output Duty Cycle	t3	LVCMOS, f_{OUT} > 156.25MHz.	40	50	60	%	
		LVCMOS, $f_{OUT} \leq$ 156.25MHz.	45	50	55	%	
		LVDS, LP-HCSL outputs.	45	50.2	55	%	
Clock Jitter	t6	Cycle-to-cycle jitter (Peak-to-Peak), See Test Frequencies for Jitter Measurements for configurations.		24		ps	4
		Reference clock RMS phase jitter (12kHz to 20MHz integration range). See Test Frequencies for Jitter Measurements for configurations.		245		fs rms	4
		OUTx RMS phase jitter(12kHz to 20MHz integration range) differential output. See Test Frequencies for Jitter Measurements for configurations.		276		fs rms	4

Table 8. Common Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Output Skew	t7	All outputs using the same driver format same V_{DDO} voltage. (9FGV1006C).		38	60	ps	
		All outputs using the same driver format and same V_{DDO} voltage. (9FGV1002C).		62	100		
Lock Time	t8a	PLL outputs valid from V_{DD}s reaching 1.5V.		5	10	ms	2,3
	t8b	REF outputs valid from V_{DD}s reaching 1.5V.		5	11	ms	2,3

[1] Practical lower frequency is determined by loop filter settings.

[2] Includes loading the configuration bits from OTP to registers.

[3] Actual PLL lock time depends on the loop configuration.

[4] Actual jitter is configuration dependent. These values are representative of what the device can achieve.

[5] Input doubler off. Maximum input frequency with input doubler on is 160MHz.

Table 9. Test Frequencies for Jitter Measurements

V_{DDx} = 3.3V±5%, 2.5V±5%, 1.8V±5%, T_A = -40°C to +85°C unless stated otherwise

XIN/CLKIN	OUT0	OUT1	OUT2	OUT3	Unit	Notes
50	156.25				MHZ	3,4
	100				MHZ	1,2,3

[1] This configuration is used for 12kHz–20MHz REF phase jitter measurement, SSC off.

[2] This configuration is used for PCIe filtered phase jitter measurements with SSC on and off.

[3] Outputs configured as LP-HCSL or LVDS with REF output off, unless noted.

[4] This configuration is used for 12kHz–20MHz OUT phase jitter measurement. REF off, SSC off.

Table 10. LVCMOS Output Electrical Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Slew Rate	S_R	3.3V ±5%, 20% to 80% of V_{DDO} (output load = 4.7pF).	2.6	3.7	4.7	V/ns	
		2.5V ±5%, 20% to 80% of V_{DDO} (output load = 4.7pF).	1.5	2.4	4.7		
		1.8V ±5%, 20% to 80% of V_{DDO} (output load = 4.7pF).	1.0	1.7	3.2		
Output High Voltage	V_{OH}	I_{OH} = -15mA at 3.3V.	0.8 x V_{DDO}		V_{DDO}	V	
		I_{OH} = -12mA at 2.5V.					
		I_{OH} = -8mA at 1.8V.					

Table 10. LVCMOS Output Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Output Low Voltage	V_{OL}	I_{OL} = 15mA at 3.3V.		0.22	0.4	V	
		I_{OL} = 12mA at 2.5V.					
		I_{OL} = 8mA at 1.8V.					
Output Leakage Current	I_{OZDD}	Outputs, tri-stated, V_{DDO}, V_{DDREF} = 3.465V.		0	5	µA	
CMOS Output Driver Impedance	R_{OUT}	T_A = 25°C.		17		Ω	

Table 11. LVDS Output Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Differential Output Voltage for the TRUE Binary State	V_{OT} (+)	247	328	454	mV	
Differential Output Voltage for the FALSE Binary State	V_{OT} (-)	-454	-332	-247	mV	
Change in V_{OT} between Complementary Output States	ΔV_{OT}			50	mV	
Output Common Mode Voltage (Offset Voltage) at 3.3V +5% and 2.5V +5%	V_{OS}	1.125	1.19	1.55	V	
Output Common Mode Voltage (Offset Voltage) at 1.8V +5%	V_{OS}	0.8	0.86	0.95	V	
Change in V_{OS} between Complementary Output States	ΔV_{OS}		0	50	mV	
Outputs Short Circuit Current, V_{OUT}+ or V_{OUT}- = 0V or V_{DD}	I_{OS}		6	12	mA	
Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT}-	I_{OSD}		3	12	mA	
Rise Times Tested at 20%–80%	T_R		257	375	ps	
Fall Times Tested at 80%–20%	T_F		287	375	ps	

Table 12. Low-Power (LP) Push-Pull HCSL Differential Outputs

V_{DDO} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C unless stated otherwise.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Slew Rate	$T_{R/F}$	Scope averaging on.	1.25	2.5	4	V/ns	2,3,16
Slew Rate Matching	$\Delta T_{R/F}$			9	20	%	1,14,16
Crossing Voltage (abs)	V_{CROSS}	Scope averaging off.	250	424	550	mV	1,4,5,16
Crossing Voltage (var)	ΔV_{CROSS}	Scope averaging off.		16	140	mV	1,4,9,16
Average Clock Period Accuracy	T_{PERIOD_AVG}	Outputs set to 100MHz for PCIe applications.	-100	0	+2600		2,10,12,13
Absolute Period	T_{PERIOD_ABS}	Includes jitter and spread modulation.	9.949	10	10.101		2,6
Absolute Maximum Voltage	V_{MAX}	Includes 300mV of overshoot (Vovs).	660	808	1150	mV	1,7,15
Absolute Minimum Voltage	V_{MIN}	Includes -300mV of undershoot (Vuds).	-300	-54	150	mV	1,8,15

[1] Measured from single-ended waveform.

[2] Measured from differential waveform.

[3] Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

[4] Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

[5] Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

[6] Defined as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation.

[7] Defined as the maximum instantaneous voltage including overshoot.

[8] Defined as the minimum instantaneous voltage including undershoot.

[9] Defined as the total variation of all crossing voltages of rising REFCLK+ and falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system.

[10] Refer to Section 8.6 of the PCI Express Base Specification, Revision 4.0 for information regarding PPM considerations.

[11] System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load C_L = 2pF.

[12] PCIe Gen1 through Gen4 specify ±300ppm frequency tolerances. The PhiClock devices already meet the tighter ±100ppm frequency tolerances proposed for PCIe Gen5 and required by most servers.

[13] "ppm" refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100ppm, then we have an error budget of 100Hz/ppm × 100ppm = 10kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±100ppm applies to systems that do not employ Spread Spectrum clocking, or that use common clock source. For systems employing Spread Spectrum Clocking, there is an additional 2,500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600ppm for Common Clock architectures. Separate Reference Clock architectures may have a lower allowed spread percentage.

[14] Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of REFCLK+ should be compared to the fall edge rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

[15] At default amplitude settings.

[16] Guaranteed by design and characterization.

Table 13. Filtered PCIe Phase Jitter Parameters

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limits	Units	Notes
PCIe Phase Jitter[7] (Common Clocked Architecture)	$t_{jphPCIeG1-CC}$	PCIe Gen1 (2.5 GT/s) SSC ≤ -0.5%	0.28	6.80	24	86	ps (p-p)	1,2
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Hi Band (5.0 GT/s) SSC ≤ -0.5%	0.11	0.36	0.64	3	ps (rms)	1,2
		PCIe Gen2 Lo Band (5.0 GT/s) SSC ≤ -0.5%	0.00	0.02	0.07	3.1	ps (rms)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (8.0 GT/s) SSC ≤ -0.5%	0.03	0.13	0.23	1	ps (rms)	1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (16.0 GT/s) SSC ≤ -0.5%	0.03	0.13	0.23	0.5	ps (rms)	1,2,3,4
	$t_{jphPCIeG5-CC}$	PCIe Gen5 (32.0 GT/s) SSC ≤ -0.5%	0.01	0.04	0.083	0.15	ps (rms)	1,2,3,5
PCIe Phase Jitter[7] (SRIS Architecture)	$t_{jphPCIeG2-SRIS}$	PCIe Gen2 (5.0 GT/s) SSC ≤ -0.3%	0.29	0.39	0.505	N/A	ps (rms)	1,2,6
	$t_{jphPCIeG3-SRIS}$	PCIe Gen3 (8.0 GT/s) SSC ≤ -0.3%	0.09	0.19	0.273		ps (rms)	1,2,6
	$t_{jphPCIeG4-SRIS}$	PCIe Gen4 (16.0 GT/s) SSC ≤ -0.3%	0.10	0.14	0.184		ps (rms)	1,2,6
	$t_{jphPCIeG5-SRIS}$	PCIe Gen5 (32.0 GT/s) SSC ≤ -0.3%	0.03	0.05	0.071		ps (rms)	1,2,6

[1] The REFCLK jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.

[2] Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

[3] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

[4] Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

[5] Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

[6] While the PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. SRIS is not defined for PCIe Gen1.

[7] 9FGV1002C or 9FGV1006C with 001/015 or Q505/Q515 configurations. See the 9FGV1002C/9FGV1006C Standard Configurations table for details and a selection of off-the-shelf configurations supporting PCIe Gen5.

Table 14. 9FGV1002C Current Consumption

V_{DDO} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C unless stated otherwise.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
V_{DDREF} Supply Current	I_{DDREF}	50MHz REFCL, subtract 3mA for 25MHz REFCLK.		7	11	mA	
Core Supply Current	I_{DDCORE}	2400MHz VCO.		37	49	mA	3
Output Buffer Supply Current V_{DDO3}	I_{DDOx}	LVDS, 325MHz.		7	9	mA	2
		LP-HCSL, 100MHz.		6	7	mA	2
		LVCMOS, 50MHz.		4	6	mA	1,2
		LVCMOS, 200MHz.		12	21	mA	1,2
Output Buffer Supply Current V_{DDO2} (includes output divider)		LVDS, 325MHz.		19	24	mA	2
		LP-HCSL, 100MHz.		16	20	mA	2
		LVCMOS, 50MHz.		14	18	mA	1,2
		LVCMOS, 200MHz.		23	35	mA	1,2
Output Buffer Supply Current V_{DDO1} (this pin must be connected if OUT0 is used)		LVDS, 325MHz.		7	10	mA	2
		LP-HCSL, 100MHz.		7	10	mA	2
		LVCMOS, 50MHz.		8	14	mA	1,2
		LVCMOS, 200MHz.		9	15	mA	1,2
Output Buffer Supply Current V_{DDO0}		LVDS, 325MHz.		6	9	mA	2
		LP-HCSL, 100MHz.		5	7	mA	2
		LVCMOS, 50MHz.		3	6	mA	1,2
		LVCMOS, 200MHz.		12	22	mA	1,2
Total Power Down Current	I_{DDPD}	Programmable outputs in HCSL mode, B37[0] = 0.		20	27	mA	2
		Programmable outputs in LVDS mode, B37[0] = 0.		33	45	mA	2
		Programmable outputs in LVCMOS1 mode, B37[0] = 0.		16	22	mA	2

[1] Single CMOS driver active for each output pair.

[2] See Test Loads for details.

[3] $I_{DDCORE} = I_{DDA} + I_{DDD}$. For integer, fractional or spread spectrum PLL.

Table 15. 9FGV1006C Current Consumption

V_{DDO} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C unless stated otherwise.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
V_{DDREF} Supply Current	I_{DDREF}	50MHz REFCLK.		3	7	mA	
Core Supply Current	I_{DDCORE}	2400MHz VCO.		37	48	mA	3
Output Buffer Supply Current (V_{DDO1})	I_{DDOx}	LVDS, 350MHz.		19	24	mA	2
		LP-HCSL, 100MHz.		16	20	mA	2
		LVCMOS, 50MHz.		14	19	mA	1,2
		LVCMOS, 200MHz.		22	34	mA	1,2
Output Buffer Supply Current (V_{DDO0} – the total for pins 9 and 10)		LVDS, 350MHz.		7	11	mA	2
		LP-HCSL, 100MHz.		8	10	mA	2
		LVCMOS, 50MHz.		8	13	mA	1,2
		LVCMOS, 200MHz.		8	14	mA	1,2
Total Power Down Current	I_{DDPD}	Programmable outputs in HCSL mode, B37[0] = 0.		19	25	mA	2
		Programmable outputs in LVDS mode, B37[0] = 0.		25	34	mA	2
		Programmable outputs in LVCMOS1 mode, B37[0] = 0.		16	22	mA	2

[1] Single CMOS driver active for each output pair.

[2] See Test Loads for details.

[3] $I_{DDCORE} = I_{DDA} + I_{DDD} + I_{DDAO}$.

Table 16. Spread Spectrum Generation Specifications

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Mod Frequency	$f_{MODPCIe}$	PCIe Compliant -0.5% spread modulation.	30	31.5	33	kHz
Mod Frequency	f_{MOD}	Modulation frequency.	30	31.5	63	kHz
Spread%	SSC%	Amount of spread value (programmable) – down spread.	-0.1	-0.5	-3.0	%
		Amount of spread value (programmable) – center spread.	±0.05		±1.5	

I²C Bus Characteristics

Table 17. I²C Bus DC Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Input High Level	V_{IH}	—	0.7 x V_{DDD}			V
Input Low Level	V_{IL}	—			0.3 x V_{DDD}	V
Hysteresis of Inputs	V_{HYS}	—	0.05 x V_{DDD}			V
Input Leakage Current	I_{IN}	—	-1		30	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA.			0.4	V

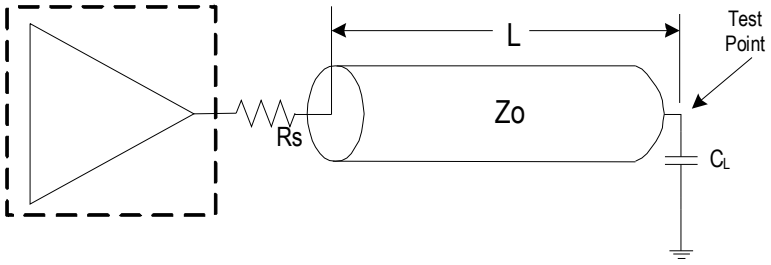
Table 18. I²C Bus AC Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Serial Clock Frequency (SCL)	F_{SCLK}	—	10		400	kHz
Bus free time between STOP and START	t_{BUF}	—	1.3			µs
Setup Time, START	$t_{SU:START}$	—	0.6			µs
Hold Time, START	$t_{HD:START}$	—	0.6			µs
Setup Time, Data Input (SDA)	$t_{SU:DATA}$	—	0.1			µs
Hold Time, Data Input (SDA) 1	$t_{HD:DATA}$	—	0			µs
Output Data Valid from Clock	t_{OVD}	—			0.9	µs
Capacitive Load for Each Bus Line	C_B	—			400	pF
Rise Time, Data and Clock (SDA, SCL)	t_R	—	20 + 0.1 x C_B		300	ns
Fall Time, Data and Clock (SDA, SCL)	t_F	—	20 + 0.1 x C_B		300	ns
HIGH Time, Clock (SCL)	t_{HIGH}	—	0.6			µs
LOW Time, Clock (SCL)	t_{LOW}	—	1.3			µs
Setup Time, STOP	$t_{SU:STOP}$	—	0.6			µs

Note: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Test Loads

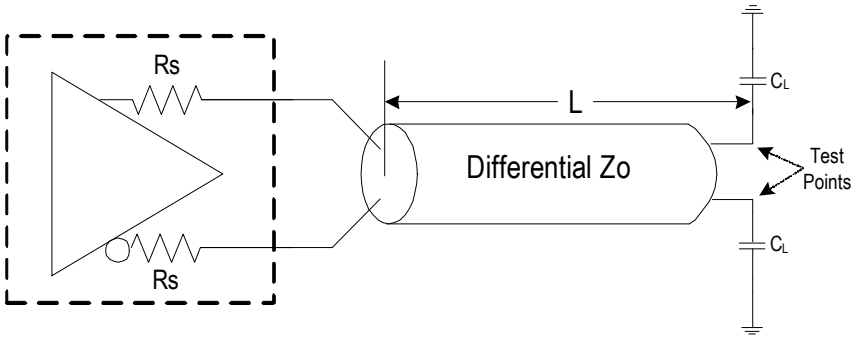
Figure 5. LVCMOS AC/DC Test Load



Rs	Zo	L	C_L
33Ω	50Ω	5 inches	4.7pF

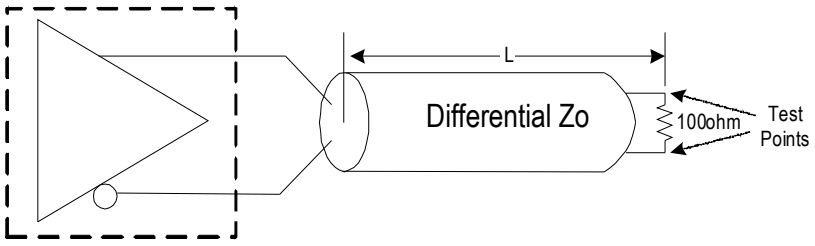
Figure 6. LP-HCSL AC/DC Test Load

(Standard PCIe source-terminated test load)



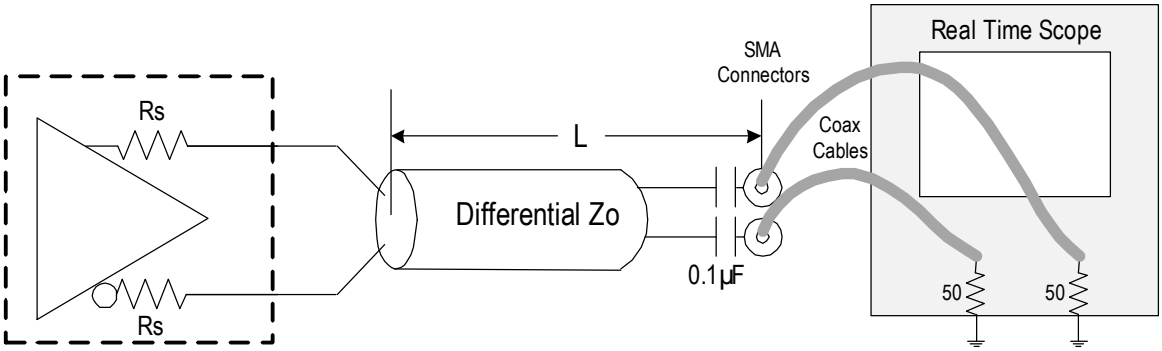
Rs	Zo	L	C_L
Internal	100Ω	5 inches	2pF
Internal	85Ω	5 inches	2pF

Figure 7. LVDS AC/DC Test Load



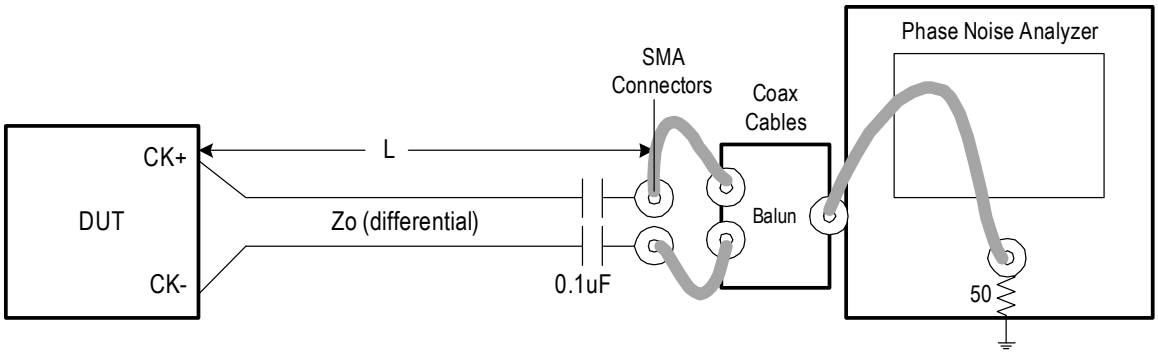
Rs	Zo	L	C_L
N/A	100Ω	5 inches	N/A

Figure 8. Test Setup for PCIe Measurement Using a Real-Time Scope



Rs	Zo	L	C_L
Internal	100Ω	5 inches	N/A

Figure 9. Test Setup for PCIe Measurement Using a Phase Noise Analyzer



Rs	Zo	L	C_L
Internal	100Ω	5 inches	N/A

Crystal Characteristics

Table 19. Recommended Crystal Characteristics

Parameter	Value	Units
Frequency	8–50	MHz
Resonance Mode	Fundamental	–
Frequency Tolerance at 25°C	±20	ppm maximum
Frequency Stability, REF at 25°C Over Operating Temperature Range	±20	ppm maximum
Temperature Range (commercial)	0–70	°C
Temperature Range (industrial)	-40–85	°C
Equivalent Series Resistance (ESR)	50	Ω maximum
Shunt Capacitance (C_O)	7	pF maximum
Load Capacitance (C_L)	8	pF maximum
Drive Level	0.1	mW maximum
Aging Per Year	±5	ppm maximum

Package Outline Drawings

The package outline drawings are appended at the end of this document and are also accessible from the link below. The package information is the most current data available and is subject to change without notice or revision of this document.

9FGV1002C:

www.idt.com/document/psc/24-vfqfpn-package-outline-drawing-40-x-40-x-075-mm-body-05mm-pitch-epad-26-x-26-mm-nbnbg24p2

www.idt.com/document/psc/24-lga-package-outline-drawing-40-x-40-x-140-mm-body-05mm-pitch-ltg24t2

9FGV1006C:

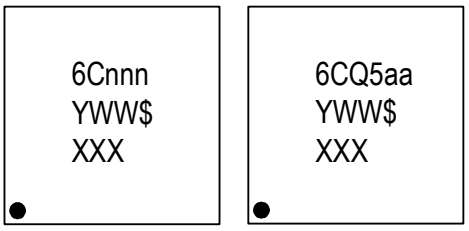
www.idt.com/document/psc/16-lga-package-outline-drawing-30-x-30-x-110-mm-body-05mm-pitch-ltg16p1

Marking Diagrams

Figure 10. 9FGV1002C Marking Diagrams

- Lines 1 and 2 are the truncated part number:
  - “nnn” denotes the decimal digits indicating a specific configuration.
  - “aa” denotes the alphanumeric digits indicating a specific Q5 configuration.
- Line 3:
  - “#” denotes the stepping number.
  - “YWW” denotes the last digits of the year and week the part was assembled.
  - “**” denotes the lot sequence; “$” denotes the mark code.

Figure 11. 9FGV1006C Marking Diagrams



- Line 1: truncated part number
  - "nnn" denotes the decimal digits indicating a specific configuration.
  - "aa" denotes the alphanumeric digits indicating a specific Q5 configuration.
- Line 2: "YWW" denotes the last digits of the year and week the part was assembled; "$" denotes mark code.
- Line 3: "XXX" denotes the last three characters of the lot number.

Standard Configurations

Table 20. 9FGV1002C/9FGV1006C Standard Configurations

Supply Voltage–all pins (V)	Output Impedance (ohms)	Number of PCIe Clock Outputs	XTAL Frequency (MHz)	Orderable Part Number (Bulk)	Orderable Part Number (Tape and Reel)
3.3	100	4	25 – external	9FGV1002C001NBGI	9FGV1002C001NBGI8
			50 – internal	9FGV1002CQ505LTGI	9FGV1002CQ505LTGI8
		2	25 – external	9FGV1006C001LTGI	9FGV1006C001LTGI8
			50 – internal	9FGV1006CQ505LTGI	9FGV1006CQ505LTGI8
	85	4	25 – external	9FGV1002C015NBGI	9FGV1002C015NBGI8
			50 – internal	9FGV1002CQ515LTGI	9FGV1002CQ515LTGI8
		2	25 – external	9FGV1006C015LTGI	9FGV1006C015LTGI8
			50 – internal	9FGV1006CQ515LTGI	9FGV1006CQ515LTGI8
1.8	100	4	25 – external	9FGV1002C002NBGI	9FGV1002C002NBGI8
			50 – internal	9FGV1002CQ506LTGI	9FGV1002CQ506LTGI8
		2	25 – external	9FGV1006C002LTGI	9FGV1006C002LTGI8
			50 – internal	9FGV1006CQ506LTGI	9FGV1006CQ506LTGI8

Table 21. Common Features of 9FGV1002C/9FGV1006C Standard Configurations

Output Freq (MHz)	Output Type	REF Outputs	Configuration	SSC amount (%)	Notes
100	LP-HCSL	Off	0	0	CC, SRNS
			1	-0.1	CC, SRIS
			2	-0.3	CC, SRIS
			3	-0.5	CC

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature	Crystal
9FGV1002CnnnNBGI	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Tray	-40 to +85°C	External
9FGV1002CnnnNBGI8	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Tape and Reel	-40 to +85°C	External
9FGV1002CQ5aaLTGI	4 × 4 mm, 0.5mm pitch 24-LGA	Tray	-40 to +85°C	50MHz Internal
9FGV1002CQ5aaLTGI8	4 × 4 mm, 0.5mm pitch 24-LGA	Tape and Reel	-40 to +85°C	50MHz Internal
9FGV1006CnnnLTGI	3 × 3 mm, 0.5mm pitch 16-LGA	Tray	-40 to +85°C	External
9FGV1006CnnnLTGI8	3 × 3 mm, 0.5mm pitch 16-LGA	Tape and Reel	-40 to +85°C	External
9FGV1006CQ5aaLTGI	3 × 3 mm, 0.5mm pitch 16-LGA	Tray	-40 to +85°C	50MHz Internal
9FGV1006CQ5aaLTGI8	3 × 3 mm, 0.5mm pitch 16-LGA	Tape and Reel	-40 to +85°C	50MHz Internal

"G" indicates RoHS 6.6 compliance.

"nnn" are decimal digits indicating a specific configuration.

"aa" are alphanumeric digits indicating a specific configuration.

"Q5" indicates internal 50MHz crystal.

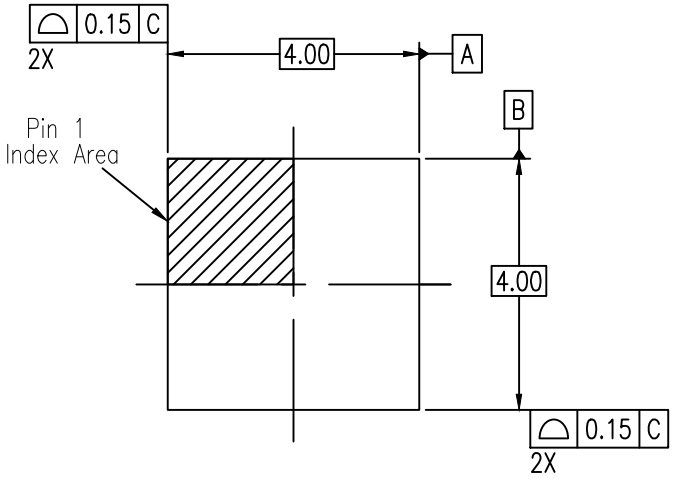
Revision History

Revision Date	Description of Change
November 30, 2020	Removed "Output Frequency" parameter from Spread Spectrum Generation Specifications table.
October 29, 2020	Updated pin descriptions for VDDAp and VDDDp.
October 9, 2020	Added a condition and values for REF outputs to the Lock Time parameter.
September 28, 2020	Removed "PCIe Gen5' from the standard configuration tables titles and the relative heading title.
August 18, 2020	Updated 9FGV1006CQ marking diagram.
August 14, 2020	Updated Slew Rate 1.8V minimum value from 0.8 to 1.0V/ns.
August 13, 2020	Updated Carrier Type in Ordering Information table from "Cut-Tape" to "Tray".
July 16, 2020	Corrected internal resistors on SEL0/SCL and SEL1/SDA to be pull-downs.
July 10, 2020	Initial release.

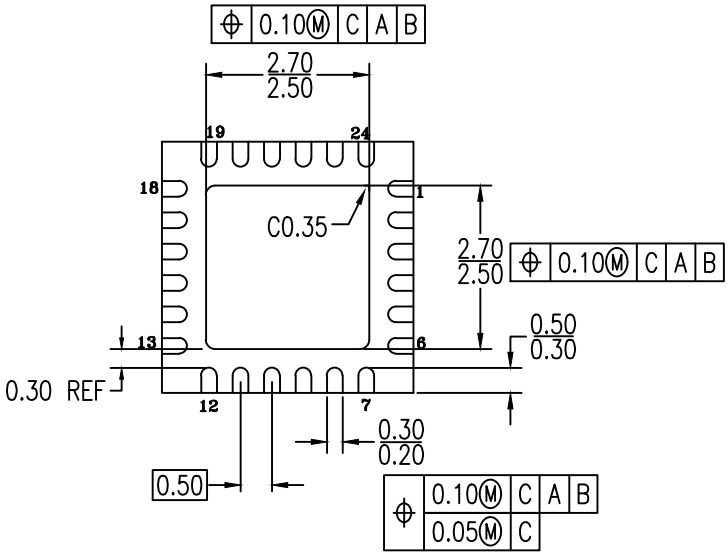
24-VFQFPN, Package Outline Drawing

4.0 x 4.0 x 0.75 mm Body, 0.5mm Pitch, Epad 2.6 x 2.6 mm

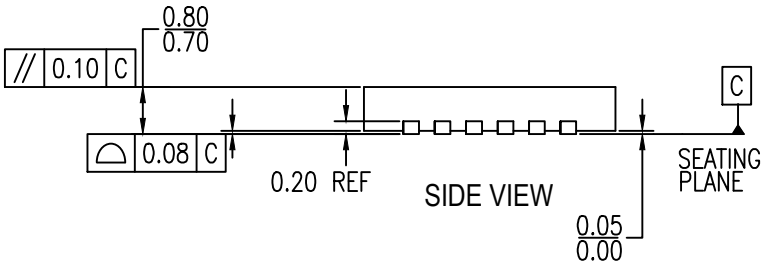
NB/NBG24P2, PSC-4313-02, Rev 01, Page 1



TOP VIEW



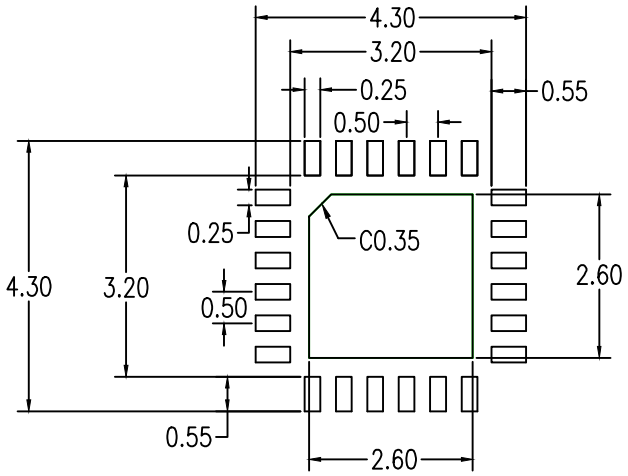
BOTTOM VIEW



SIDE VIEW

NOTES:

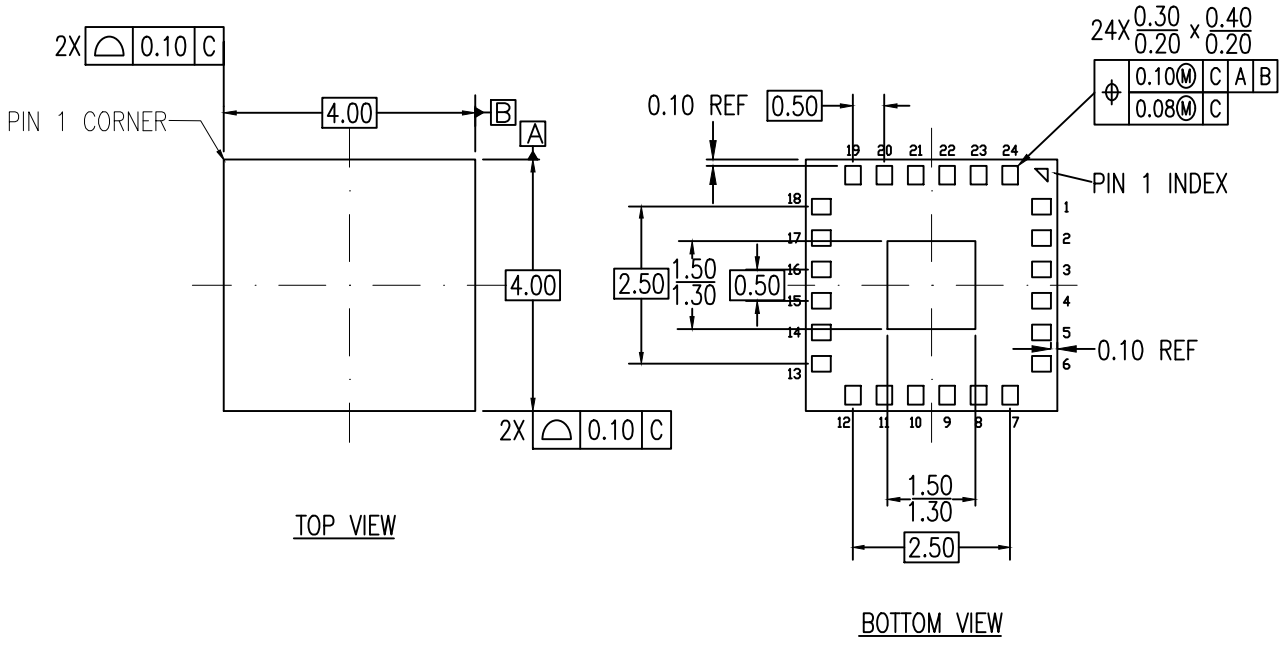
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1994
2. ALL DIMENSONS ARE IN MILLIMETERS
3. INDEX AREA PIN 1 IDENTIFIER

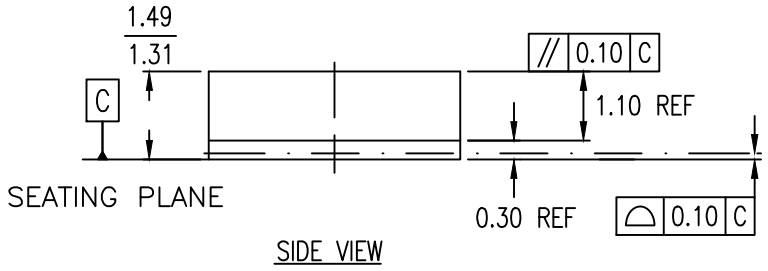


RECOMMENDED LAND PATTERN DIMENSION

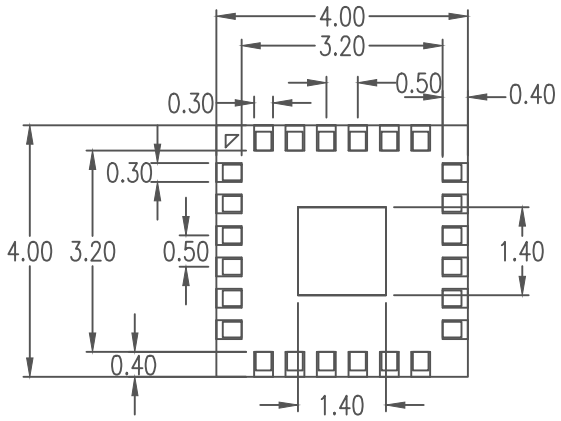
NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1994
2. ALL DIMENSONS ARE IN MILLIMETERS
3. LAND PATTERN RECOMMENDATION PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Jan 24, 2018	Rev 01	Change QFN to VFQFPN and New Format
May 11, 2016	Rev 00	Initial Release





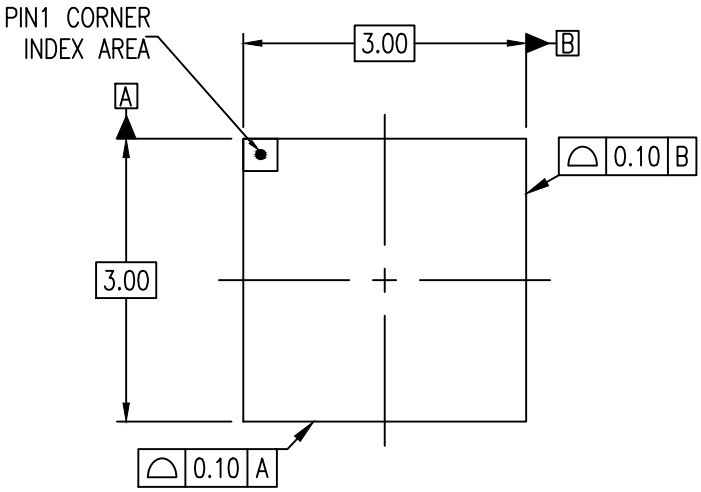
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.



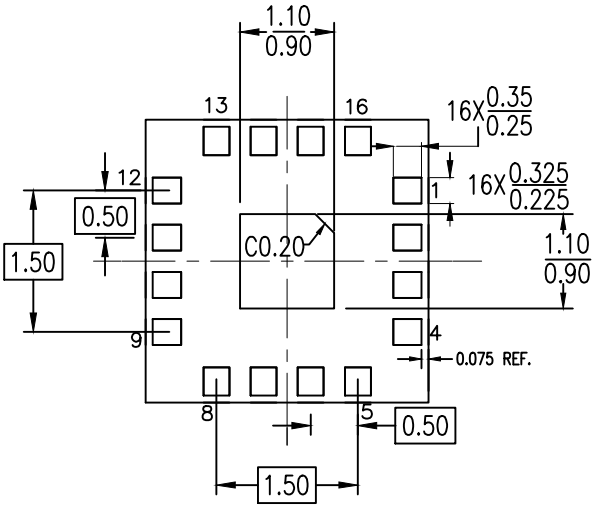
RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

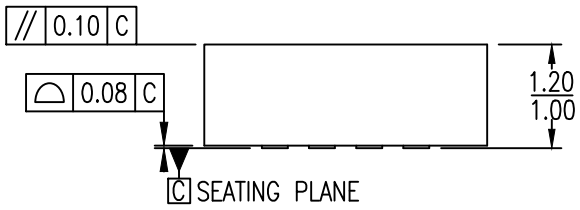
Package Revision History		
Date Created	Rev No.	Description
Sept 15, 2017	Rev 00	Initial Release



TOP VIEW

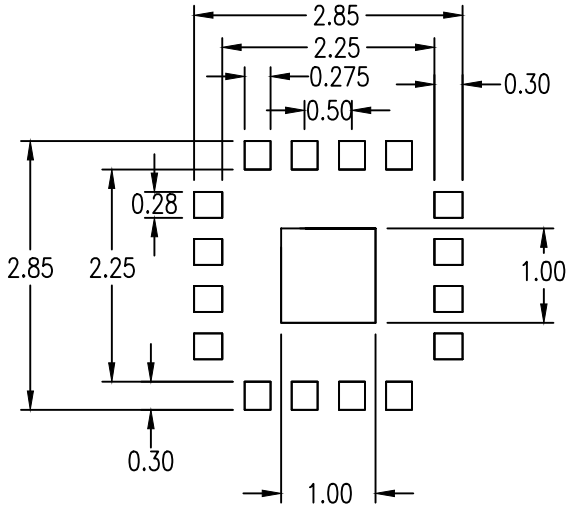


BOTTOM VIEW



SIDE VIEW

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Nov 6, 2017	Rev 02	Modify Solder Mask & Epad Chamfer
Sept 29, 2017	Rev 01	Modify Land Pattern

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