Description

The 9FGL6241 / 9FGL6251 are intelligent buffer/clock generators tailored for single and dual-ported nVME SSDs. They support Common (CC) and Independent Reference (IR) clocking architectures and are ideal for U.2 and M.2 form factors. The devices are also useful in PCIe master/slave and clock multiplexing applications, with an internal clock generator as a third input channel.

Typical Applications

- 1 × 4 and 2 × 2 nVME SSDs
- 3:2 PCIe clock multiplexing

Output Features

- Two 100MHz Low-Power HCSL (LP-HCSL) outputs with Zo = 100Ω or 85Ω
- One 33 1/3MHz or 25MHz 1.8V LVCMOS REF output
- One open drain CC_IR output indicates PCIe clock mode

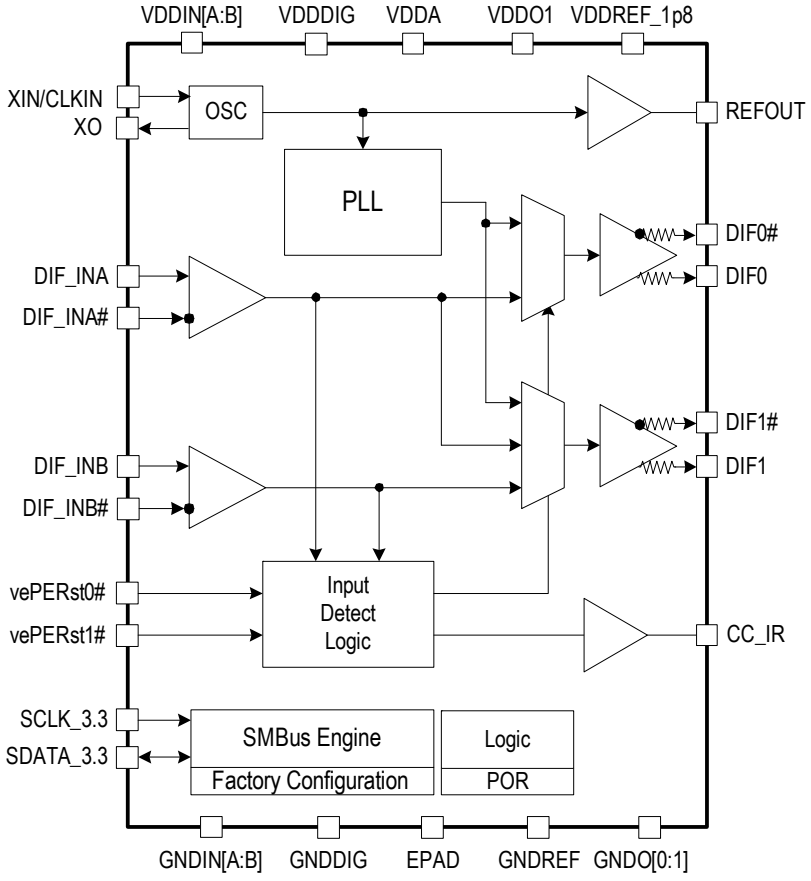
Features

- Automatically detects presence or absence of input clocks
- Integrated terminations on LP-HCSL outputs save 8 resistors
- 201, 301 configurations for SRnS (IR) or CC architectures default to 0% SSC
- 202, 302 configurations for SRIS (IR) or CC architectures default to -0.5% SSC
  - SMBus-selectable -0.25% SSC
- Choice of 25MHz or 33 1/3MHz reference clock
- REF clock output; saves external XO
- 2.5V to 3.3V operating voltage (VDDREF is 1.8V)
- 4 × 4 mm 28-VQFP-N package with external crystal
- 4 × 4 mm 28-LGA package with optional internal crystal
- Contact factory for other configurations

Key Specifications

- DIF cycle-to-cycle jitter < 50ps
- PCIe Gen1–4 (CC) compliant; Gen2–3 (IR) compliant

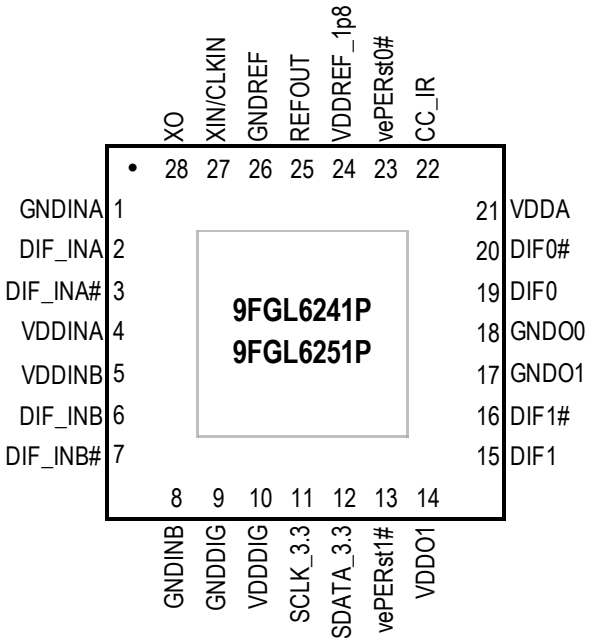
Block Diagram



Contents

Pin Assignments

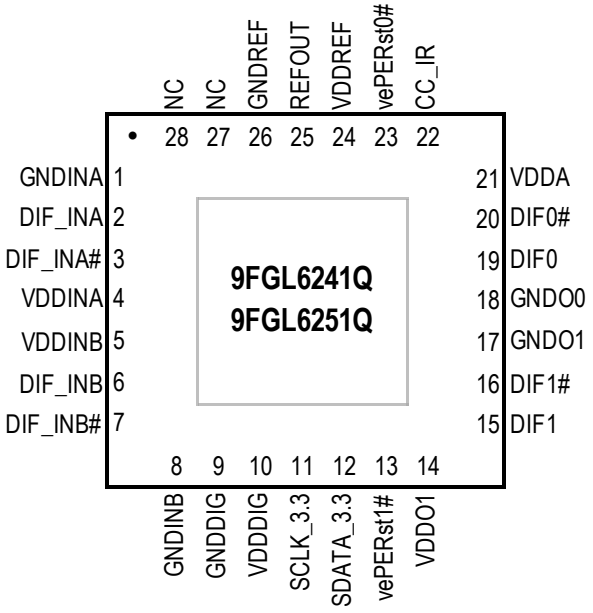
Figure 1. Pin Assignments for 4 × 4 mm NDG28 28-VQFP-N Package – Top View



28-VQFP-N, 4 × 4 mm, 0.4mm pitch

^ prefix indicates internal 120kohm pull-up resistor
v prefix indicates internal 120kohm pull-down resistor

Figure 2. Pin Assignments for 4 × 4 mm LTG28 28-LGA Package – Top View



28-LGA, 4 × 4 mm, 0.4mm pitch

^ prefix indicates internal 120kohm pull-up resistor
v prefix indicates internal 120kohm pull-down resistor

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	GNDINA	GND	Ground pin for input A.
2	DIF_INA	Input	True input of differential clock.
3	DIF_INA#	Input	Complement input of differential clock.
4	VDDINA	Power	Power supply for input A.
5	VDDINB	Power	Power supply for input B.
6	DIF_INB	Input	True input of differential clock.
7	DIF_INB#	Input	Complement input of differential clock.
8	GNDINB	GND	Ground pin for input B.
9	GNDDIG	GND	Ground pin for digital circuitry.
10	VDDDIG	Power	Digital power.
11	SCLK_3.3	Input	Clock pin of SMBus circuitry, 3.3V tolerant.
12	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
13	vePERst1#	Input	Enterprise PCIe Reset for Port B eSSD drives configured as 2 x 2. This active low signal indicates when the power supply is within specified voltage limits and is used to reset internal circuitry. The rising edge is used to determine the clocking mode. It is logically equivalent to PERST# reset signal. See the PCIe CEM specification for additional details.
14	VDDO1	Power	Power supply for output 1.
15	DIF1	Output	Differential true clock output.
16	DIF1#	Output	Differential complementary clock output.
17	GNDO1	GND	Ground pin for output 1.
18	GNDO0	GND	Ground pin for output 0.
19	DIF0	Output	Differential true clock output.
20	DIF0#	Output	Differential complementary clock output.
21	VDDA	Power	Power supply for PLL core. See Power Connections table for additional information.
22	CC_IR	Open Drain Output	Output indicating which mode (CC or IR) is active. Input clocks are present and are being directed to the outputs in CC mode. Input clocks are absent and internally generated clocks are being directed to the outputs in IR mode. This pin is an open drain output and requires an external pull up resistor for proper functionality. The polarity of this pin is programmable. Consult the General SMBus Serial Interface Information registers for details.
23	vePERst0#	Input	Enterprise PCIe Reset for Port A eSSD drives configured as 1x4 or 2x2. This active low signal indicates when the power supply is within specified voltage limits and is used to reset internal circuitry. The rising edge is used to determine the clocking mode. It is logically equivalent to PERST# reset signal. See the PCIe CEM specification for additional details.
24	VDDREF_1p8	Power	Power supply for XTAL and REF clocks, nominally 1.8V.
25	REFOUT	Output	Reference clock output.
26	GNDREF	GND	Ground pin for the REF outputs.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
27[a]	XIN/CLKIN	Input	Crystal input or reference clock input.
28[a]	XO	Output	Crystal output.
29	EPAD	GND	Connect to ground.

[a] These pins are no connect (NC) on devices with integrated crystal (9FGL6241Q and 9FGL6251Q).

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9FGL6241 / 9FGL6251 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Maximum	Units	Notes
Supply Voltage	V_{DDx}			4.6	V	1,2
Input Voltage	V_{IN}		-0.5	V_{DD}+0.5	V	1,3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins.		3.9	V	1
Storage Temperature	Ts		-65	150	°C	1
Junction Temperature	Tj			125	°C	1
Input ESD Protection	ESD prot	Human Body Model.	2500		V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 4.6V.

Thermal Characteristics

Table 3. Thermal Characteristics

Symbol	Parameter	Package	Typical Values	Units	Notes
θ_{JC}	Junction to case.	LTG28	51.4	°C/W	1
θ_{Jb}	Junction to base.		26.9	°C/W	1
θ_{JA0}	Junction to air, still air.		68.6	°C/W	1
θ_{JA1}	Junction to air, 1 m/s air flow.		63.5	°C/W	1
θ_{JA3}	Junction to air, 3 m/s air flow.		58.6	°C/W	1
θ_{JA5}	Junction to air, 5 m/s air flow.		56.2	°C/W	1

Table 3. Thermal Characteristics (Cont.)

Symbol	Parameter	Package	Typical Values	Units	Notes
θ_{JC}	Junction to case.	NDG28	42	°C/W	1
θ_{Jb}	Junction to base.		2.4	°C/W	1
θ_{JA0}	Junction to air, still air.		39	°C/W	1
θ_{JA1}	Junction to air, 1 m/s air flow.		33	°C/W	1
θ_{JA3}	Junction to air, 3 m/s air flow.		28	°C/W	1
θ_{JA5}	Junction to air, 5 m/s air flow.		27	°C/W	1

[1] EPAD soldered to board.

Electrical Characteristics

$T_A = T_{AMB}$. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 4. SMBus Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
SMBus Input Low Voltage	V_{ILSMB}				0.63	V	
SMBus Input High Voltage	V_{IHSMB}		1.17		3.6	V	
SMBus Output Low Voltage	V_{OLSMB}	At I_{PULLUP}.			0.4	V	
SMBus Sink Current	I_{PULLUP}	At V_{OL}.	4			mA	
Nominal Bus Voltage	V_{DDSMB}		1.8		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max. V_{IL} - 0.15V) to (Min. V_{IH} + 0.15V).			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min. V_{IH} + 0.15V) to (Max. V_{IL} - 0.15V).			300	ns	1
SMBus Operating Frequency	f_{SMB}	SMBus operating frequency.			400	kHz	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] The device must be powered up for the SMBus to function.

Table 5. Input/Supply/Common Parameters – Normal Operating Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	$V_{DDx2.5}$	2.5V supply voltage for all V_{DD} pins except V_{DDREF}	2.375	2.5	3.465	V	
	$V_{DDx3.3}$	3.3V supply voltage for all V_{DD} pins except V_{DDREF}	3.135	3.3	3.465	V	
	V_{DDREF}	Supply voltage for crystal oscillator and REFOUT.	1.71	1.8	1.89	V	
Ambient Operating Temperature	T_{AMB}	Industrial range.	-40	25	85	°C	
Input High Voltage	V_{IH}	ePERst0#, ePERst1#.	0.75 x V_{DDx}	1.6	V_{DDx} + 0.3	V	4
Input Low Voltage	V_{IL}		-0.3		0.25 x V_{DDx}	V	4

Table 5. Input/Supply/Common Parameters – Normal Operating Conditions (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input High Voltage	$V_{IHCLKIN}$	XIN/CLKIN.	0.65 x V_{DDREF}	1.6	V_{DDREF} + 0.3	V	5
Input Low Voltage	$V_{ILCLKIN}$		-0.3		0.35 x V_{DDREF}	V	5
Output High Voltage	V_{OHCC_IR}	CC_IR at default polarity.	0.9 x V_{DDx}		V_{DDx}	V	4
Output Low Voltage	V_{OLCC_IR}	CC_IR at default polarity.			0.4	V	4
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DD}.	-5		5	µA	
	I_{INP}	Single-ended inputs. V_{IN} = 0V; inputs with internal pull-up resistors. V_{IN} = V_{DD}; inputs with internal pull-down resistors.	-50		50	µA	
Input Frequency	F_{IN}	Differential inputs (DIF_IN).		100		MHz	
		Crystal input or clock input, 3xx devices.		33 1/3		MHz	
		Crystal input or clock input, 2xx devices.		25		MHz	
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic inputs, except DIF_IN.	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs.	1.5		2.7	pF	1
	C_{OUT}	Output pin capacitance.			6	pF	1
Clk Stabilization	t_{STAB}	From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock.		0.54	1.8	ms	1,2
Output SS Modulation Frequency	f_{MOD}	Modulation frequency (triangular modulation).	30	31.7	33	kHz	
Tfall	t_F	Fall time of single-ended control inputs.			5	ns	2
Trise	t_R	Rise time of single-ended control inputs.			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] V_{DDx} is either 2.5V or 3.3V.

[5] When driven by an external clock or XO, it must be AC coupled to the CLKIN pin.

Table 6. Differential Clock Input Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage – DIF_IN	V_{CROSS}	Cross over voltage.	150		900	mV	1
Input Swing – DIF_IN	V_{SWING}	Differential value.	300			mV	1
Input Slew Rate – DIF_IN	dv/dt	Measured differentially.	0.4		8	V/ns	1,2

Table 6. Differential Clock Input Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND.	-5		5	µA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform.	45		55	%	1
Input Jitter –Cycle to Cycle	J_{DIFIn}	Differential measurement.	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

Table 7. Current Consumption

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I_{DD_REF}	V_{DDREF} at 1.8V		1.7	2.6	mA	
	$I_{DD\_VDD2.5}$	2.5V operation in IR mode, V_{DDREF} at 1.8V.		37	47	mA	
	$I_{DD\_VDD3.3}$	3.3V operation in IR mode, V_{DDREF} at 1.8V.		40	50	mA	
	$I_{DD\_VDD2.5}$	2.5V operation in CC mode, V_{DDREF} at1.8V.		23	28	mA	
	$I_{DD\_VDD3.3}$	3.3V operation in CC mode, V_{DDREF} at 1.8V.		25	31	mA	

Table 8. Output Duty Cycle, Jitter, Skew and PLL Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Duty Cycle	t_{DC}	Measured differentially, IR Mode.	45	49	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, CC Mode.	-1.5	-0.3	0.7	%	1,3
Skew, Input to Output	t_{pdBYP}	Fanout Mode, V_T = 50%.	3300	3962	4600	ps	1
Skew, Output to Output	t_{sk3}	IR Mode, V_T = 50%.		17	50	ps	1,4
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	IR Mode.		20	50	ps	1,2
		Additive jitter in CC Mode.		0.3	10	ps	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operating in Common Clock Mode.

[4] All outputs at default slew rate.

Table 9. DIF Low-Power HCSL Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Slew Rate	dV/dt	Scope averaging on, fast setting.	1.3	2.2	3.2	V/ns	1,2,3
	dV/dt	Scope averaging on, slow setting.	0.7	1.5	2.5	V/ns	1,2,3
Slew Rate Matching	ΔdV/dt	Slew rate matching.		9	20	%	1,4
Voltage High	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on).	660	778	850	mV	7
Voltage Low	V_{LOW}		-150	-4	150		7

Table 9. DIF Low-Power HCSL Outputs (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Max Voltage	Vmax	Measurement on single-ended signal using absolute value (scope averaging off).		799	1150	mV	7
Min Voltage	Vmin		-300	-35			7
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.	250	412	550	mV	1,5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.		29	140	mV	1,6

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

Table 10. PCIe Filtered Additive Phase Jitter Parameters–Common Clocked (CC) Architectures, 3.3V Fanout Mode

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Additive Phase Jitter, CC (fanout buffer) Mode V_{DDREF} = 1.8V Other V_{DD}s = 3.3V	$t_{jphPCIeG1-CC}$	PCIe Gen1.		0.0	4.5	N/A	ps (p-p)	1,2,5
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.01	0.02		ps (rms)	1,2,4,5
		PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.2	0.31		ps (rms)	1,2,4,5
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.10	0.19		ps (rms)	1,2,4,5
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.10	0.19		ps (rms)	1,2,4,5

Table 11. PCIe Filtered Additive Phase Jitter Parameters–Common Clocked (CC) Architectures, 2.5V Fanout Mode

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Additive Phase Jitter, CC (fanout buffer) Mode V_{DDREF} = 1.8V Other V_{DD}s = 2.5V	$t_{jphPCIeG1-CC}$	PCIe Gen1.		0.7	3.9	N/A	ps (p-p)	1,2,5
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.01	0.02		ps (rms)	1,2,4,5
		PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.2	0.33		ps (rms)	1,2,4,5
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.12	0.20		ps (rms)	1,2,4,5
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.12	0.20		ps (rms)	1,2,4,5

[1] Applies to all outputs.

[2] Based on PCIe Base Specification Rev 4.0 version 1.0. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] For RMS values additive jitter is calculated by solving the following equation for b [*a^2 + b^2 = c^2*] where “a” is rms input jitter and “c” is rms total jitter.

[5] Driven by 9FGL0841 or equivalent.

Table 12. PCIe Filtered Phase Jitter Parameters–3.3V Clock Generator Mode [4,5]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
PCIe Gen1 (Common Clock)	$t_{jphPCIeG1-CC}$	SSC on or off, V_{DDx} = 3.3V, V_{DDREF} = 1.8V		16	28	86	ps (p-p)	1,2,5
PCIe Gen2 Lo Band (Common Clock) 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz)	$t_{jphPCIeG2-CC}$			0.43	0.55	3	ps (rms)	1,2,4,5
PCIe Gen2 High Band (Common Clock) 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz)				0.9	1.37	3.1	ps (rms)	1,2,4,5
PCIe Gen3 (Common Clock) (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)	$t_{jphPCIeG3-CC}$			0.25	0.38	1	ps (rms)	1,2,4,5
PCIe Gen4 (Common Clock) (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)	$t_{jphPCIeG4-CC}$			0.25	0.38	0.5	ps (rms)	1,2,4,5
PCIe Gen2 (SRIS) (PLL BW of 16MHz, CDR = 5MHz)	$t_{jphPCIeG2-IR}$	-0.5% spread, V_{DDx} = 3.3V, V_{DDREF} = 1.8V		0.7	0.81	2	ps (rms)	1,2
PCIe Gen3 (SRIS) (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)	$t_{jphPCIeG3-IR}$			0.6	0.67	0.7	ps (rms)	1,2
PCIe Gen2 (SRIS) (PLL BW of 16MHz, CDR = 5MHz)	$t_{jphPCIeG2-IR}$	-0.25% spread, V_{DDx} = 3.3V, V_{DDREF} = 1.8V		0.7	0.75	2	ps (rms)	1,2
PCIe Gen3 (SRIS) (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)	$t_{jphPCIeG3-IR}$			0.4	0.44	0.7	ps (rms)	1,2

Table 13. PCIe Filtered Phase Jitter Parameters–2.5V Clock Generator Mode [4,5]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
PCIe Gen1 (Common Clock)	$t_{jphPCIeG1-CC}$	SSC on or off, V_{DDx} = 2.5V, V_{DDREF} = 1.8V		17	29	86	ps (p-p)	1,2,5
PCIe Gen2 Lo Band (Common Clock) 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz)	$t_{jphPCIeG2-CC}$			0.44	0.56	3	ps (rms)	1,2,4,5
PCIe Gen2 High Band (Common Clock) 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz)				1.0	1.5	3.1	ps (rms)	1,2,4,5
PCIe Gen3 (Common Clock) (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)	$t_{jphPCIeG3-CC}$			0.29	0.41	1	ps (rms)	1,2,4,5
PCIe Gen4 (Common Clock) (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)	$t_{jphPCIeG4-CC}$			0.29	0.41	0.5	ps (rms)	1,2,4,5
PCIe Gen2 (SRIS) (PLL BW of 16MHz, CDR = 5MHz)	$t_{jphPCIeG2-IR}$	-0.5% spread, V_{DDx} = 2.5V, V_{DDREF} = 1.8V		0.9	1.1	2	ps (rms)	1,2
PCIe Gen3 (SRIS) (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)	$t_{jphPCIeG3-IR}$			0.62	0.70	0.7	ps (rms)	1,2
PCIe Gen2 (SRIS) (PLL BW of 16MHz, CDR = 5MHz)	$t_{jphPCIeG2-IR}$	-0.25% spread, V_{DDx} = 2.5V, V_{DDREF} = 1.8V		0.80	1.01	2	ps (rms)	1,2
PCIe Gen3 (SRIS) (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)	$t_{jphPCIeG3-IR}$			0.42	0.49	0.7	ps (rms)	1,2

[1] Applies to all outputs.

[2] Based on PCIe Base Specification Rev3.1a. These filters are different than common clock filters. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] As of PCIe Base Specification Rev4.0 version 1.0, IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRnS). Industry limits for IR clocking are not specified in the Base Specification; limits are commonly agreed upon with major customers.

[5] All outputs at default slew rate (fast).

Table 14. REF Output

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Long Accuracy	ppm	Independent Reference Mode.	-100	0	100	ppm	1,2
Long Accuracy	ppm	Common Clock Mode.		0		ppm	1,2
Clock Period	$T_{period25M}$	25MHz reference input.		40		ns	2
	$T_{period33M}$	33 1/3MHz reference input.		30		ns	2
Rise/Fall Slew Rate	t_{rf1}	Slowest slew rate, 20% to 80% of $V_{DDREF.}$	0.5	0.89	1.6	V/ns	1
	t_{rf2}	Slow slew rate, 20% to 80% of $V_{DDREF.}$	0.8	1.5	2.3	V/ns	1,3
	t_{rf3}	Fast slew rate, 20% to 80% of $V_{DDREF.}$	0.8	1.5	2.3	V/ns	1
	t_{rf4}	Fastest slew rate, 20% to 80% of $V_{DDREF.}$	1.0	1.7	2.4	V/ns	1
Duty Cycle	d_{t1X}	$V_T = V_{DD}/2$ V.	45	48.2	55	%	1,4
Duty Cycle Distortion	d_{tcd}	$V_T = V_{DD}/2$ V.	-0.75	0.00	0	%	1,5
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	$V_T = V_{DD}/2$ V.		52	250	ps	1,4

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Internal crystal, external crystal may be tuned to 0ppm.

[3] Default SMBus value.

[4] When driven by a crystal.

[5] When driven by an external oscillator via the XIN/CLKIN pin, XO should be floating.

Power Management

Table 15. Operating Configuration Table (Byte0, bit 5 = 0)

ePERst0#	DIF_INA	ePERst1#	DIF_INB	DIF0	DIF1	CC_IR[1,2]
↑	No clock present	0	X	From PLL	From PLL	IR Mode
↑	Clock present	0	X	Input A	Input B	CC Mode
0	X	↑	No clock present	From PLL	From PLL	IR Mode
0	X	↑	Clock present	Input A	Input B	CC Mode

[1] Polarity of CC_IR is determined by Byte3[3].

[2] CC_IR Mode is determined by the status of the input clock associated with the first ePERstn# to deassert.

[3] Rising arrow indicates first ePERst# to deassert. Once an ePERst# has gone high, the other ePERst# is ignored.

Table 16. Operating Configuration Table (Byte0, bit 5 = 1)

ePERst0#	DIF_INA	ePERst1#	DIF_INB	DIF0	DIF1	CC_IR[1,2]
↑	No clock present	X	X	From PLL	From PLL	IR Mode
↑	Clock present	X	X	Input A	Input A	CC Mode

[1] Polarity of CC_IR is determined by Byte3[3].

[2] When set to 1, the device only responds to DIF_INA and ePERst0#. ePERst1# must remain low and never deassert.

Table 17. SMBus Address

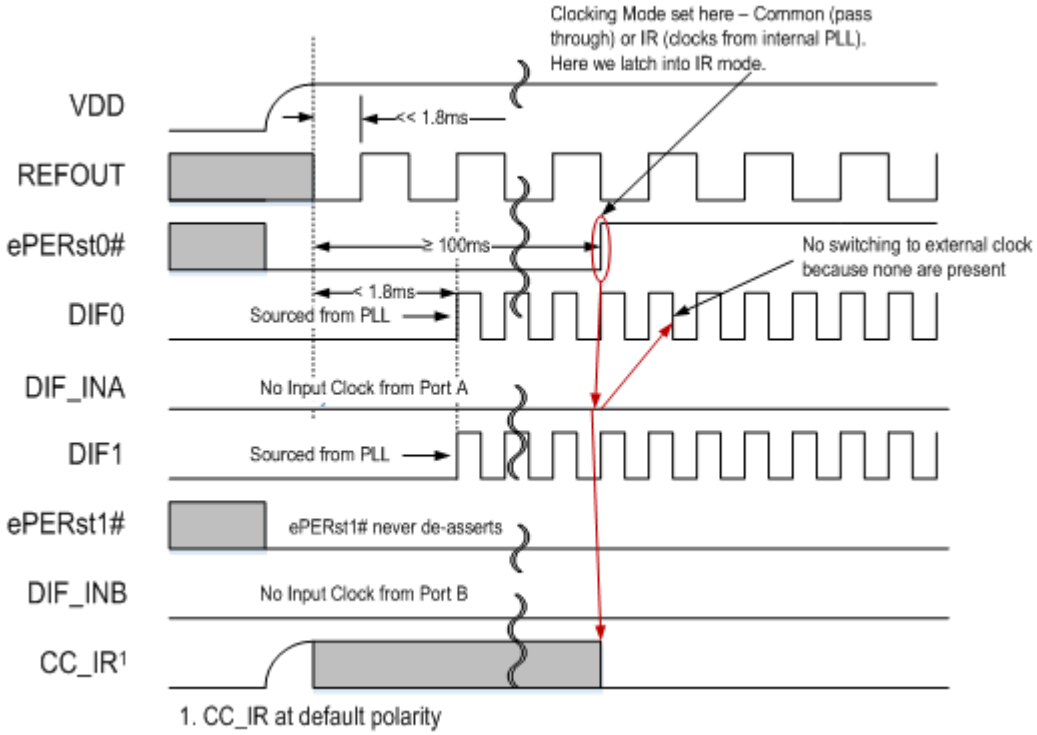
Address	+ Read/Write Bit
1101000	X

Table 18. Power Connections

Pin Number		
V_{DD}	GND	Description
4	1	DIF_INA
5	8	DIF_INB
10	9	Digital Power, SMBus
14	17	DIF1
21	18	DIF0, PLL analog
24	26	XTAL, REF

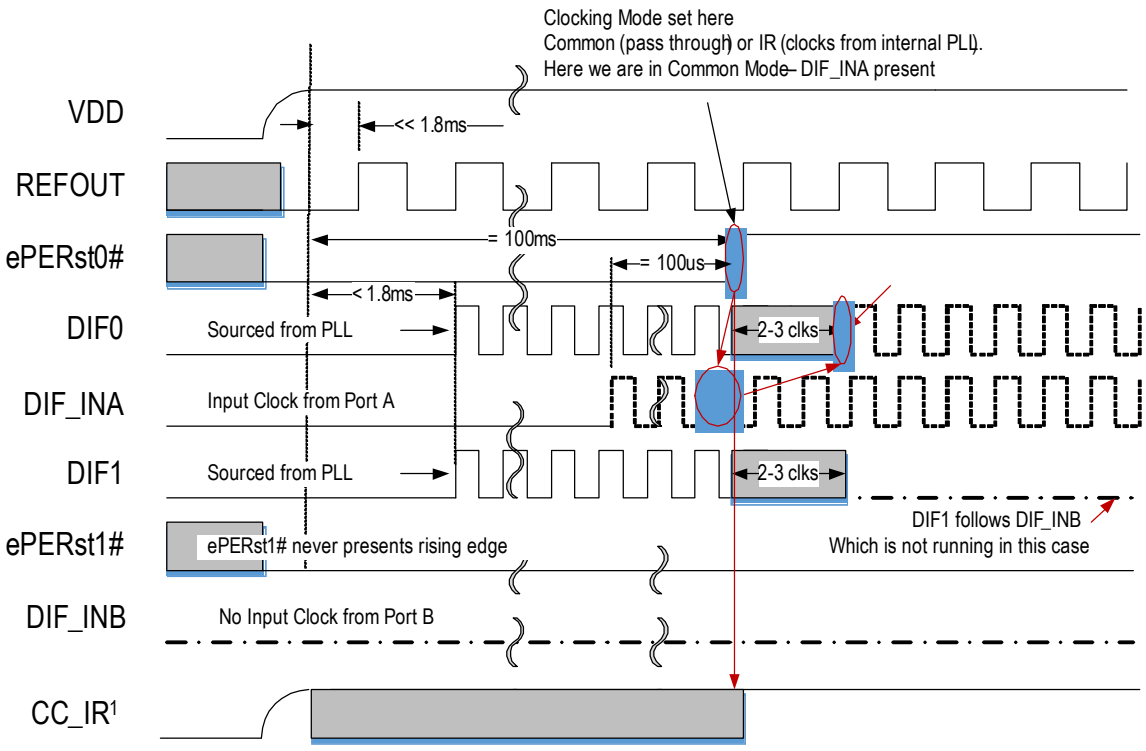
Timing Diagrams

Figure 3. Independent Reference Clock Mode from ePERst0# Deassertion



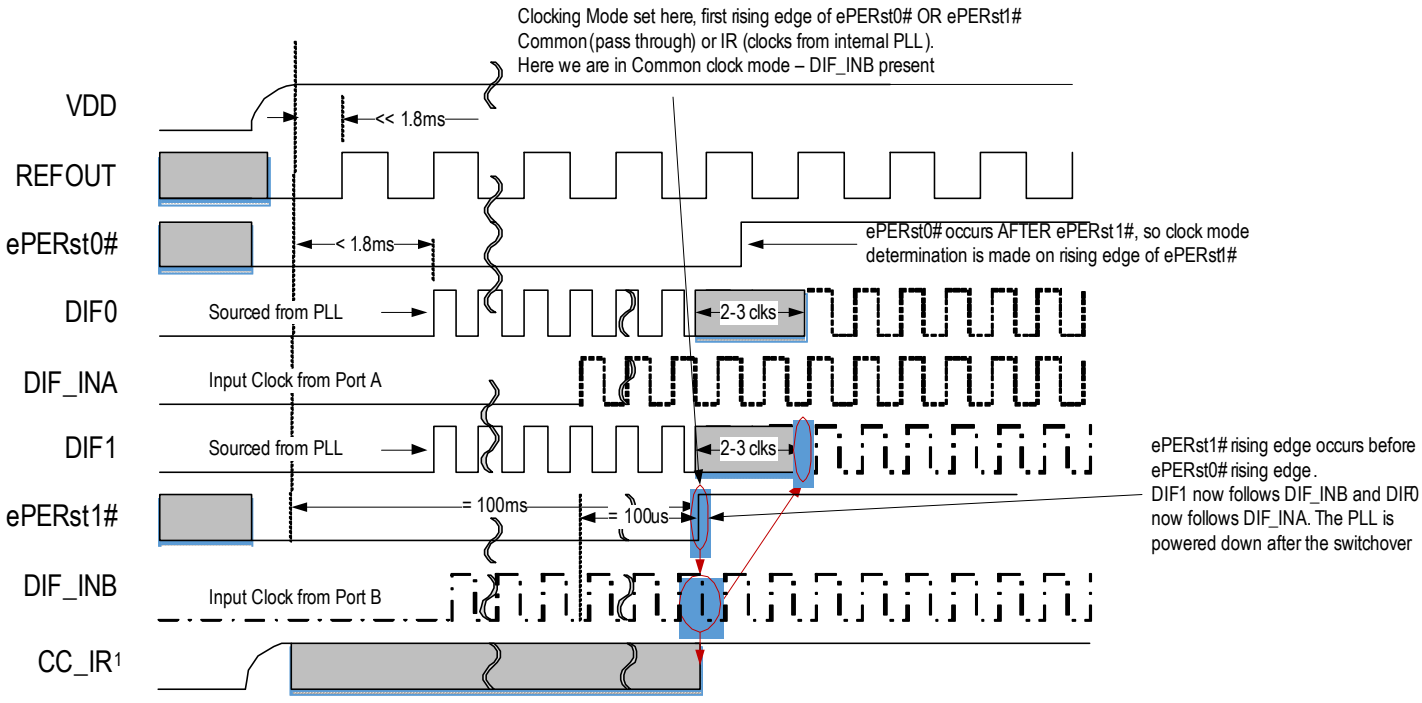
1. CC_IR at default polarity

Figure 4. Common Clock Mode from ePERst0# Deassertion



1. CC_IR at default polarity

Figure 5. Common Clock Mode from ePERst1# Deassertion



1. CC_IR at default polarity

Test Loads

Figure 6. LVCMOS AC/DC Test Load

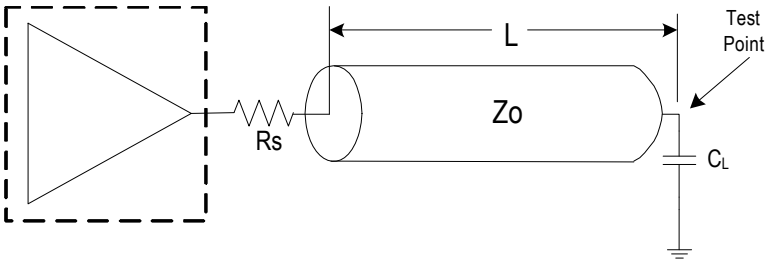


Figure 7. LP-HCSL AC/DC Test Load (standard PCIe source-terminated test load)

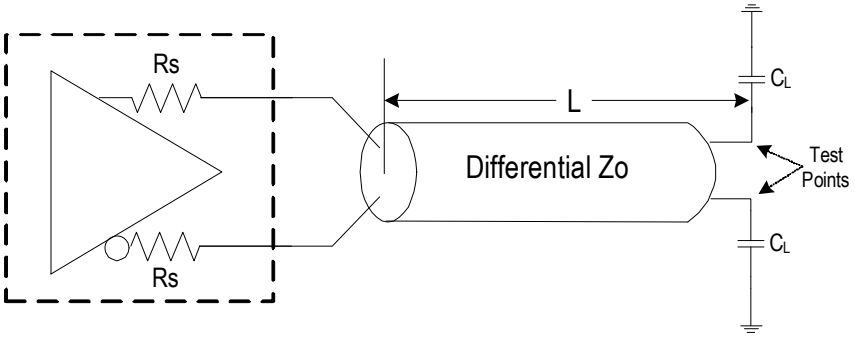


Figure 8. Test Setup for PCIe Jitter Measurements

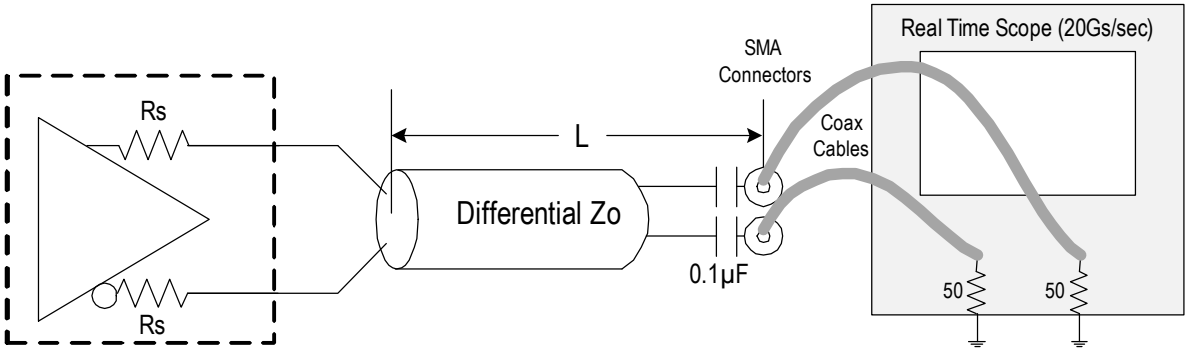


Table 19. Terminations

Device	L (inches)	Zo (Ω)	Rs (Ω)	LVCMOS C_L (pF)	LP-HCSL C_L (pF)
9FGL6241	10	100	None needed	4.7	2
9FGL6251	10	100	7.5		
9FGL6251	10	85	None needed		

Alternate Terminations

The 9FGL family can easily drive LVPECL, LVDS, and CML logic. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for details.

Crystal Characteristics

Table 20. Recommended Crystal Characteristics

Parameter	Value	Units
Frequency	25MHz or 33 1/3MHz	MHz
Resonance Mode	Fundamental	—
Frequency Tolerance @ 25°C	±20	ppm maximum
Frequency Stability, reference at 25°C over operating temperature range	±20	ppm maximum
Temperature Range (industrial)	-40–85	°C
Equivalent Series Resistance (ESR)	50	Ω maximum
Shunt Capacitance (C_O)	7	pF maximum
Load Capacitance (C_L)	6	pF maximum
Drive Level	0.3	mW maximum
Aging per year	±5	ppm maximum

Spread Spectrum Selection

Table 21. Spread Spectrum Selection for 201 and 301 Configurations

Byte 1[4:3]	Description	Spread Amount	Notes
00	SRnS Mode	0	Default configuration at power-up.
01	CC/SRIS Mode	-0.25%	Accessible via SMBus.
10	CC Mode	0	Accessible via SMBus.
11	CC/SRIS Mode	-0.50%	Accessible via SMBus.

The 201/301 devices are designed for Separate Reference clock No Spread applications. They power up in a special mode for this application (configuration 00). Using the SMBus to change to one of the other configurations will require a system reset. Transitioning back to configuration 00 from one of the other configurations will also require a system reset. Contact the factory if a different default configuration set is desired.

Table 22. Spread Spectrum Selection for 202 and 302 Configurations

Byte 1[4:3]	Description	Spread Amount	Notes
00	Reserved	Reserved	Reserved.
01	CC/SRIS Mode	-0.25%	Accessible via SMBus.
10	CC Mode	0	Accessible via SMBus.
11	CC/SRIS Mode	-0.50%	Default configuration at power-up.

The 202/302 devices are configured for Common Clock/Separate Reference clock Independent Spread applications. They power up in configuration 11. The SMBus may be used to change cleanly between configuration 01 or 10 without requiring a system reset. Contact the factory if a different default configuration set is desired.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Note: See Ordering Information for additional details on bits labeled “OTP Configured”.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Output Enable and Status Readback Register

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	DIF_INA Status	Presence of DIF_INA	R	DIF_INA not running	DIF_INA running	Real Time [b]
Bit 6	DIF_INB Status	Presence of DIF_INB	R	DIF_INB not running	DIF_INB running	Real Time [b]
Bit 5	1x4 CC Mode Configuration [c]	Allows DIF_INA to drive both DIF0 and DIF1 in CC mode	RW	DIFN_INA only drives DIF0 in CC Mode	DIF_INA drives both DIF[1:0] in CC Mode	0
Bit 4	ePERst1# PD_ EN	Enable pull-down on ePERst1#	RW	Pull-down disabled	Pull-down enabled	1
Bit 3	ePERst0# PD_EN	Enable pull-down on ePERst0#	RW	Pull-down disabled	Pull-down enabled	1
Bit 2	Reference Frequency	Specifies input frequency	RW	25MHz	33 1/3MHz	Part Number Dependent
Bit 1	DIF1 OE	Output Enable	RW	Disabled [a]	Enabled	1
Bit 0	DIF0 OE	Output Enable	RW	Disabled [a]	Enabled	1

[a] The disabled state depends on Byte2[3:2]. '00' = Low, '01' = HiZ, '10' = Low, '11' = High.

[b] The state of both of these inputs at the time of the first rising edge of ePERst0# or ePERst1# determines the operating mode of the device.

[c] Setting this bit to '1', allows the device to drive both DIF0 and DIF1 from DIF_INA in Common Clock mode. When set to '1', the device only responds to DIF_INA and ePERst0#. ePERst1# must remain low and never deassert.

SMBus Table: Spread Spectrum and V_{HIGH} Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	CC_IR Status [a]	CC-IR Readback	R	Common Clock Mode	Independent RefClk Mode	Latched
Bit 6	CC_IR_Mode Override [b]	Forces desired CC_IR Mode	RW	Common Clock Mode	Independent RefClk Mode	0
Bit 5	CC_IR_Override_Enable	Enable SW override of CC_IR Mode	RW	CC_IR controlled by ePERst logic	Byte1, bit 6 controls CC_IR Mode	0
Bit 4	Spread Spectrum Default[1] [c]	Spread Spectrum default	RW	See Spread Spectrum Selection Table 21 and Table 22 [c]		Part Number Dependent
Bit 3	Spread Spectrum Default[0] [c]		RW			
Bit 2	Reserved					X
Bit 1	DIF Amplitude[1]	Controls output amplitude	RW	00 = 0.6V	01 = 0.68V	1
Bit 0	DIF Amplitude[0]		RW	10 = 0.75V	11 = 0.85V	0

[a] This bit is indicates the state of the input clock (operating mode) associated with the first ePERst# signal to deassert and is latched upon its deassertion.

[b] Byte 1, bit 5 must be set to '1' for this bit to control operation of the part.

[c] The default value depends on the particular device.

SMBus Table: Slew Rate and Output Configuration Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	DIF[1]_IMP_1	Differential output 1 impedance[a]	RW	ZOUT: 00 = 33Ω	ZOUT: 10 = 100Ω	Part Number Dependent
Bit 6	DIF[1]_IMP_0		RW	ZOUT: 01 = 85Ω	11 = Reserved	
Bit 5	DIF[0]_IMP_1	Differential output 0 impedance[a]	RW	ZOUT: 00 = 33Ω	ZOUT: 10 = 100Ω	
Bit 4	DIF[0]_IMP_0		RW	ZOUT: 01 = 85Ω	11 = Reserved	
Bit 3	STOP_STOP[1]	Output stop state (True/Complement)	RW	00 = Low/Low	10 = High/Low	00
Bit 2	STOP_STATE[0]		RW	01 = HiZ/HiZ	11 = Low/High	
Bit 1	DIF1 SLEW RATE SEL	Adjust slew rate of DIF1	RW	Slow setting	Fast setting	1
Bit 0	DIF0 SLEW RATE SEL	Adjust slew rate of DIF0	RW	Slow setting	Fast setting	1

[a] 9FGL624x devices default to '10' (100Ω). 9FGL625x devices default to '01' (85Ω).

SMBus Table: REF and Polarity Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	REF Slew Rate	Slew rate control	RW	00 = Slowest	01 = Slow	0
Bit 6			RW	10 = Fast	11 = Fastest	1
Bit 5	Reserved					X
Bit 4	REF OE	REF output enable	RW	Disabled[a]	Enabled	1
Bit 3	CC_IR POLARITY	Determines CC_IR polarity	RW	Low when input detected (Common Mode)	Low when Input is NOT detected (IR Mode)	1
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	Reserved					X

[a] The disabled state depends on Byte2[3:2]. '00' = Low, '01' = HiZ, '10' = Low, '11' = High.

SMBus Table: Reserved Register

Byte 4	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Reserved					1
Bit 5	Reserved					1
Bit 4	Reserved					1
Bit 3	Reserved					1
Bit 2	Reserved					1
Bit 1	Reserved					1
Bit 0	Reserved					1

Note: Byte 4 is reserved and reads back 'hFF'.

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	1st silicon = 0000 A revision = 0001		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			1
Bit 3	VID3	VENDOR ID	R	0001 = IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Device Type/Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device ID7	Device ID	RW	Device with external crystal in NDG28 = 1C hex Device with internal crystal in LTG28 = 18 hex		0
Bit 6	Device ID6		RW			0
Bit 5	Device ID5		RW			0
Bit 4	Device ID4		RW			1
Bit 3	Device ID3		RW			1
Bit 2	Device ID2		RW			x
Bit 1	Device ID1		RW			0
Bit 0	Device ID0		RW			0

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	BC4	Byte count programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

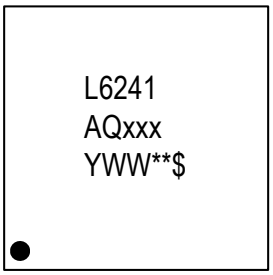
Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

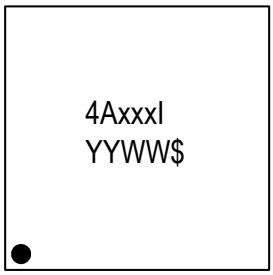
www.idt.com/document/psc/ndndg28-package-outline-40-x-40-x-09-mm-body-vqpf-n-04-mm-ball-pitch

www.idt.com/document/psc/ltg28-package-outline-40-x-40-mm-body-04-mm-pitch-lga

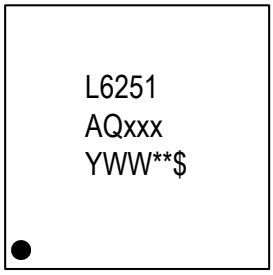
Marking Diagrams



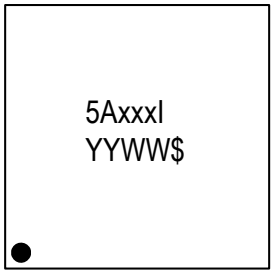
(for 9FGL6241Q
28-LGA devices)



(for 9FGL6241
28-VQFP-N devices)



(for 9FGL6251Q
28-LGA devices)



(for 9FGL6251
28-VQFP-N devices)

- Line 1 and 2 (Line 1 only on VQFP-N devices) is the truncated part number.
- “xxx” denotes dash code (201, 202, 301, 302)
- “YWW” or “YYWW” is the last digit(s) of the year and work-week that the part was assembled.
- “**” denotes sequential lot number.
- “$” denotes mark code.

Ordering Information

Table 23. Ordering Information

Orderable Part Number	Crystal/XO	IR Spread Mode	DIF ZOUT	Package	Carrier Type	Temperature
9FGL6241AQ201LTGI	25MHz internal	SSC off (SRNS)	100Ω	28-LGA	Trays	-40° to +85°C
9FGL6241AQ201LTGI8					Tape and Reel	
9FGL6241AQ202LTGI		SSC on (SRIS)			Trays	
9FGL6241AQ202LTGI8					Tape and Reel	
9FGL6241AP201NDGI	25MHz external	SSC off (SRNS)		28-VQFP-N	Trays	
9FGL6241AP201NDGI8					Tape and Reel	
9FGL6241AP202NDGI		SSC on (SRIS)			Trays	
9FGL6241AP202NDGI8					Tape and Reel	
9FGL6241AQ301LTGI	33 1/3MHz internal	SSC off (SRNS)		28-LGA	Trays	
9FGL6241AQ301LTGI8					Tape and Reel	
9FGL6241AQ302LTGI		SSC on (SRIS)			Trays	
9FGL6241AQ302LTGI8					Tape and Reel	
9FGL6241AP301NDGI	33 1/3MHz external	SSC off (SRNS)		28-VQFP-N	Trays	
9FGL6241AP301NDGI8					Tape and Reel	
9FGL6241AP302NDGI		SSC on (SRIS)			Trays	
9FGL6241AP302NDGI8					Tape and Reel	
9FGL6251AQ201LTGI	25MHz internal	SSC off (SRNS)	85Ω	28-LGA	Trays	
9FGL6251AQ201LTGI8					Tape and Reel	
9FGL6251AQ202LTGI		SSC on (SRIS)			Trays	
9FGL6251AQ202LTGI8					Tape and Reel	
9FGL6251AP201NDGI	25MHz external	SSC off (SRNS)		28-VQFP-N	Trays	
9FGL6251AP201NDGI8					Tape and Reel	
9FGL6251AP202NDGI		SSC on (SRIS)			Trays	
9FGL6251AP202NDGI8					Tape and Reel	
9FGL6251AQ301LTGI	33 1/3MHz internal	SSC off (SRNS)		28-LGA	Trays	
9FGL6251AQ301LTGI8					Tape and Reel	
9FGL6251AQ302LTGI		SSC on (SRIS)			Trays	
9FGL6251AQ302LTGI8					Tape and Reel	
9FGL6251AP301NDGI	33 1/3MHz external	SSC off (SRNS)		28-VQFP-N	Trays	
9FGL6251AP301NDGI8					Tape and Reel	
9FGL6251AP302NDGI		SSC on (SRIS)			Trays	
9FGL6251AP302NDGI8					Tape and Reel	

“G” indicates RoHS 6 of 6 compliant.

Revision History

Revision Date	Description of Change
November 9, 2018	▪ Updated document title. ▪ Updated Features bullets. ▪ Updated Input/Supply/Common Parameters table. ▪ Updated Spread Spectrum tables. ▪ Updated SMBus Table: Spread Spectrum and VHIGH Control Register (Byte1).
October 11, 2018	Initial release.