

## ULTRA MOBILE PC CLOCK FOR EMBEDDED APPLICATIONS

ICS9EMS9633

### Recommended Application:

Poulsbo Based Ultra-Mobile PC (UMPC) for Embedded Applications

### Output Features:

- 3 - CPU low power differential push-pull pairs
- 3 - SRC low power differential push-pull pairs
- 1 - LCD100 SSCD low power differential push-pull pair
- 1 - DOT96 low power differential push-pull pair
- 1 - REF, 14.31818MHz, 3.3V SE output

### Features/Benefits:

- Industrial temperature range compliant
- Supports ULV CPUs with 67 to 167 MHz CPU outputs
- Dedicated TEST/SEL and TEST/MODE pins saves isolation resistors on pins
- CPU STOP# input for power management
- Fully integrated Vreg
- Integrated series resistors on differential outputs
- 1.5V VDD IO operation, 3.3V VDD core and REF supply pin for REF
- -40 to +85C operating range

### SSOP Pin Configuration

REF	1	48	VDDREF_3.3
GNDREF	2	47	X1
VDDCORE_3.3	3	46	X2
FSC_L	4	45	CLKPWRGD#/PD_3.3
TEST_MODE	5	44	CPU_STOP#
TEST_SEL	6	43	CPUT0_LPR
SCLK	7	42	CPUC0_LPR
SDATA	8	41	VDDIO_1.5
VDDCORE_3.3	9	40	GNDCPU
VDDIO_1.5	10	39	CPUT1_LPR
DOT96C_LPR	11	38	CPUC1_LPR
DOT96T_LPR	12	37	VDDCORE_3.3
GNDDOT	13	36	VDDIO_1.5
GNDLCD	14	35	GNDCPU
LCD100C_LPR	15	34	CPUT2_LPR
LCD100T_LPR	16	33	CPUC2_LPR
VDDIO_1.5	17	32	FSB_L
VDDCORE_3.3	18	31	*CR#2
*CR#0	19	30	SRCT2_LPR
GNDSRC	20	29	SRCC2_LPR
SRCC0_LPR	21	28	GNDSRC
SRCT0_LPR	22	27	SRCT1_LPR
*CR#1	23	26	SRCC1_LPR
VDDCORE_3.3	24	25	VDDIO_1.5

9EMS9633

48 SSOP Package

\* indicates inputs with internal pull up of ~10Kohm to 3.3V

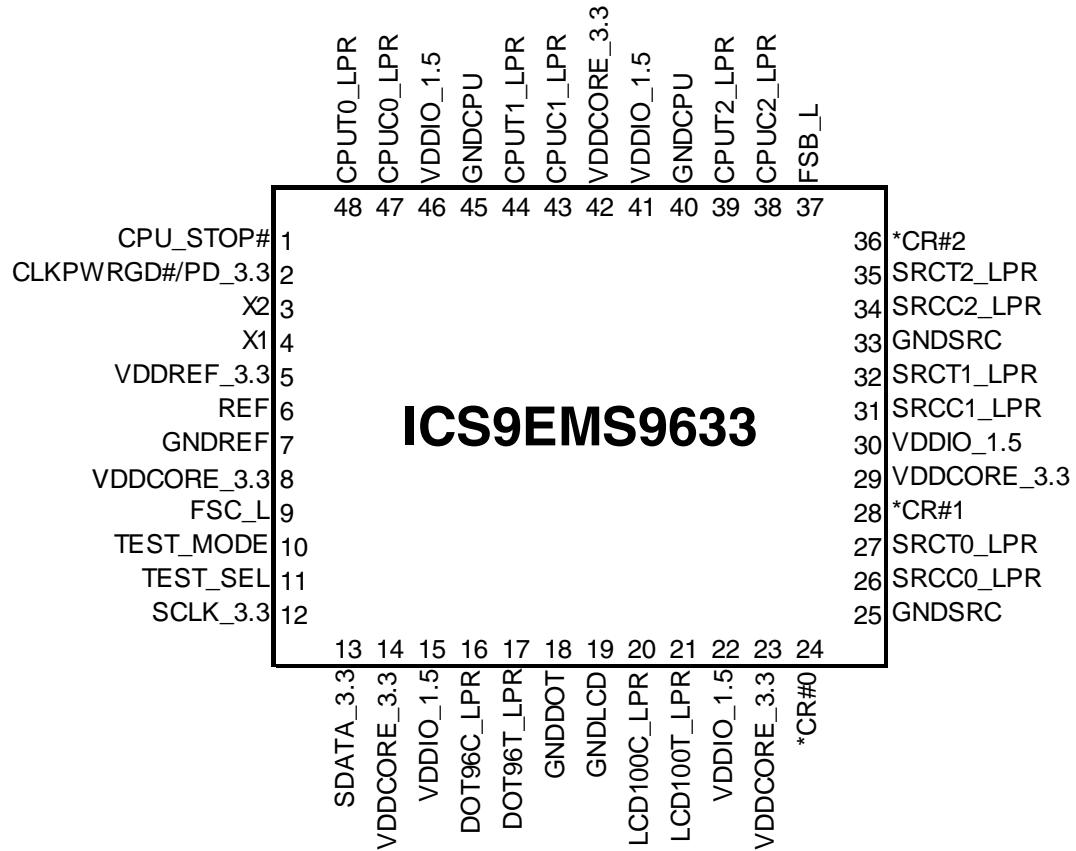
## SSOP Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	REF	OUT	14.318 MHz reference clock.
2	GNDREF	PWR	Ground pin for the REF outputs.
3	VDDCORE_3.3	PWR	3.3V power for the PLL core
4	FSC_L	IN	Low threshold input for CPU frequency selection. Refer to input electrical characteristics for $V_{il\_FS}$ and $V_{ih\_FS}$ values.
5	TEST_MODE	IN	TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
6	TEST_SEL	IN	TEST_SEL: latched input to select TEST MODE 1 = All outputs are tri-stated for test 0 = All outputs behave normally.
7	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
8	SDATA	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
9	VDDCORE_3.3	PWR	3.3V power for the PLL core
10	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
11	DOT96C_LPR	OUT	Complement clock of low power differential pair for 96.00MHz DOT clock. No 50ohm resistor to GND needed. No Rs needed.
12	DOT96T_LPR	OUT	True clock of low power differential pair for 96.00MHz DOT clock. No 50ohm resistor to GND needed. No Rs needed.
13	GNDOT	PWR	Ground pin for DOT clock output
14	GNDLCD	PWR	Ground pin for LCD clock output
15	LCD100C_LPR	OUT	Complement clock of low power differential pair for LCD100 SS clock. No 50ohm resistor to GND needed. No Rs needed.
16	LCD100T_LPR	OUT	True clock of low power differential pair for LCD100 SS clock. No 50ohm resistor to GND needed. No Rs needed.
17	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
18	VDDCORE_3.3	PWR	3.3V power for the PLL core
19	*CR#0	IN	Clock request for SRC0, 0 = enable, 1 = disable
20	GNDSRC	PWR	Ground pin for the SRC outputs
21	SRCC0_LPR	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
22	SRCT0_LPR	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
23	*CR#1	IN	Clock request for SRC1, 0 = enable, 1 = disable
24	VDDCORE_3.3	PWR	3.3V power for the PLL core

**SSOP Pin Description (continued)**

PIN #	PIN NAME	TYPE	DESCRIPTION
25	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
26	SRCC1_LPR	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
27	SRCT1_LPR	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
28	GNDSRC	PWR	Ground pin for the SRC outputs
29	SRCC2_LPR	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
30	SRCT2_LPR	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
31	*CR#2	IN	Clock request for SRC2, 0 = enable, 1 = disable
32	FSB_L	IN	Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
33	CPUC2_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
34	CPUT2_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
35	GNDCPU	PWR	Ground pin for the CPU outputs
36	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
37	VDDCORE_3.3	PWR	3.3V power for the PLL core
38	CPUC1_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
39	CPUT1_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
40	GNDCPU	PWR	Ground pin for the CPU outputs
41	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
42	CPUC0_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
43	CPUT0_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
44	CPU_STOP#	IN	Stops all CPU clocks, except those set to be free running clocks
45	CLKPWRGD#/PD_3.3	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active low input. / Asynchronous active high input pin used to place the device into a power down state.
46	X2	OUT	Crystal output, Nominally 14.318MHz
47	X1	IN	Crystal input, Nominally 14.318MHz.
48	VDDREF_3.3	PWR	Power pin for the XTAL and REF clocks, nominal 3.3V

## MLF Pin Configuration



**48-pin MLF, 6x6 mm, 0.4mm pitch**

\* indicates inputs with internal pull up of ~10Kohm to 3.3V

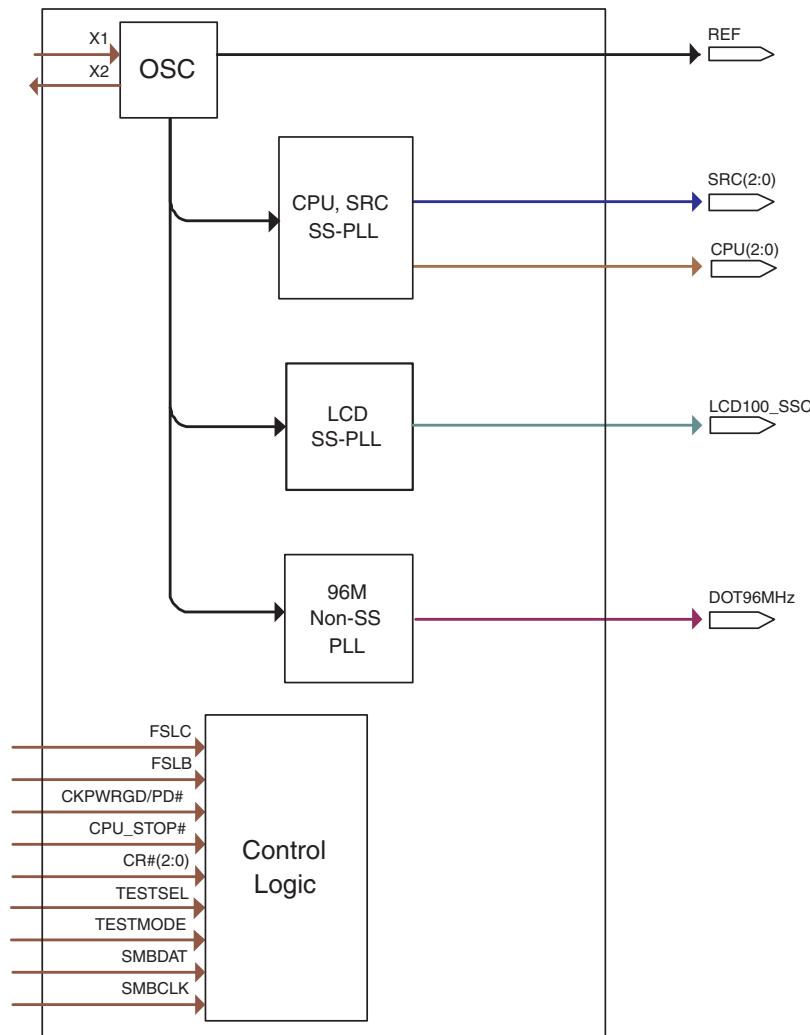
## MLF Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	CPU_STOP#	IN	Stops all CPU clocks, except those set to be free running clocks
2	CLKPWRGD#/PD_3.3	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active low input. / Asynchronous active high input pin used to place the device into a power down state.
3	X2	OUT	Crystal output, Nominally 14.318MHz
4	X1	IN	Crystal input, Nominally 14.318MHz.
5	VDDREF_3.3	PWR	Power pin for the XTAL and REF clocks, nominal 3.3V
6	REF	OUT	14.318 MHz reference clock.
7	GNDREF	PWR	Ground pin for the REF outputs.
8	VDDCORE_3.3	PWR	3.3V power for the PLL core
9	FSC_L	IN	Low threshold input for CPU frequency selection. Refer to input electrical characteristics for $V_{il\_FS}$ and $V_{ih\_FS}$ values.
10	TEST_MODE	IN	TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
11	TEST_SEL	IN	TEST_SEL: latched input to select TEST MODE 1 = All outputs are tri-stated for test 0 = All outputs behave normally.
12	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
13	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
14	VDDCORE_3.3	PWR	3.3V power for the PLL core
15	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
16	DOT96C_LPR	OUT	Complement clock of low power differential pair for 96.00MHz DOT clock. No 50ohm resistor to GND needed. No Rs needed.
17	DOT96T_LPR	OUT	True clock of low power differential pair for 96.00MHz DOT clock. No 50ohm resistor to GND needed. No Rs needed.
18	GNDOT	PWR	Ground pin for DOT clock output
19	GNDLCD	PWR	Ground pin for LCD clock output
20	LCD100C_LPR	OUT	Complement clock of low power differential pair for LCD100 SS clock. No 50ohm resistor to GND needed. No Rs needed.
21	LCD100T_LPR	OUT	True clock of low power differential pair for LCD100 SS clock. No 50ohm resistor to GND needed. No Rs needed.
22	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
23	VDDCORE_3.3	PWR	3.3V power for the PLL core
24	*CR#0	IN	Clock request for SRC0, 0 = enable, 1 = disable

**MLF Pin Description (continued)**

PIN #	PIN NAME	TYPE	DESCRIPTION
25	GNDSRC	PWR	Ground pin for the SRC outputs
26	SRCC0_LPR	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
27	SRCT0_LPR	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
28	*CR#1	IN	Clock request for SRC1, 0 = enable, 1 = disable
29	VDDCORE_3.3	PWR	3.3V power for the PLL core
30	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
31	SRCC1_LPR	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
32	SRCT1_LPR	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
33	GNDSRC	PWR	Ground pin for the SRC outputs
34	SRCC2_LPR	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
35	SRCT2_LPR	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
36	*CR#2	IN	Clock request for SRC2, 0 = enable, 1 = disable
37	FSB_L	IN	Low threshold input for CPU frequency selection. Refer to input electrical characteristics for $V_{il\_FS}$ and $V_{ih\_FS}$ values.
38	CPUC2_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
39	CPUT2_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
40	GNDCPU	PWR	Ground pin for the CPU outputs
41	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
42	VDDCORE_3.3	PWR	3.3V power for the PLL core
43	CPUC1_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
44	CPUT1_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
45	GNDCPU	PWR	Ground pin for the CPU outputs
46	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
47	CPUC0_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
48	CPUT0_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.

## Functional Block Diagram



## Power Groups

Pin Number		Description	
VDD	GND		
41, 46	40, 45	CPUCLK	Low power outputs
42			VDDCORE_3.3V
30	25, 33	SRCCLK	Low power outputs
29			VDDCORE_3.3V
22	19	LCDCLK	Low power outputs
23			VDDCORE_3.3V
15	18	DOT 96Mhz	Low power outputs
14			VDDCORE_3.3V
5	7	Xtal, REF	

## Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
3.3V Supply Voltage	V <sub>DDxxx_3.3</sub>	Supply Voltage		3.9	V	1,2
1.5V Supply Voltage	V <sub>DDxxx_1.5</sub>	Supply Voltage		3.9	V	1,2
3.3_Input High Voltage	V <sub>IH3.3</sub>	3.3V Inputs		VDD_3.3+ 0.3V	V	1,2,3
Minimum Input Voltage	V <sub>IL</sub>	Any Input	GND - 0.5		V	1
Storage Temperature	T <sub>s</sub>	-	-65	150	°C	1,2
Input ESD protection	ESD prot	Human Body Model	2000		V	1,2
		Man Machine Model	200		V	1,2

### Notes:

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Operation under these conditions is neither implied, nor guaranteed.

<sup>3</sup> Maximum input voltage is not to exceed maximum VDD

## Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Ambient Operating Temp	T <sub>ambientTEMP</sub>	No Airflow	-40	85	°C	1
3.3V Supply Voltage	V <sub>DDxxx_3.3</sub>	3.3V +/- 5%	3.135	3.465	V	1
1.5V Supply Voltage	V <sub>DDxxx_1.5</sub>	1.5V - 5% to 3.3V + 5%	1.425	3.465	V	1
3.3V Input High Voltage	V <sub>IHSE3.3</sub>	Single-ended inputs	2	V <sub>DD</sub> + 0.3	V	1
3.3V Input Low Voltage	V <sub>ILSE3.3</sub>	Single-ended inputs	V <sub>SS</sub> - 0.3	0.8	V	1
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND	-5	5	uA	1
Input Leakage Current	I <sub>INRES</sub>	Inputs with pull or pull down resistors. (CR# pins) V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND	-200	200	uA	1
Output High Voltage	V <sub>OHSE</sub>	Single-ended outputs, I <sub>OH</sub> = -1mA	2.4		V	1
Output Low Voltage	V <sub>OLSE</sub>	Single-ended outputs, I <sub>OL</sub> = 1 mA		0.4	V	1
Low Threshold Input-High Voltage	V <sub>IH_FS</sub>	3.3 V +/- 5%	0.7	1.5	V	1
Low Threshold Input-Low Voltage	V <sub>IL_FS</sub>	3.3 V +/- 5%	V <sub>SS</sub> - 0.3	0.35	V	1
Operating Supply Current	I <sub>DD_DEFAULT</sub>	3.3V supply, LCDPLL off		65	mA	1
	I <sub>DD_LCDEN</sub>	3.3V supply, LCDPLL enabled		70	mA	1
	I <sub>DD_IO</sub>	1.5V supply, Differential IO current, all outputs enabled		55	mA	1
Power Down Current	I <sub>DD_PD3.3</sub>	3.3V supply, Power Down Mode		2	mA	1
	I <sub>DD_PDI0</sub>	1.5V IO supply, Power Down Mode		0.5	mA	1
Input Frequency	F <sub>i</sub>	V <sub>DD</sub> = 3.3 V		15	MHz	2
Pin Inductance	L <sub>pin</sub>			7	nH	1
Input Capacitance	C <sub>IN</sub>	Logic Inputs	1.5	5	pF	1
	C <sub>OUT</sub>	Output pin capacitance		6	pF	1
	C <sub>INX</sub>	X1 & X2 pins		5	pF	1
Spread Spectrum Modulation Frequency	f <sub>SSMOD</sub>	Triangular Modulation	30	33	kHz	1

### AC Electrical Characteristics - Input/Common Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Clk Stabilization	$T_{STAB}$	From VDD Power-Up or de-assertion of PD# to 1st clock		1.8	ms	1
Tdrive_SRC	$T_{DRSRC}$	SRC output enable after CR# assertion		15	ns	1
Tdrive_PD#	$T_{DRPD}$	Differential output enable after PD# de-assertion		300	us	1
Tdrive_CPU	$T_{DRSRC}$	CPU output enable after CPU_STOP# de-assertion		10	ns	1
Tfall_PD#	$T_{FALL}$	Fall/rise time of PD# and CPU_STOP# inputs		5	ns	1
Trise_PD#	$T_{RISE}$			5	ns	1

### AC Electrical Characteristics - Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	$t_{SLR}$	Differential Measurement	0.5	6	V/ns	1,2
Falling Edge Slew Rate	$t_{FLR}$	Differential Measurement	0.5	6	V/ns	1,2
Rise/Fall Time Variation	$t_{SLVAR}$	Single-ended Measurement		125	ps	1
Maximum Output Voltage	$V_{HIGH}$	Includes overshoot		1150	mV	1
Minimum Output Voltage	$V_{LOW}$	Includes undershoot	-300		mV	1
Differential Voltage Swing	$V_{SWING}$	Differential Measurement	300		mV	1
Crossing Point Voltage	$V_{XABS}$	Single-ended Measurement	300	550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		140	mV	1,3,5
Duty Cycle	$D_{CYC}$	Differential Measurement	45	55	%	1
CPU Jitter - Cycle to Cycle	$CPUJ_{c2c}$	Differential Measurement		85	ps	1
SRC Jitter - Cycle to Cycle	$SRCJ_{c2c}$	Differential Measurement		125	ps	1
DOT Jitter - Cycle to Cycle	$DOTJ_{c2c}$	Differential Measurement		250	ps	1
CPU[2:0] Skew	$CPU_{SKEW10}$	Differential Measurement		100	ps	1
SRC[2:0] Skew	$SRC_{SKEW}$	Differential Measurement		250	ps	1

### Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300	300	ppm	1,2
Clock period	$T_{period}$	14.318MHz output nominal	69.8203	69.8622	ns	2
Absolute min/max period	$T_{abs}$	14.318MHz output nominal	69.8203	70.86224	ns	2
Output High Voltage	$V_{OH}$	$I_{OH} = -1 \text{ mA}$	2.4		V	1
Output Low Voltage	$V_{OL}$	$I_{OL} = 1 \text{ mA}$		0.4	V	1
Output High Current	$I_{OH}$	$V_{OH} @ \text{MIN} = 1.0 \text{ V}$ , $V_{OH} @ \text{MAX} = 3.135 \text{ V}$	-33	-33	mA	1
Output Low Current	$I_{OL}$	$V_{OL} @ \text{MIN} = 1.95 \text{ V}$ , $V_{OL} @ \text{MAX} = 0.4 \text{ V}$	30	38	mA	1
Rising Edge Slew Rate	$t_{SLR}$	Measured from 0.8 to 2.0 V	1	4	V/ns	1
Falling Edge Slew Rate	$t_{FLR}$	Measured from 2.0 to 0.8 V	1	4	V/ns	1
Duty Cycle	$d_{11}$	$V_T = 1.5 \text{ V}$	45	55	%	1
Jitter	$t_{cyc-cyc}$	$V_T = 1.5 \text{ V}$		1000	ps	1

## Electrical Characteristics - SMBus Interface

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
SMBus Voltage	$V_{DD}$		2.7	3.3	V	1
Low-level Output Voltage	$V_{OLSM}$	@ $I_{PULLUP}$		0.4	V	1
Current sinking at $V_{OLSM} = 0.4$ V	$I_{PULLUP}$	SMB Data Pin	4		mA	1
SCLK/SDATA Clock/Data Rise Time	$T_{RI2C}$	(Max VIL - 0.15) to (Min VIH + 0.15)		1000	ns	1
SCLK/SDATA Clock/Data Fall Time	$T_{FI2C}$	(Min VIH + 0.15) to (Max VIL - 0.15)		300	ns	1
Maximum SMBus Operating Frequency	$F_{SMBUS}$	Block Mode		100	kHz	1

### Notes on Electrical Characteristics:

- <sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.
- <sup>2</sup>Slew rate measured through Vswing centered around differential zero
- <sup>3</sup> $V_{xabs}$  is defined as the voltage where  $CLK = CLK\#$
- <sup>4</sup>Only applies to the differential rising edge (CLK rising and CLK# falling)
- <sup>5</sup>Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.
- <sup>6</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz
- <sup>7</sup>Operation under these conditions is neither implied, nor guaranteed.

## Clock Periods Differential Outputs with Spread Spectrum Enabled

Measurement Window	1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock	Units	Notes
Symbol	Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition	Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
	Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum		
Signal Name	SRC 100	9.87400	9.99900	9.99900	10.00000	10.00100	10.05130	10.17630	ns 1,2
	CPU 100	9.91400	9.99900	9.99900	10.00000	10.00100	10.05130	10.13630	ns 1,2
	CPU 133	7.41425	7.49925	7.49925	7.50000	7.50075	7.53845	7.62345	ns 1,2
	CPU 166	5.91440	5.99940	5.99940	6.00000	6.00060	6.03076	6.11576	ns 1,2
	DOT 96	10.16560		10.41560	10.41670	10.41770		10.66770	ns 1,2

## Clock Periods Differential Outputs with Spread Spectrum Disabled

Measurement Window	1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock	Units	Notes
Symbol	Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition	Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
	Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum		
Signal Name	SRC 100	9.87400		9.99900	10.00000	10.00100		10.17630	ns 1,2
	CPU 100	9.91400		9.99900	10.00000	10.00100		10.13630	ns 1,2
	CPU 133	7.41425		7.49925	7.50000	7.50075		7.62345	ns 1,2
	CPU 166	5.91440		5.99940	6.00000	6.00060		6.11576	ns 1,2
	DOT 96	10.16560		10.41560	10.41670	10.41770		10.66770	ns 1,2

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REfout is at 14.31818MHz

**Table 1: CPU Frequency Select Table**

FS <sub>LC</sub> <sup>1</sup>	FS <sub>LB</sub> <sup>1</sup>	CPU MHz	SRC MHz	DOT MHz	LCD MHz	REF MHz
0	0	133.33	100.00	96.00	100.00	14.318
0	1	166.67				
1	0	100.00				
1	1	66.67				

1. FS<sub>LC</sub> is a low-threshold input. Please see V<sub>IL\_FS</sub> and V<sub>IH\_FS</sub> specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.

**Table 2: LCD Spread Select Table (Pin 20/21)**

B1b5	B1b4	B1b3	Spread %	Comment
0	0	0	-0.5%	LCD100
0	0	1	-1%	LCD100
0	1	0	-2%	LCD100
0	1	1	-2.5%	LCD100
1	0	0	+/- 0.25%	LCD100
1	0	1	+/-0.5%	LCD100
1	1	0	+/-1%	LCD100
1	1	1	+/-1.25%	LCD100

**Table 3: CPU N-step Programming**

CPU (MHz)	P	Default N (hex)	Fcpu
133.33	3	64	= 4MHz x N/P
166.67	3	7D	= 4MHz x N/P
100.00	4	64	= 4MHz x N/P
200.00	2	64	= 4MHz x N/P

**CPU Power Management Table**

PD	CPU_STOP#	SMBus Register OE	CPU	CPU#
0	1	Enable	Running	Running
1	X	Enable	Low/20K	Low
0	0	Enable	High	Low
0	X	Disable	Low/20K	Low

**SRC, LCD, DOT Power Management Table**

PD	CR_x#	SMBus Register OE	SRC	SRC#	DOT/LCD	DOT#/LCD#
0	0	Enable	Running	Running	Running	Running
1	X	X	Low/20K	Low	Low/20K	Low
0	1	Enable	Low/20K	Low	Running	Running
0	X	Disable	Low/20K	Low	Low/20K	Low

**REF Power Management Table**

PD	SMBus Register OE	REF
0	Enable	Running
1	X	Low
0	Disable	Low

## General SMBus serial interface information for the ICS9EMS9633

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address  $D2_{(h)}$
- ICS clock will **acknowledge**
- Controller (host) sends the begining byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address  $D2_{(h)}$
- ICS clock will **acknowledge**
- Controller (host) sends the begining byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address  $D3_{(h)}$
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if  $X_{(h)}$  was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

### Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
	Slave Address $D2_{(h)}$	
WR	WRite	
		ACK
Beginning Byte = N		ACK
		ACK
Data Byte Count = X		ACK
Beginning Byte N	X Byte	ACK
○		ACK
○		○
○		○
○		○
Byte N + X - 1		ACK
P	stoP bit	

### Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
	Slave Address $D2_{(h)}$	
WR	WRite	
		ACK
Beginning Byte = N		ACK
		ACK
RT	Repeat starT	
	Slave Address $D3_{(h)}$	
RD	ReaD	
		ACK
		Data Byte Count = X
	ACK	Beginning Byte N
		○
		○
		○
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

Byte 0 PLL & Divider Enable Register

Bit(s)	Pin #	Name	Description	Type	0	1	Default
7	-	PLL1 Enable	This bit controls whether the PLL driving the CPU and SRC clocks is enabled or not.	RW	0 = Disabled	1 = Enabled	1
6	-	PLL2 Enable	This bit controls whether the PLL driving the DOT and clock is enabled or not.	RW	0 = Disabled	1 = Enabled	1
5	-	PLL3 Enable	This bit controls whether the PLL driving the LCD clock is enabled or not.	RW	0 = Disabled	1 = Enabled	1
4	-	Reserved					0
3	-	CPU Divider Enable	This bit controls whether the CPU output divider is enabled or not. <b>NOTE:</b> This bit should be automatically set to '0' if bit 7 is set to '0'.	RW	0 = Disabled	1 = Enabled	1
2	-	SRC Output Divider Enable	This bit controls whether the SRC output divider is enabled or not. <b>NOTE:</b> This bit should be automatically set to '0' if bit 7 is set to '0'.	RW	0 = Disabled	1 = Enabled	1
1	-	LCD Output Divider Enable	This bit controls whether the LCD output divider is enabled or not. <b>NOTE:</b> This bit should be automatically set to '0' if bit 5 is set to '0'.	RW	0 = Disabled	1 = Enabled	1
0	-	DOT Output Divider Enable	This bit controls whether the DOT output divider is enabled or not. <b>NOTE:</b> This bit should be automatically set to '0' if bit 6 is set to '0'.	RW	0 = Disabled	1 = Enabled	1

Byte 1 PLL SS Enable/Control Register

Bit(s)	Pin #	Name	Description	Type	0	1	Default			
7		PLL1 SS Enable	This bit controls whether PLL1 has spread enabled or not. Spread spectrum for PLL1 is set at -0.5% down-spread. Note that PLL1 drives the CPU and SRC clocks.	RW	0 = Disabled	1 = Enabled	1			
6		PLL3 SS Enable	This bit controls whether PLL3 has spread enabled or not. Note that PLL3 drives the SSC clock, and that the spread spectrum amount is set in bits 3-5.	RW	0 = Disabled	1 = Enabled	1			
5		PLL3 FS Select	These 3 bits select the frequency of PLL3 and the SSC clock when Byte 1 Bit 6 (PLL3 Spread Spectrum Enable) is set.	RW	See Table 2: LCD Spread Select Table	0				
4						0				
3						0				
2		Reserved				0				
1		Reserved				0				
0		Reserved				0				

Byte 2 Output Enable Register

Bit(s)	Pin #	Name	Description	Type	0	1	Default
7		CPU0 Enable	This bit controls whether the CPU[0] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
6		CPU1 Enable	This bit controls whether the CPU[1] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
5		CPU2 Enable	This bit controls whether the CPU[2] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
4		SRC0 Enable	This bit controls whether the SRC[0] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
3		SRC1 Enable	This bit controls whether the SRC[1] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
2		SRC2 Enable	This bit controls whether the SRC[2] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
1		DOT Enable	This bit controls whether the DOT output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
0		LCD100 Enable	This bit controls whether the LCD output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1

Byte 3 Output Control Register

Bit(s)	Pin #	Name	Description	Type	0	1	Default
7			Reserved				0
6			Reserved				0
5		REF Enable	This bit controls whether the REF output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
4		REF Slew	These bits control the edge rate of the REF clock.	RW	00 = Slow Edge Rate 01 = Medium Edge Rate 10 = Fast Edge Rate 11 = Reserved		10
3							
2		CPU0 Stop Enable	This bit controls whether the CPU[0] output buffer is free-running or stoppable. If it is set to stoppable the CPU[0] output buffer will be disabled with the assertion of CPU_STP#.	RW	Free Running	Stoppable	0
1		CPU1 Stop Enable	This bit controls whether the CPU[1] output buffer is free-running or stoppable. If it is set to stoppable the CPU[1] output buffer will be disabled with the assertion of CPU_STP#.	RW	Free Running	Stoppable	0
0		CPU2 Stop Enable	This bit controls whether the CPU[2] output buffer is free-running or stoppable. If it is set to stoppable the CPU[2] output buffer will be disabled with the assertion of CPU_STP#.	RW	Free Running	Stoppable	0

Byte 4 CPU PLL N Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				1
Bit 6			Reserved				1
Bit 5			Reserved				1
Bit 4			Reserved				1
Bit 3			Reserved				1
Bit 2			Reserved				1
Bit 1			Reserved				1
Bit 0		CPU N Div8	N Divider Prog bit 8	RW			0

Byte 5 CPU PLL/N Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		CPU N Div7	See Table 3: CPU N-step Programming	RW	Default depends on latched input frequency.	X	X
Bit 6		CPU N Div6		RW			
Bit 5		CPU N Div5		RW			
Bit 4		CPU N Div4		RW			
Bit 3		CPU N Div3		RW	Default for CPU = 166 is 7Dh. Default for all other frequencies is 64h.	X	X
Bit 2		CPU N Div2		RW			
Bit 1		CPU N Div1		RW			
Bit 0		CPU N Div0		RW			

Byte 6 Reserved

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				1
Bit 6			Reserved				1
Bit 5			Reserved				1
Bit 4			Reserved				1
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				1
Bit 0			Reserved				1

Byte 7 Reserved

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				0
Bit 6			Reserved				0
Bit 5			Reserved				0
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				0
Bit 0			Reserved				0

Byte 8 Reserved

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				0
Bit 6			Reserved				0
Bit 5			Reserved				0
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				0
Bit 0			Reserved				0

Byte 9 LCD100 PLL N Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		LCD100 N Div7	N Divider Programming Byte9 bit(7:0) and Byte8 bit7	R	See N-step programming formula	X	
Bit 6		LCD100 N Div6		R		X	
Bit 5		LCD100 N Div5		R		X	
Bit 4		LCD100 N Div4		R		X	
Bit 3		LCD100 N Div3		R		X	
Bit 2		LCD100 N Div2		R		X	
Bit 1		LCD100 N Div1		R		X	
Bit 0		LCD100 N Div0		R		X	

Byte 10 Status Readback Register

Bit(s)	Pin #	Name	Description	Type	0	1	Default
7	37	FSB	Frequency Select B	R	See Table 1: CPU Frequency Select Table	Latch	
6	9	FSC	Frequency Select C				Latch
5	24	CR0# Readbk	Real time CR0# State Indicator	R	CR0# is Low	CR0# is High	X
4	28	CR1# Readbk	Real time CR1# State Indicator	R	CR1# is Low	CR1# is High	X
3	36	CR2# Readbk	Real time CR2# State Indicator	R	CR2# is Low	CR2# is High	X
2			Reserved				0
1			Reserved				0
0			Reserved				0

Byte 11 Revision ID/Vendor ID Register

Bit(s)	Pin #	Name	Description	Type	0	1	Default
7		Rev Code Bit 3	Revision ID (0 for A rev)	R	Vendor specific	X	
6		Rev Code Bit 2		R		X	
5		Rev Code Bit 1		R		X	
4		Rev Code Bit 0		R		X	
3		Vendor ID bit 3	Vendor ID	R		0	
2		Vendor ID bit 2		R		0	
1		Vendor ID bit 1		R		0	
0		Vendor ID bit 0		R		1	

Byte 12 Device ID Register

Bit(s)	Pin #	Name	Description	Type	0	1	Default
7		DEV_ID3	Device ID MSB	R			0
6		DEV_ID2	Device ID 2	R			0
5		DEV_ID1	Device ID 1	R			1
4		DEV_ID0	Device ID LSB	R			1
3			Reserved				0
2			Reserved				0
1			Reserved				0
0			Reserved				0

Byte 13 Reserved Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				0
Bit 6			Reserved				0
Bit 5			Reserved				0
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				0
Bit 0			Reserved				0

Byte 14 Reserved Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				0
Bit 6			Reserved				0
Bit 5			Reserved				0
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				0
Bit 0			Reserved				0

Byte 15 Byte Count Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				0
Bit 6			Reserved				0
Bit 5		BC5	Byte Count 5	RW	Specifies Number of bytes to be read back during an SMBus read. Default is 0xF.		0
Bit 4		BC4	Byte Count 4	RW			0
Bit 3		BC3	Byte Count 3	RW			1
Bit 2		BC2	Byte Count 2	RW			1
Bit 1		BC1	Byte Count 1	RW			1
Bit 0		BC0	Byte Count LSB	RW			1

Bytes 16:40 are reserved

Byte 41 N Program Enable Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				0
Bit 6			Reserved				0
Bit 5			Reserved				0
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1		CPU N Enable	Enables CPU N programming	RW	Disabled	Enabled	0
Bit 0		LCD N Enable	Enables LCD N programming	RW	Disabled	Enabled	0

**Test Clarification Table**

Comments	HW		
	TEST_SEL HW PIN	TEST_MODE HW PIN	OUTPUT
<0.35V	X	NORMAL	
Power-up w/ TEST_SEL = 1 to enter test mode Cycle power to disable test mode TEST_MODE -->low Vth input TEST_MODE is a real time input	>0.7V	<0.35V	HI-Z
	>0.7V	>0.7V	REF/N

**MLF Top Mark Information (9EMS9633KILF)**

	48	47	46	45	44	43	42	41	40	39	38	37
1	●											36
2												35
3												34
4												33
5												32
6												31
7												30
8												29
9												28
10												27
11												26
12												25
	13	14	15	16	17	18	19	20	21	22	23	24

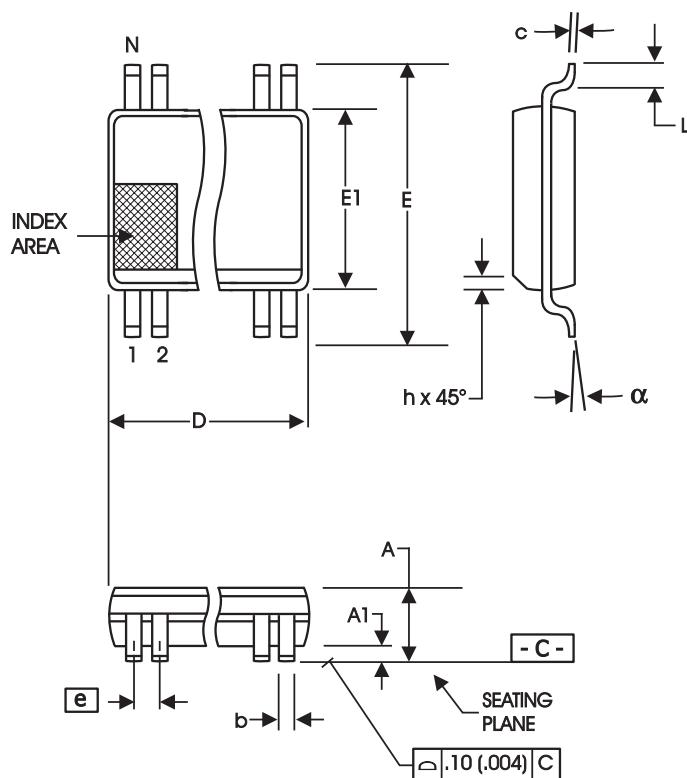
Line 1. Company name

Line 2. Part Number

Line 3. YYWW = Date Code

Line 3. Country of Origin

Line 4. ##### = Lot Number



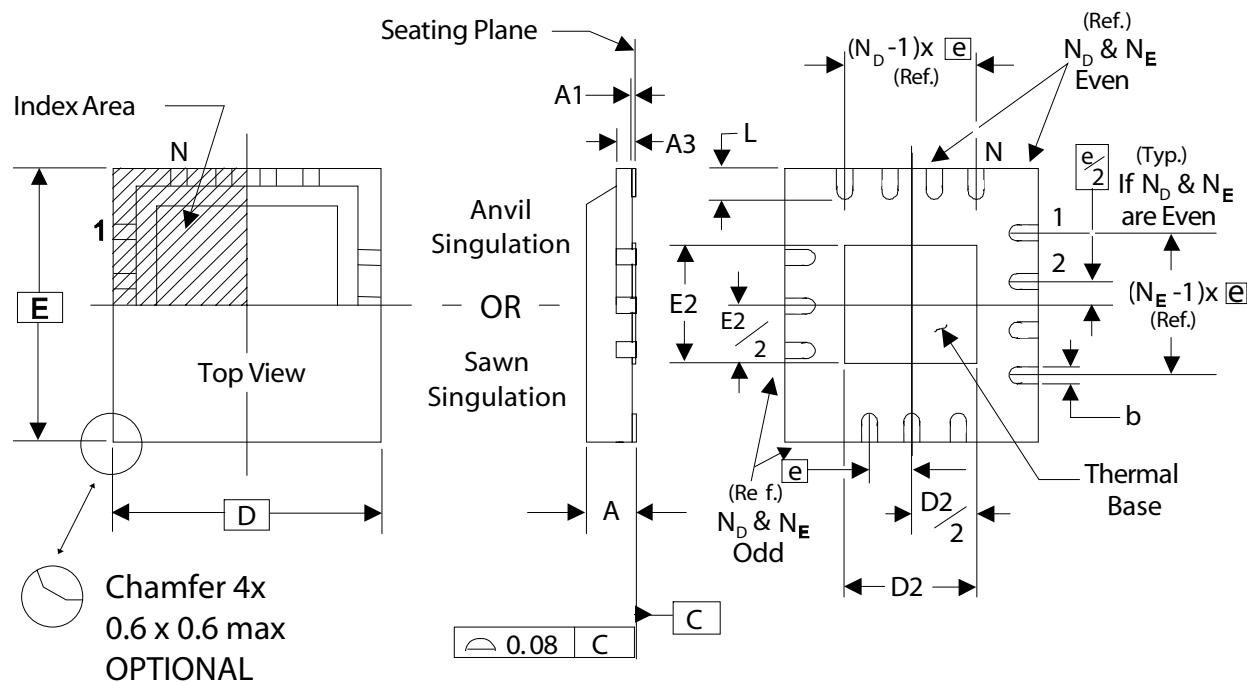
SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS MIN	COMMON DIMENSIONS MAX	COMMON DIMENSIONS MIN	COMMON DIMENSIONS MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS	SEE VARIATIONS	SEE VARIATIONS	SEE VARIATIONS
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS	SEE VARIATIONS	SEE VARIATIONS	SEE VARIATIONS
a	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034



THERMALLY ENHANCED, VERY THIN, FINE PITCH  
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.3
e	0.40 BASIC	

DIMENSIONS

SYMBOL	48L TOLERANCE
N	48
N <sub>D</sub>	12
N <sub>E</sub>	12
D x E BASIC	6.00 x 6.00
D2 MIN. / MAX.	3.95 / 4.25
E2 MIN. / MAX.	3.95 / 4.25
L MIN. / MAX.	0.30 / 0.50

Ordering Information

Part/Order Number	Shipping Packaging	Package	Temperature
9EMS9633BKILF	Tubes	48-pin MLF	-40 to +85° C
9EMS9633BKILFT	Tape and Reel	48-pin MLF	-40 to +85° C
9EMS9633BFILF	Tubes	48-pin SSOP	-40 to +85° C
9EMS9633BFILFT	Tape and Reel	48-pin SSOP	-40 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.  
Due to package size constraints, actual top-side marking may differ from the full orderable part number.

## Revision History

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