

## Description

The 9DMV0141 is a member of IDT's SOC-Friendly 1.8V Very-Low-Power (VLP) PCIe Gen1-2-3 family. It has integrated output terminations providing  $Z_0=100\Omega$  for direct connection to  $100\Omega$  transmission lines. The output has an OE# pin for optimal system control and power management. The part provides asynchronous or glitch-free switching modes.

## Typical Application

2:1 PCIe Gen1-2-3 Clock Multiplexer

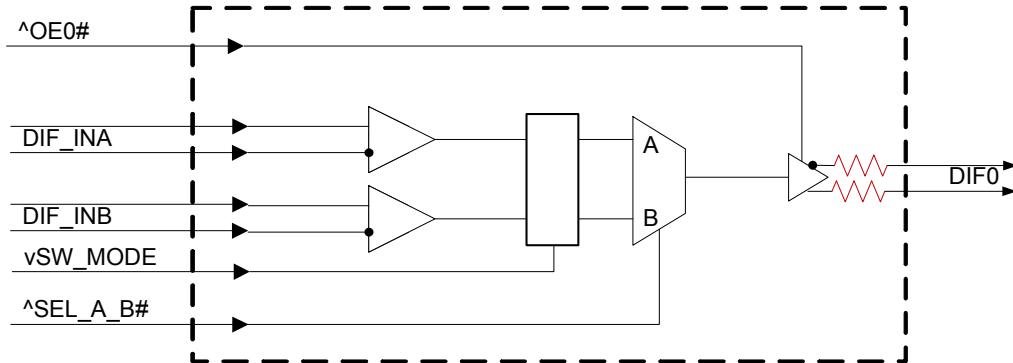
## Output Features

- 1 -Low-Power (LP) HCSL DIF pair w/ $Z_0=100\Omega$

## Key Specifications

- DIF *additive* cycle-to-cycle jitter <5ps
- DIF phase jitter is PCIe Gen1-2-3 compliant
- 125MHz additive phase jitter 420fs rms typical (12kHz to 20MHz)

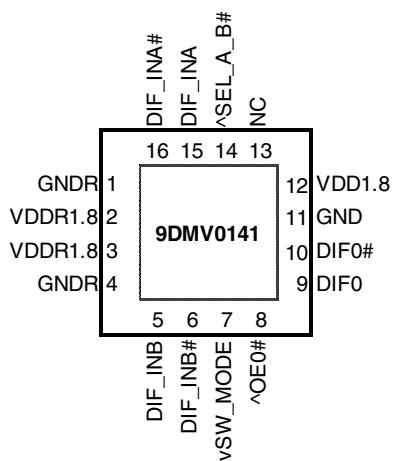
## Block Diagram



## Features

- LP-HCSL output w/integrated terminations; saves 4 resistors compared to standard HCSL output
- 1.8V operation; 12mW typical power consumption
- Selectable asynchronous or glitch-free switching; allows the mux to be selected at power up even if both inputs are not running, then transition to glitch-free switching mode
- Spread Spectrum Compatible; supports EMI reduction
- OE# pins; support DIF power management
- HCSL differential inputs; can be driven by common clock sources
- 1MHz to 200MHz operating frequency
- Configuration can be accomplished with strapping pins; SMBus interface not required for device control
- Space saving 16-pin 3x3mm VFQFPN; minimal board space

## Pin Configuration



**16-pin VFQFPN, 3x3 mm, 0.5mm pitch**

^ prefix indicates internal 120KOhm pull up resistor  
v prefix indicates internal 120KOhm pull down resistor

Note: Paddle may be connected to ground for thermal purposes. It is not required electrically.

### Power Management Table

OEx# Pin	DIF_IN	DIFx	
		True O/P	Comp. O/P
0	Running	Running	Running
1	Running	Low	Low

### Power Connections

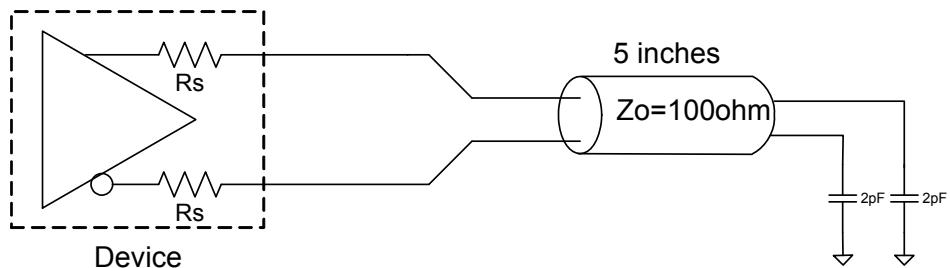
Pin Number		Description
VDD	GND	
2	1	Input A receiver analog
3	4	Input B receiver analog
12	11	DIF outputs

### Pin Descriptions

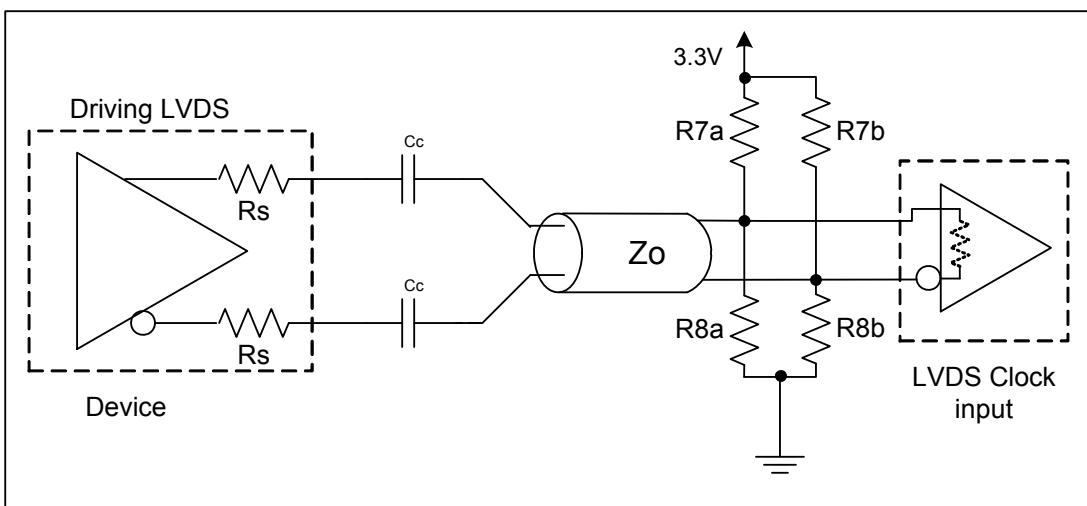
Pin#	Pin Name	Type	Pin Description
1	GNDR	GND	Analog Ground pin for the differential input (receiver)
2	VDDR1.8	PWR	1.8V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
3	VDDR1.8	PWR	1.8V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
4	GNDR	GND	Analog Ground pin for the differential input (receiver)
5	DIF_INB	IN	HCSL Differential True input
6	DIF_INB#	IN	HCSL Differential Complement Input
7	vSW_MODE	IN	Switch Mode. This pin selects either asynchronous or glitch-free switching of the mux. Use asynchronous mode if 0 or 1 of the input clocks is running. Use glitch-free mode if both input clocks are running. This pin has an internal pull down resistor of ~120kohms. 0 = asynchronous mode 1 = glitch-free mode
8	^OE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs
9	DIF0	OUT	Differential true clock output
10	DIF0#	OUT	Differential Complementary clock output
11	GND	GND	Ground pin.
12	VDD1.8	PWR	Power supply, nominal 1.8V
13	NC	N/A	No Connection.
14	^SEL_A_B#	IN	Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor. 0 = Input B selected, 1 = Input A selected.
15	DIF_INA	IN	HCSL Differential True input
16	DIF_INA#	IN	HCSL Differential Complement Input

## Test Loads

### Low-Power HCSL Differential Output Test Load



## Driving LVDS



### Driving LVDS inputs

Component	Value		Note
	Receiver has termination	Receiver does not have termination	
R7a, R7b	10K ohm	140 ohm	
R8a, R8b	5.6K ohm	75 ohm	
Cc	0.1 $\mu\text{F}$	0.1 $\mu\text{F}$	
Vcm	1.2 volts	1.2 volts	

## Electrical Characteristics—Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>DDxx</sub>	Applies to all V <sub>DD</sub> pins	-0.5		2.5	V	1,2
Input Voltage	V <sub>IN</sub>		-0.5		V <sub>DD</sub> +0.5V	V	1, 3
Input High Voltage, SMBus	V <sub>IHSMB</sub>	SMBus clock and data pins			3.6V	V	1
Storage Temperature	T <sub>S</sub>		-65		150	°C	1
Junction Temperature	T <sub>J</sub>				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

<sup>3</sup>Not to exceed 2.5V.

## Electrical Characteristics—Input/Supply/Common Parameters—Normal Operating Conditions

TA = T<sub>AMB</sub>, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>DDxx</sub>	Applies to all V <sub>DD</sub> pins	1.7	1.8	1.9	V	
Ambient Operating Temperature	T <sub>AMB</sub>	Industrial range	-40	25	85	°C	1
Input High Voltage	V <sub>IH</sub>	Single-ended inputs, except SMBus	0.75 V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V	
Input Low Voltage	V <sub>IL</sub>	Single-ended inputs, except SMBus	-0.3		0.25 V <sub>DD</sub>	V	
Input Current	I <sub>IN</sub>	Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = V <sub>DD</sub>	-5		5	uA	
	I <sub>INP</sub>	Single-ended inputs V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors V <sub>IN</sub> = V <sub>DD</sub> ; Inputs with internal pull-down resistors	-200		200	uA	
Input Frequency	F <sub>byp</sub>		1		200	MHz	2
Pin Inductance	L <sub>pin</sub>				7	nH	1
Capacitance	C <sub>IN</sub>	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C <sub>INDIF IN</sub>	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C <sub>OUT</sub>	Output pin capacitance			6	pF	1
Clk Stabilization	T <sub>STAB</sub>	From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Input SS Modulation Frequency PCIe	f <sub>MODINPCle</sub>	Allowable Frequency for PCIe Applications (Triangular Modulation)	30		33	kHz	
Input SS Modulation Frequency non-PCIe	f <sub>MODIN</sub>	Allowable Frequency for non-PCIe Applications (Triangular Modulation)	0		66	kHz	
OE# Latency	t <sub>LATOE#</sub>	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	clocks	1,3
Tfall	t <sub>F</sub>	Fall time of single-ended control inputs			5	ns	1,2
Trise	t <sub>R</sub>	Rise time of single-ended control inputs			5	ns	1,2

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup>DIF\_IN input

## Electrical Characteristics—Clock Input Parameters

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	$V_{IHDF}$	Differential inputs (single-ended measurement)	300	750	1150	mV	1
Input Low Voltage - DIF_IN	$V_{ILDIF}$	Differential inputs (single-ended measurement)	$V_{SS} - 300$	0	300	mV	1
Input Common Mode Voltage - DIF_IN	$V_{COM}$	Common Mode Input Voltage	200		725	mV	1
Input Amplitude - DIF_IN	$V_{SWING}$	Peak to Peak value ( $V_{IHDF} - V_{ILDIF}$ )	300		1450	mV	1
Input Slew Rate - DIF_IN	$dv/dt$	Measured differentially	0.35		8	V/ns	1,2
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{DD}$ , $V_{IN} = GND$	-5		5	uA	
Input Duty Cycle	$d_{tin}$	Measurement from differential waveform	45	50	55	%	1
Input Jitter - Cycle to Cycle	$J_{DIFin}$	Differential Measurement	0		150	ps	1

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Slew rate measured through +/-75mV window centered around differential zero

## Electrical Characteristics—DIF Low-Power HCSL Outputs

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	$Trf$	Scope averaging on	1.8	3.0	4.2	V/ns	1,2,3
Slew rate matching	$\Delta Trf$	Slew rate matching, Scope averaging on		3	20	%	1,2,4
Voltage High	$V_{HIGH}$	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	783	850	mV	
Voltage Low	$V_{LOW}$		-150	26	150		
Max Voltage	$V_{max}$	Measurement on single ended signal using absolute value. (Scope averaging off)		790	1150	mV	
Min Voltage	$V_{min}$		-300	9			
$V_{swing}$	$V_{swing}$	Scope averaging off	300	1514		mV	1,2
Crossing Voltage (abs)	$V_{cross\_abs}$	Scope averaging off	250	393	550	mV	1,5
Crossing Voltage (var)	$\Delta V_{cross}$	Scope averaging off		12	140	mV	1,6

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Slew rate is measured through the  $V_{swing}$  voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

<sup>5</sup>  $V_{cross}$  is defined as voltage where  $Clock = Clock\#$  measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all  $V_{cross}$  measurements in any particular system. Note that this is a subset of  $V_{cross\_min/max}$  ( $V_{cross}$  absolute) allowed. The intent is to limit  $V_{cross}$  induced modulation by setting  $\Delta V_{cross}$  to be smaller than  $V_{cross}$  absolute.

## Electrical Characteristics—Current Consumption

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DDOP}$	VDD rails, All outputs active @100MHz		7.9	12	mA	
Disable Current	$I_{DDDIS}$	VDD rails, All outputs disabled Low/Low		1.5	2.5	mA	2

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Input clock stopped after outputs have parked Low/Low.

## Electrical Characteristics—Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle Distortion	$t_{DCD}$	Measured differentially, @100MHz	-1	-0.12	1	%	1,3
Skew, Input to Output	$t_{pdBYP}$	$V_T = 50\%$	1853	2409	3132	ps	1
Jitter, Cycle to cycle	$t_{j cyc-cyc}$	Additive Jitter		0.1	5	ps	1,2

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Duty cycle distortion is the difference in duty cycle between the output and the input clock.

## Electrical Characteristics—Phase Jitter Parameters

TA =  $T_{AMB}$ , Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Additive Phase Jitter, Bypass Mode	$t_{jphPCleG1}$	PCIe Gen 1		1.3	5	N/A	ps (p-p)	1,2,3,5
	$t_{jphPCleG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.1	0.3	N/A	ps (rms)	1,2,3,4,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.1	0.2	N/A	ps (rms)	1,2,3,4
	$t_{jphPCleG3}$	PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)		0.065	0.1	N/A	ps (rms)	1,2,3,4
	$t_{jph125M0}$	125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		284	350	N/A	fs (rms)	1,6
	$t_{jph125M1}$	125MHz, 12KHz to 20MHz, -20dB/decade rollover < 12kHz, -40db/decade rolloff > 20MHz		420	500	N/A	fs (rms)	1,6

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> See <http://www.pcisig.com> for complete specs

<sup>3</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

<sup>4</sup> For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter =  $\text{SQRT}[(\text{total jitter})^2 - (\text{input jitter})^2]$

<sup>5</sup> Driven by 9FGV0831 or equivalent

<sup>6</sup> Driven by Rohde & Schwartz SMA100

## Marking Diagram



### Notes:

1. "XXX" is the last 3 characters of the lot number.
2. "YYWW" is the last two digits of the year and week that the part was assembled.
3. Line 3: truncated part number
4. "L" denotes RoHS compliant package.
5. "I" denotes industrial temperature grade.

## Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	$\theta_{JC}$	Junction to Case	NLG16	66	°C/W	1
	$\theta_{Jb}$	Junction to Base		5	°C/W	1
	$\theta_{JA0}$	Junction to Air, still air		63	°C/W	1
	$\theta_{JA1}$	Junction to Air, 1 m/s air flow		56	°C/W	1
	$\theta_{JA3}$	Junction to Air, 3 m/s air flow		51	°C/W	1
	$\theta_{JA5}$	Junction to Air, 5 m/s air flow		49	°C/W	1

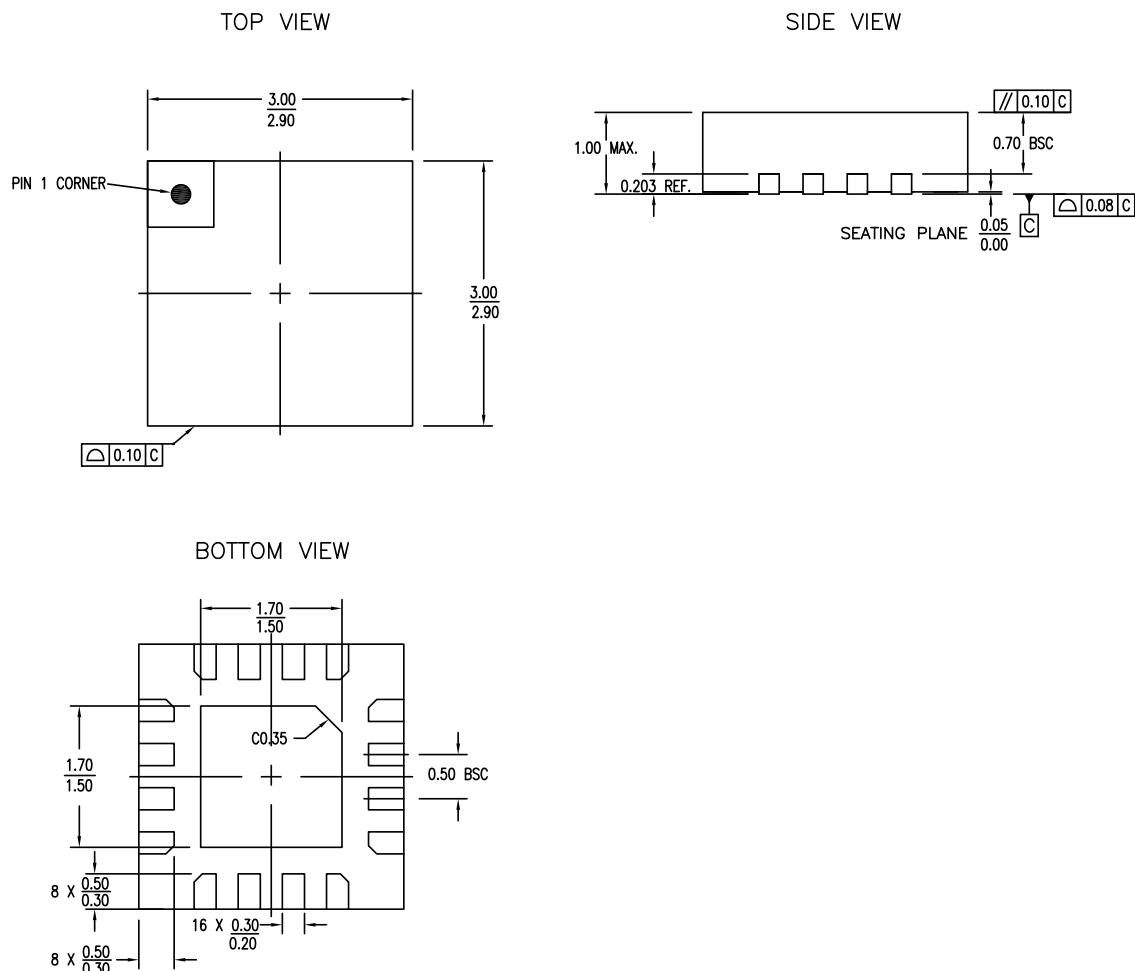
<sup>1</sup>ePad soldered to board

## Package Outline and Dimensions (NLG16P2)



## 16-QFN Package Outline Drawing

3.0 x 3.0 x 1.0 mm, 0.5 mm Pitch 16-QFN, 1.70 x 1.70 mm Epad  
NL/NLG16P2, PSC-4169-02, Rev 02, Page 1



## NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. TOP DOWN VIEW-AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

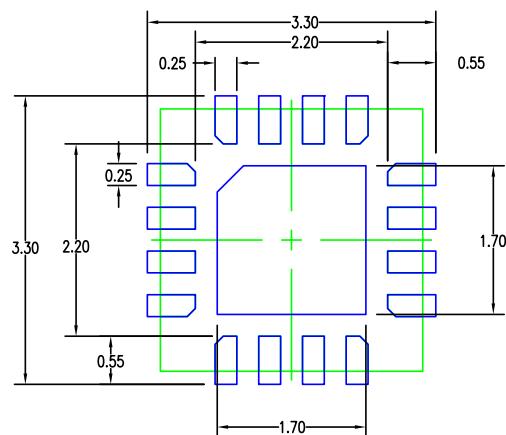
## Package Outline and Dimensions (NLG16P2), cont.



## 16-QFN Package Outline Drawing

3.0 x 3.0 x 1.0 mm, 0.5 mm Pitch 16-QFN, 1.70 x 1.70 mm Epad

NL/NLG16P2, PSC-4169-02, Rev 02, Page 2



RECOMMENDED LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Jul 28, 2017	Rev 02	New format
Feb 27, 2017	Rev 01	Change "L" Tolerance from 0.05 to 0.10

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## Ordering Information

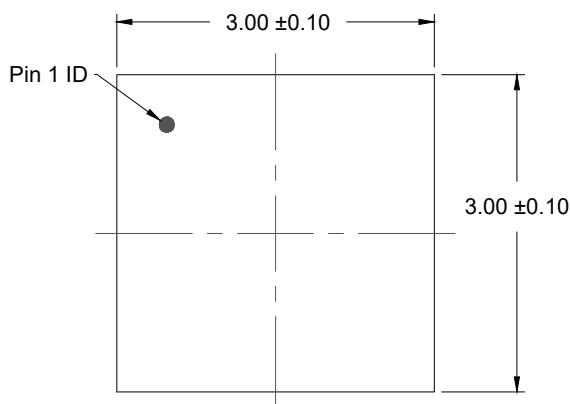
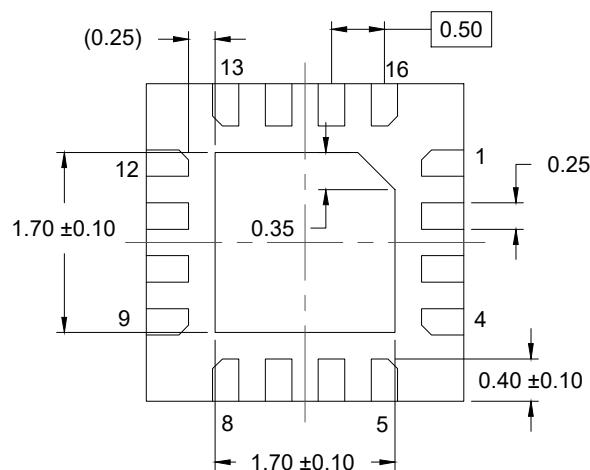
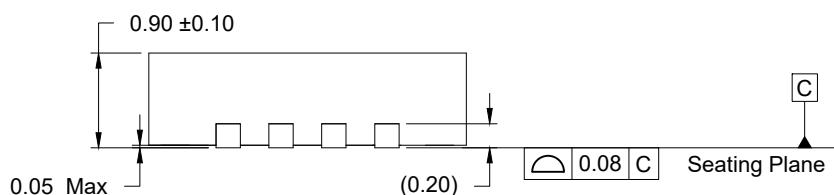
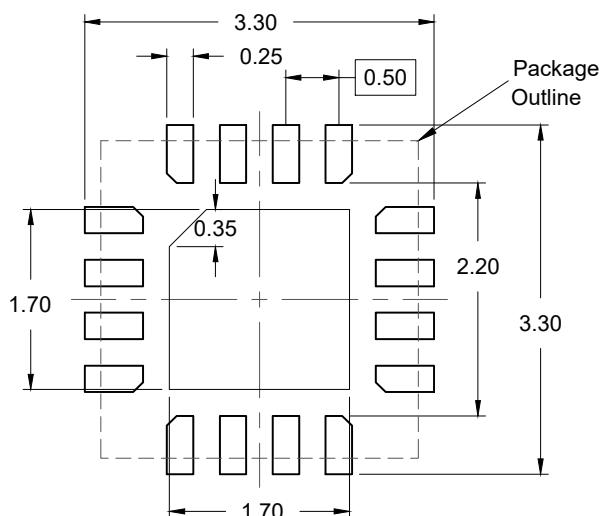
Part / Order Number	Shipping Packaging	Package	Temperature
9DMV0141AKILF	Trays	16-pin VFQFPN	-40 to +85° C
9DMV0141AKILFT	Tape and Reel	16-pin VFQFPN	-40 to +85° C

“LF” to the suffix denotes Pb-Free configuration, RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

## Revision History

Rev.	Initiator	Issue Date	Description	Page #
A	RDW	9/29/2014	1. Update front page text and electrical tables with char data. 2. Update pinout diagram with note about package paddle. 3. Move to final.	Various
B	RDW	1/26/2015	Updated package drawing to the latest NLG16 document.	8
C	RDW	5/11/2007	Updated package drawing to the latest NLG16 document.	8,9
D	RDW	8/15/2017	Updated package drawing to NLG16P2 document.	8,9


TOP VIEW

BOTTOM VIEW

SIDE VIEW

RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

**NOTES:**

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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