

Description

The 9DMV0131B/9DMV0141B are 1.8V members of IDT's full-featured PCIe clock family. The 9DMV0131B uses external series resistors for maximum flexibility, while the 9DMV0141B integrates output terminations for direct connection to 100Ω transmission lines. An OE# pin provides optimal system control and power management. The parts provide asynchronous or glitch-free switching modes.

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Typical Applications

- Servers
- nVME drives
- Embedded systems/Industrial control
- High-performance computing
- Accelerators

Key Specifications

- Additive cycle-to-cycle jitter < 5ps
- Additive PCIe Gen5 phase jitter < 38fs RMS
- 156.25MHz additive phase jitter 130fs RMS typical (12kHz to 20MHz)

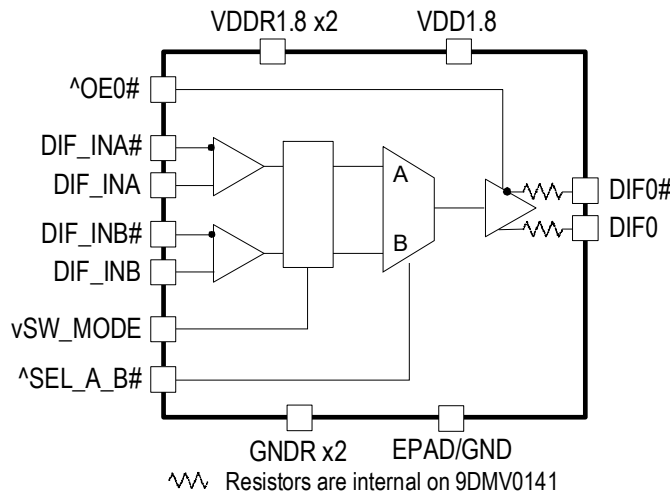
Features

- Direct connection to 100Ω loads saves 4 resistors (9DMV0141B)
- External series resistors allow use in 85Ω or 100Ω systems (9DMV0131B)
- 1.8V operation; 12mW typical power consumption
- Selectable asynchronous or glitch-free switching; allows the mux to be selected at power up even if both inputs are not running, then transition to glitch-free switching mode
- OE# pin for flexible power sequencing
- HCSL differential inputs
- Spread spectrum tolerant; allows reduction of EMI
- 1MHz to 200MHz operating frequency
- Configuration accomplished with strapping pins, no SMBus needed
- Space-saving 3 × 3 mm 16-VFQFPN; minimal board space

Output Features

- 1 Low-Power HCSL (LP-HCSL) DIF pair

Block Diagram

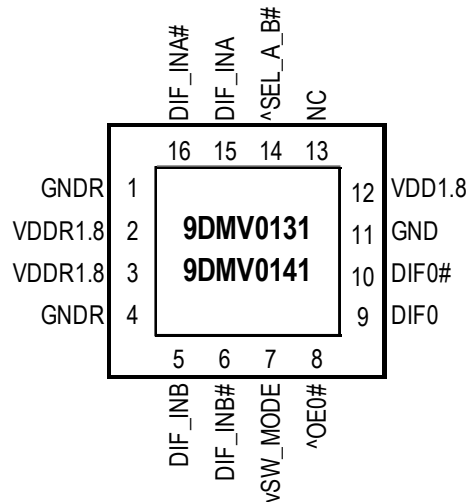


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Pin Assignments

Figure 1. Pin Assignments for 3 × 3 mm 16-VFQFPN Package – Top View



16-VFQFPN, 3 x 3 mm, 0.5mm pitch

^ prefix indicates internal 120kOhm pull-up resistor
 v prefix indicates internal 120kOhm pull-down resistor

Note: Paddle may be connected to ground for thermal purposes. It is not required electrically.

Pin Descriptions

Table 1. Pin Descriptions

| Number | Name | Type | Description |
|--------|----------|--------|---|
| 1 | GNDR | GND | Analog ground pin for the differential input (receiver). |
| 2 | VDDR1.8 | Power | Power supply for differential input clock (receiver). This V_{DD} should be treated as an analog power rail and filtered appropriately. Nominally 1.8V. |
| 3 | VDDR1.8 | Power | Power supply for differential input clock (receiver). This V_{DD} should be treated as an analog power rail and filtered appropriately. Nominally 1.8V. |
| 4 | GNDR | GND | Analog ground pin for the differential input (receiver). |
| 5 | DIF_INB | Input | True input of differential clock. |
| 6 | DIF_INB# | Input | Complement input of differential clock. |
| 7 | vSW_MODE | Input | Switch Mode. This pin selects either asynchronous or glitch-free switching of the mux. Use asynchronous mode if 0 or 1 of the input clocks is running. Use glitch-free mode if both input clocks are running. This pin has an internal pull-down resistor and is dynamically configurable. 0 = asynchronous mode, 1 = glitch-free mode. |
| 8 | ^OE0# | Input | Active low input for enabling output 0. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output. |
| 9 | DIF0 | Output | Differential true clock output. |
| 10 | DIF0# | Output | Differential complementary clock output. |
| 11 | GND | GND | Ground pin. |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|--------|-----------|-------|---|
| 12 | VDD1.8 | Power | Power supply, nominally 1.8V. |
| 13 | NC | — | No connection. |
| 14 | ^SEL_A_B# | Input | Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor. 0 = Input B selected, 1 = Input A selected. |
| 15 | DIF_INA | Input | True input of differential clock. |
| 16 | DIF_INA# | Input | Complement input of differential clock. |

Table 2. Power Management

| OEx# Pin | DIF_IN | DIFx | |
|----------|---------|----------|-------------------|
| | | True O/P | Complementary O/P |
| 0 | Running | Running | Running |
| 1 | Running | Low | Low |

Table 3. Power Connections

| Pin Number | | Description |
|-----------------|-----|--------------------------|
| V _{DD} | GND | |
| 2 | 1 | Input A receiver analog. |
| 3 | 4 | Input B receiver analog. |
| 12 | 11 | DIF outputs, |

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9DMV0131B/9DMV0141B at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 4. Absolute Maximum Ratings

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit | Notes |
|-----------|----------------------|-------------------------------|---------|---------|-----------------|------|-------|
| V_{DDx} | Supply Voltage | Applies to all V_{DD} pins. | -0.5 | | 2.5 | V | 1,2 |
| V_{IN} | Input Voltage | | -0.5 | | $V_{DD} + 0.5V$ | V | 1,3 |
| T_s | Storage Temperature | | -65 | | 150 | °C | 1 |
| T_j | Junction Temperature | | | | 125 | °C | 1 |
| ESD prot | Input ESD protection | Human Body Model. | 2000 | | | V | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Operation under these conditions is neither implied nor guaranteed.

³ Not to exceed 2.5V.

Thermal Characteristics

Table 5. Thermal Characteristics

| Symbol | Parameter | Conditions | Package | Value | Unit | Notes |
|----------------|--------------------|---------------------------------|---------|-------|------|-------|
| θ_{JC} | Thermal Resistance | Junction to case. | NLG16 | 66 | °C/W | 1 |
| θ_{JB} | | Junction to board. | | 5 | °C/W | 1 |
| θ_{JA0} | | Junction to air, still air. | | 63 | °C/W | 1 |
| θ_{JA1} | | Junction to air, 1m/s air flow. | | 56 | °C/W | 1 |
| θ_{JA2} | | Junction to air, 3m/s air flow. | | 51 | °C/W | 1 |
| θ_{JA3} | | Junction to air, 5m/s air flow. | | 49 | °C/W | 1 |

¹ EPAD soldered to board.

Electrical Characteristics

$T_A = T_{AMB}$, supply voltages per normal operating conditions. See [Test Loads](#) for loading conditions.

Table 6. Electrical Characteristics–Input/Supply/Common Parameters – Normal Operating Condition

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units | Notes |
|-----------------|--|---|---------------|---------|----------------|---------|-------|
| V_{DDxx} | Supply Voltage | Applies to all V_{DD} pins. | 1.7 | 1.8 | 1.9 | V | |
| T_{AMB} | Ambient Operating Temperature | Industrial range. | -40 | 25 | 85 | °C | 1 |
| V_{IH} | Input High Voltage | Single-ended inputs, except SMBus. | $0.75 V_{DD}$ | | $V_{DD} + 0.3$ | V | |
| V_{IL} | Input Low Voltage | Single-ended inputs, except SMBus. | -0.3 | | $0.25 V_{DD}$ | V | |
| I_{IN} | Input Current | Single-ended inputs, $V_{IN} = GND$, $V_{IN} = V_{DD}$. | -5 | | 5 | μA | |
| I_{INP} | | Single-ended inputs. $V_{IN} = 0 V$; Inputs with internal pull-up resistors. $V_{IN} = V_{DD}$; Inputs with internal pull-down resistors. | -100 | | 100 | μA | |
| F_{ibyp} | Input Frequency | | 1 | | 200 | MHz | 2 |
| L_{pin} | Pin Inductance | | | | 7 | nH | 1 |
| C_{IN} | Capacitance | Logic Inputs, except DIF_IN. | 1.5 | | 5 | pF | 1 |
| C_{INDIF_IN} | | DIF_IN differential clock inputs. | 1.5 | | 2.7 | pF | 1,4 |
| C_{OUT} | | Output pin capacitance. | | | 6 | pF | 1 |
| T_{STAB} | Clk Stabilization | From V_{DD} power-up and after input clock stabilization or de-assertion of PD# to 1st clock. | | | 1 | ms | 1,2 |
| $f_{MODINPCle}$ | Input SS Modulation Frequency PCIe | Allowable frequency for PCIe applications (triangular modulation). | 30 | | 33 | kHz | |
| f_{MODIN} | Input SS Modulation Frequency non-PCIe | Allowable frequency for non-PCIe applications (triangular modulation). | 0 | | 66 | kHz | |
| $t_{LATO\#}$ | OE# Latency | DIF start after OE# assertion. DIF stop after OE# deassertion. | 1 | 2 | 3 | clocks | 1,3 |
| t_F | Tfall | Fall time of single-ended control inputs. | | | 5 | ns | 1,2 |
| t_R | Trise | Rise time of single-ended control inputs. | | | 5 | ns | 1,2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV.

⁴ DIF_IN input.

Table 7. Clock Input Parameters

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit | Notes |
|-------------|----------------------------------|--|---------|---------|---------|---------|-------|
| V_{CROSS} | Input Crossover Voltage – DIF_IN | Crossover voltage (common mode voltage). | 200 | | 725 | | |
| V_{SWING} | Input Swing–DIF_IN | Differential value. | 300 | | | mV | 1 |
| dv/dt | Input Slew Rate–DIF_IN | Measured differentially. | 0.6 | | | V/ns | 1,2 |
| I_{IN} | Input Leakage Current | $V_{IN} = 0.8V$, $V_{IN} = GND$. | -5 | | 5 | μA | |
| d_{tin} | Input Duty Cycle | Measurement from differential waveform. | 45 | | 55 | % | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through $\pm 75mV$ window centered around differential zero.

Table 8. DIF Low-Power HCSL Outputs

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit | Notes |
|--------------------|------------------------|---|---------|---------|---------|------|-------|
| T_{RF} | Slew Rate | Scope averaging on, 9DMV0141B | 2 | 2.9 | 4.0 | V/ns | 1,2,3 |
| ΔT_{RF} | Slew Rate Matching | Slew rate matching, scope averaging on. | | 3 | 20 | % | 1,4 |
| V_{HIGH} | Voltage High | Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on). | 660 | 783 | 850 | mV | |
| V_{LOW} | Voltage Low | | -150 | 26 | 150 | | |
| V_{MAX} | Max Voltage | Measurement on single ended signal using absolute value (scope averaging off). | | 790 | 1150 | mV | |
| V_{MIN} | Min Voltage | | -300 | 9 | | | |
| V_{CROSS_ABS} | Crossing Voltage (abs) | Scope averaging off. | 250 | 393 | 550 | mV | 1,5 |
| $\Delta-V_{CROSS}$ | Crossing Voltage (var) | Scope averaging off. | | 12 | 140 | mV | 1,6 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform.

³ Slew rate is measured through the V_{SWING} voltage range centered around differential 0V. This results in a $\pm 150mV$ window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a $\pm 75mV$ window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ V_{CROSS} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all V_{CROSS} measurements in any particular system. Note that this is a subset of $V_{CROSS-MIN/MAX}$ (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting $\Delta-V_{CROSS}$ to be smaller than V_{CROSS} absolute.

Table 9. Current Consumption

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit | Notes |
|--------------------|--------------------------|--|---------|---------|---------|------|-------|
| I _{DDOP} | Operating Supply Current | V _{DD} rails, all outputs active at 100MHz. | | 7.9 | 12 | mA | |
| I _{DDDIS} | Disable Current | V _{DD} rails, all outputs disabled Low/Low. | | 1.5 | 2.5 | mA | 2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Input clock stopped after outputs have parked Low/Low.

Table 10. Output Duty Cycle, Jitter, Skew and PLL Characteristics

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit | Notes |
|----------------------------------|------------------------|-------------------------------------|---------|---------|---------|------|-------|
| t _{DCD} | Duty Cycle Distortion | Measured differentially, at 100MHz. | -0.5 | -0.12 | 0.5 | % | 1,3 |
| t _{pdBYP} | Skew, Input to Output | V _T = 50%. | 1800 | 2409 | 3000 | ps | 1 |
| t _{j_{cyc-cyc}} | Jitter, Cycle to Cycle | Additive Jitter. | | | 5 | ps | 1,2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform.

³ Duty cycle distortion is the difference in duty cycle between the output and the input clock.

Table 11. PCIe Refclk Phase Jitter [1] [2]

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions. See [Test Loads](#) for loading conditions

| Symbol | Parameter | Conditions | Typical | Maximum | PCIe Specification | Unit |
|-----------------------------|---|-----------------------------|---------|---------|--------------------|----------|
| t _{jphPCIeG1-CC} | Additive PCIe Phase Jitter in Fan-out Buffer Mode (Common Clocked Architecture) SSC ≤ -0.5% | PCIe Gen1 (2.5 GT/s) | 1.7 | 3.0 | [5] | ps pk-pk |
| t _{jphPCIeG2-CC} | | PCIe Gen2 Hi Band (5 GT/s) | 0.122 | 0.199 | | ps RMS |
| t _{jphPCIeG3-CC} | | PCIe Gen2 Lo Band (5 GT/s) | 0.033 | 0.049 | | |
| t _{jphPCIeG4-CC} | | PCIe Gen3 (8 GT/s) | 0.059 | 0.098 | | |
| t _{jphPCIeG5-CC} | | PCIe Gen4 (16 GT/s) [3] [6] | 0.059 | 0.098 | | |
| | | PCIe Gen5 (32 GT/s) [3] [7] | 0.023 | 0.038 | | |
| t _{jphPCIeG1-SRIS} | Additive PCIe Phase Jitter in Fan-out Buffer Mode (SRIS Architecture) [4] SSC ≤ -0.3% | PCIe Gen1 (2.5 GT/s) | 0.175 | 0.275 | N/A | ps RMS |
| t _{jphPCIeG2-SRIS} | | PCIe Gen2 (5 GT/s) | 0.156 | 0.247 | | |
| t _{jphPCIeG3-SRIS} | | PCIe Gen3 (8 GT/s) | 0.041 | 0.064 | | |
| t _{jphPCIeG4-SRIS} | | PCIe Gen4 (16 GT/s) | 0.043 | 0.066 | | |
| t _{jphPCIeG5-SRIS} | | PCIe Gen5 (32 GT/s) | 0.036 | 0.059 | | |

¹ The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 7.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.

² Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.

- ³ SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
- ⁴ The PCI Express Base Specification 7.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
- ⁵ The RMS sum of the source jitter and the additive jitter must be less than the jitter specification listed for the clock generator operating mode.
- ⁶ Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
- ⁷ Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

Table 12. Non-PCIe Additive Phase Jitter

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions. See [Test Loads](#) for loading conditions

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit |
|--------------------------------------|----------------------------|---|---------|---------|---------|--------|
| Additive Phase Jitter ^[1] | t _{jph12k-20Madd} | 12kHz to 20MHz integration range, 156.25MHz carrier. ^[2] | — | 130 | — | fs RMS |

¹ Additive jitter for RMS values is calculated by solving for b, where $[b = \sqrt{c^2 - a^2}]$, "a" is RMS input jitter and "c" is RMS total jitter.

² Driven by SMA100B source.

Test Loads

Figure 2. Low-Power HCSL Output Test Load (standard PCIe source-terminated test load with high impedance receiver)

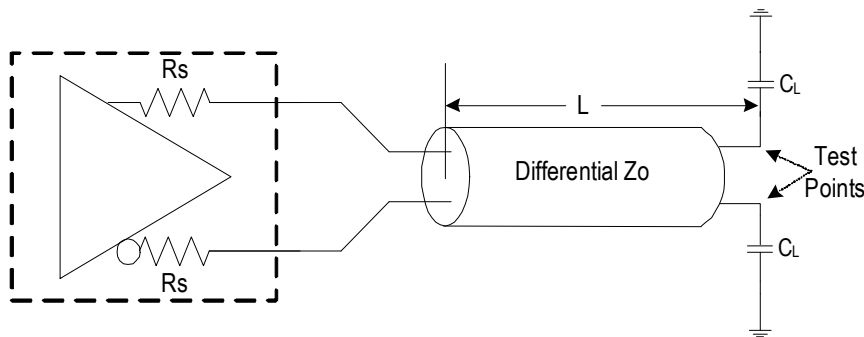


Table 13. Parameters for Low-Power HCSL Output Test Load

| Device | Rs (Ω) | Zo (Ω) | L (inches) | CL (pF) |
|----------|----------|--------|------------|---------|
| 9DMV0131 | 24 | 85 | 5 | 2 |
| | 33 | 100 | 5 | 2 |
| 9DMV0141 | Internal | 100 | 5 | 2 |

Alternate Terminations

The LP-HCSL output can easily drive other logic families. See application note ["AN-891"](#) for termination schemes for LVPECL, LVDS, CML, and SSTL.

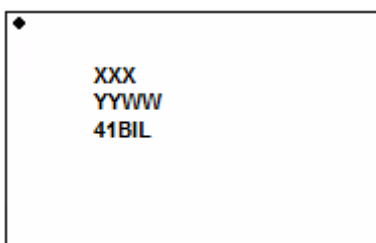
Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

Marking Diagrams



- Line 1: “XXX” is the Asm lot number.
- Line 2 indicates the following:
 - “YY” is the last two digits of the year; “WW” is the work week number when the part was assembled.
- Line 3: truncated part number.

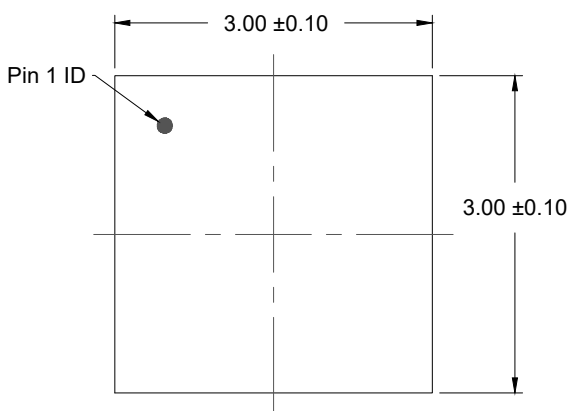


Ordering Information

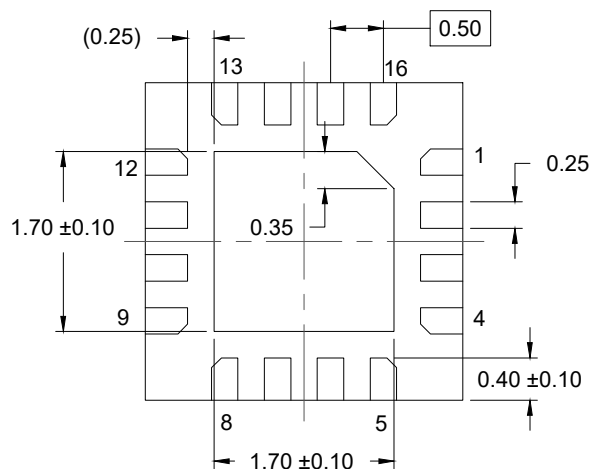
| Orderable Part Number | Description | Package | Carrier Type | Temperature Range |
|-----------------------|---------------------|---|---------------|-------------------|
| 9DMV0131BKILF | 85Ω or 100Ω systems | 3 × 3 × 0.9 mm, 16-VFQFPN | Tray | -40° to +85°C |
| 9DMV0131BKILFT | 85Ω or 100Ω systems | | Tape and Reel | -40° to +85°C |
| 9DMV0141BKILF | 100Ω systems | | Tray | -40° to +85°C |
| 9DMV0141BKILFT | 100Ω systems | | Tape and Reel | -40° to +85°C |

Revision History

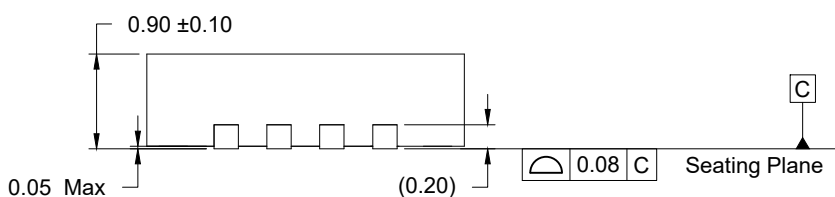
| Revision Date | Description of Change |
|-------------------|---|
| December 15, 2025 | Updated pin 7 description in Pin Descriptions . |
| May 25, 2021 | <ul style="list-style-type: none"> ▪ Updated Additive Phase Jitter bullet in Key Specifications for Gen5. ▪ Updated document title to "...PCIe Gen1-5..." ▪ Replaced Filtered Phase Jitter tables with PCIe Refclk Phase Jitter table. ▪ Replaced Unfiltered Phase Jitter table with Non-PCIe Additive Phase Jitter table. ▪ Updated Package Outline Drawings section, Marking Diagrams, and added POD link in the "Package" column in Ordering Information. |
| December 12, 2019 | Added 9DMV0131B information to datasheet. |
| February 25, 2019 | Initial release. |



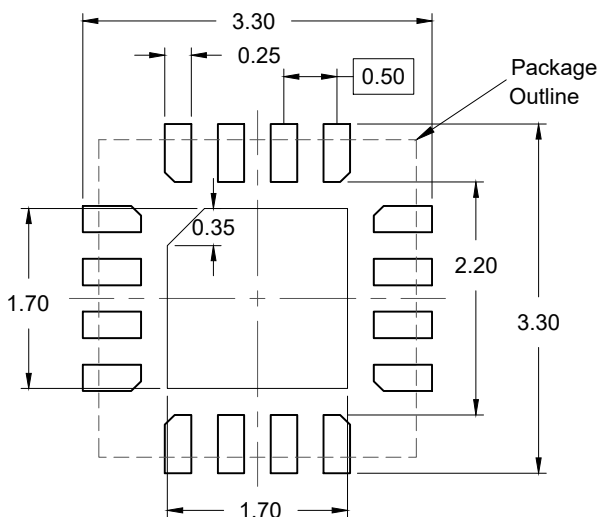
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.

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