Description

The 9DML4493A is a 4-input, 4-output clock multiplexer. It can also operate as a dual 2-input, 2-output clock multiplexer. It has very low additive phase jitter and is suitable for all PCIe data rates. The device supports today's complex system power sequencing requirements with Power Down Tolerant and Flexible Power Sequencing features.

Typical Applications

- Servers
- Storage
- Networking
- High-Performance computing
- Accelerators

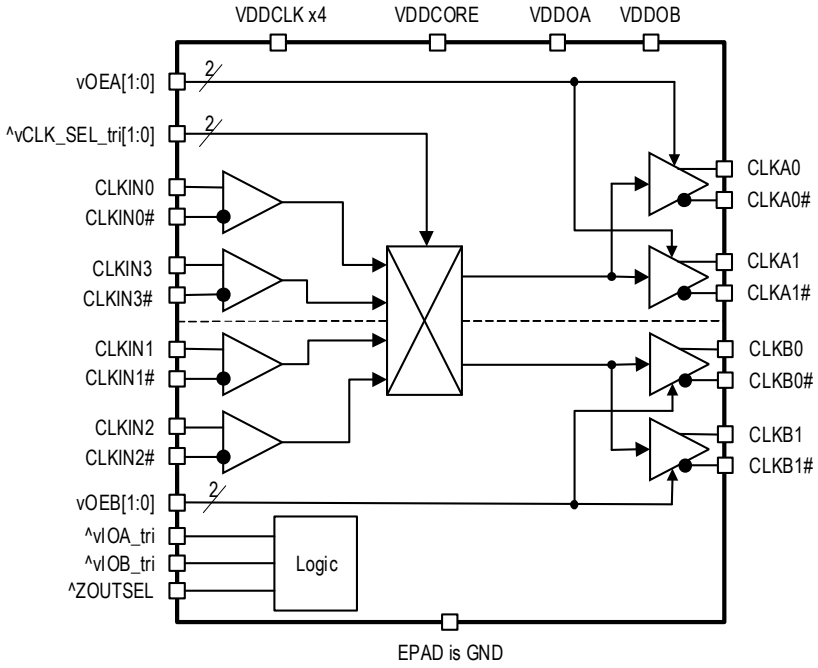
Key Specifications

- Additive phase jitter:
  - 5.1fs RMS typical (PCIe Gen7 CC at 100MHz)
  - 66fs RMS typical (12kHz–20MHz at 156.25M)
- Supports common Clocked (CC) and IR (SRIS, SRNS) timing architectures.
- Propagation delay < 1.2ns typical

Features

- Four differential inputs support LVPECL, LVDS, HCSL or LVCMOS reference clocks
- Flexible Power Sequencing (FPS) ensures good behavior when powered up without input clock, or when the input clock is present without power
- Power-Down Tolerant (PDT) inputs: CLK_SEL_tri, OE pins, IOA_tri, IOB_tri, ZOUTSEL may be driven when the 9DML4493 is not powered up
- Accepts input frequencies ranging from 1PPS (1Hz) to 350MHz
- Configured via pin straps - no serial bus needed
  - Pin-selectable 100Ω or 85Ω differential output impedance
  - Three pin-selectable output amplitudes per bank
  - Pin-selectable 4:4 mode or dual 2:2 MUX modes
- Glitch-free output enable pins for each output
- Spread-spectrum tolerant
- Voltage supply of 1.8V, 2.5V, or 3.3V
- -40°C to +85°C ambient operating temperature
- 5 × 5 mm 32-VFQFPN package

Block Diagram

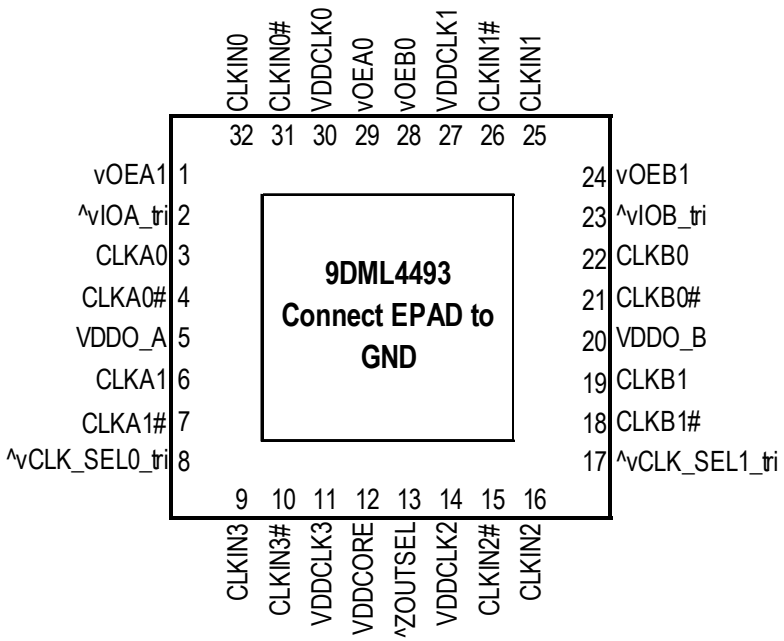


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Pin Assignments

Figure 1. Pin Assignments for 5 × 5 mm 32-VFQFPN Package – Top View



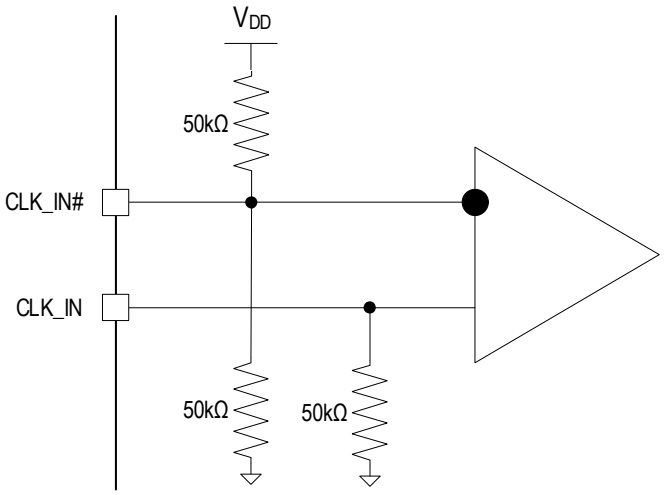
32-pin VFQFPN, 5 x 5 mm, 0.5mm pitch

^ prefix indicates internal pull-up resistor

v prefix indicates internal pull-down resistor

^v prefix indicates internal pull-up and pull-down resistor biasing to VDD/2

Clock Input Bias Network



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	vOEA1	Input	Active high input for enabling output 1 of bank A. This pin has internal pull-down. 0 =disable output low, 1 = enable output.
2	^vIOA_tri	Input	Sets nominal amplitude of Bank A outputs. This is a tri-level input with internal pull-up and pull down resistors. See Output Amplitude Select, High Impedance Loads table for details.
3	CLKA0	Output	True output of bank A clock 0.
4	CLKA0#	Output	Complementary output of bank A clock 0.
5	VDDO_A	Power	Power supply for output group A.
6	CLKA1	Output	True output of bank A clock 1.
7	CLKA1#	Output	Complementary output of bank A clock 1.
8	^vCLK_SEL0_tri	Input	Input clock selection pin. This is a tri-level input with internal pull-up and pull-down resistors that bias the pin to VDD/2 when left open. See the Input Select table for details.
9	CLKIN3	Input	True side of differential input clock 3.
10	CLKIN3#	Input	Complementary side of differential input clock 3.
11	VDDCLK3	Power	Power supply for clock input 3.
12	VDDCORE	Power	Power supply for core logic.
13	^ZOUTSEL	Input	Input to select differential output impedance. This input has an internal pull-up resistor. See the Output Impedance Select table for details.
14	VDDCLK2	Power	Power supply for clock input 2.
15	CLKIN2#	Input	Complementary side of differential input clock 2.
16	CLKIN2	Input	True side of differential input clock 2.
17	^vCLK_SEL1_tri	Input	Input clock selection pin. This is a tri-level input with internal pull-up and pull-down resistors that bias the pin to VDD/2 when left open. See the Input Select table for details.
18	CLKB1#	Output	Complementary output of bank B clock 1.
19	CLKB1	Output	True output of bank B clock 1.
20	VDDO_B	Power	Power supply for output group B.
21	CLKB0#	Output	Complementary output of bank B clock 0.
22	CLKB0	Output	True output of bank B clock 0.
23	^vIOB_tri	Input	Sets nominal amplitude of Bank B outputs. This is a tri-level input with internal pull-up and pull-down resistors. See Output Amplitude Select, High Impedance Loads table for details.
24	vOEB1	Input	Active high input for enabling output 1 of bank B. This pin has internal pull-down. 0 = disable output low, 1 = enable output.
25	CLKIN1	Input	True side of differential input clock 1.
26	CLKIN1#	Input	Complementary side of differential input clock 1.
27	VDDCLK1	Power	Power supply for clock input 1.
28	vOEB0	Input	Active high input for enabling output 0 of bank B. This pin has internal pull-down. 0 = disable output low, 1 = enable output.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
29	vOEA0	Input	Active high input for enabling output 0 of bank A. This pin has internal pull-down. 0 =disable output low, 1 = enable output.
30	VDDCLK0	Power	Power supply for clock input 0.
31	CLKIN0#	Input	Complementary side of differential input clock 0.
32	CLKIN0	Input	True side of differential input clock 0.
33	EPAD	GND	Connect to ground.

Table 2. Power Management

OExx Pin	CLKINx	CLKA[1:0], CLKB[1:0]	
		True Output	Complementary Output
1	Running	Running	Running
0	Running	Low	Low

Table 3. Power Connections

Pin Number		Description
VDD	GND	
5	33 (EPAD)	Output Bank A
11	33 (EPAD)	Input CLK3
12	33 (EPAD)	Core Logic
14	33 (EPAD)	Input CLK2
20	33 (EPAD)	Output Bank B
27	33 (EPAD)	Input CLK1
30	33 (EPAD)	Input CLK0

Table 4. Input Select

CLK_SEL0_tri	CLK_SEL1_tri	Description
0	0	CLK0 drives Bank A and B.
0	1	CLK1 drives Bank A and B.
1	0	CLK2 drives Bank A and B.
1	1	CLK3 drives Bank A and B.
M	M	Reserved.
M	0	CLK0 drives Bank A and CLK1 drives Bank B.

Table 4. Input Select (Cont.)

CLK_SEL0_tri	CLK_SEL1_tri	Description
M	1	CLK0 drives Bank A and CLK2 drives Bank B.
0	M	CLK3 drives Bank A and CLK1 drives Bank B.
1	M	CLK3 drives Bank A and CLK2 drives Bank B.

Table 5. Output Impedance Select

ZOUTSEL	Differential Output Impedance (Ω)
0	85 (42.5 single-ended)
1	100 (50 single-ended)

Table 6. Output Amplitude Select, High Impedance Loads

IOA_tri, IOB_tri	2.5V or 3.3V Operation	1.8V Operation
M	750mV nominal Vhigh	700mV nominal Vhigh
0	825mV nominal Vhigh	750mV nominal Vhigh
1	925mV nominal Vhigh	825mV nominal Vhigh

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9DML4493A at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Supply Voltage	V_{DDx}	With respect to ground.	-	-	3.63	V	1,2
Input Voltage	V_{IN}		-0.5	-	V_{DD} + 0.5	V	1
Continuous Current	I_O	CLK output pins.	-	-	40	mA	1
Surge Current	I_O	CLK output pins.	-	-	60	mA	1
Storage Temperature	T_S		-65	-	150	°C	1
Junction Temperature	T_J		-	-	125	°C	1
Soldering Temperature	T_{LD}	10 seconds maximum.	-	-	260	°C	1
Input ESD Protection	ESD Prot	Human Body Model.	2000	-	-	V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics

$T_A = T_{AMB}$, supply voltages per normal operation conditions. See Test Loads for loading conditions.

Table 8. PCIe Refclk Jitter

Parameter	Symbol	Conditions	Typical	Maximum	Specification Limit	Unit	Notes
Additive PCIe Refclk Jitter (Common Clocked Architecture) VDD = 1.8V	$t_{jphPCIeG1-CC}$	PCIe Gen 1 (2.5 GT/s)	1478.9	2326.1	86,000	fs pk-pk	1, 2
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Hi Band (5.0 GT/s)	130.1	205.8	3,100	fs RMS	1, 2
		PCIe Gen 2 Lo Band (5.0 GT/s)	38.0	59.1	3,000		1, 2
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (8.0 GT/s)	43.4	68.5	1,000		1, 2
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (16.0 GT/s)	50.0	78.7	500		1, 2, 3, 4
	$t_{jphPCIeG5-CC}$	PCIe Gen 5 (32.0 GT/s)	17.1	26.9	150		1, 2, 3, 5
	$t_{jphPCIeG6-CC}$	PCIe Gen 6 (64.0 GT/s)	10.0	15.7	100		1, 2, 3, 6
	$t_{jphPCIeG7-CC}$	PCIe Gen 7 (128.0 GT/s)	7.0	11.0	67		1, 2, 3, 7
Additive PCIe Refclk Jitter (Common Clocked Architecture) VDD = 2.5V or 3.3V	$t_{jphPCIeG1-CC}$	PCIe Gen 1 (2.5 GT/s)	1084.9	1662.0	86,000	fs pk-pk	1, 2
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Hi Band (5.0 GT/s)	94.8	146.6	3,100	fs RMS	1, 2
		PCIe Gen 2 Lo Band (5.0 GT/s)	29.4	43.1	3,000		1, 2
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (8.0 GT/s)	31.8	48.8	1,000		1, 2
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (16.0 GT/s)	36.7	97.0	500		1, 2, 3, 4
	$t_{jphPCIeG5-CC}$	PCIe Gen 5 (32.0 GT/s)	12.5	19.2	150		1, 2, 3, 5
	$t_{jphPCIeG6-CC}$	PCIe Gen 6 (64.0 GT/s)	7.3	11.2	100		1, 2, 3, 6
	$t_{jphPCIeG7-CC}$	PCIe Gen 7(128.0 GT/s)	5.1	7.8	67		1, 2, 3, 7
Additive PCIe Refclk Jitter (IR Architecture) VDD = 1.8V	$t_{jphPCIeG2-IR}$	PCIe Gen 2 (5.0 GT/s)	102.8	159.7	N/A	fs RMS	1, 2, 8
	$t_{jphPCIeG3-IR}$	PCIe Gen 3 (8.0 GT/s)	40.8	63.5	N/A		1, 2, 8
	$t_{jphPCIeG4-IR}$	PCIe Gen 4 (16.0 GT/s)	42.0	65.3	N/A		1, 2, 8
	$t_{jphPCIeG5-IR}$	PCIe Gen 5 (32.0 GT/s)	11.8	18.5	N/A		1, 2, 8
	$t_{jphPCIeG6-IR}$	PCIe Gen 6 (64.0 GT/s)	8.4	13.0	N/A		1, 2, 8
	$t_{jphPCIeG7-IR}$	PCIe Gen 7 (128.0 GT/s)	5.9	9.2	N/A		1, 2, 8
Additive PCIe Refclk Jitter (IR Architecture) VDD = 2.5V or 3.3V	$t_{jphPCIeG2-IR}$	PCIe Gen 2 (5.0 GT/s)	77.1	81.6	N/A	fs RMS	1, 2, 8
	$t_{jphPCIeG3-IR}$	PCIe Gen 3 (8.0 GT/s)	30.4	44.9	N/A		1, 2, 8
	$t_{jphPCIeG4-IR}$	PCIe Gen 4 (16.0 GT/s)	31.3	91.2	N/A		1, 2, 8
	$t_{jphPCIeG5-IR}$	PCIe Gen 5 (32.0 GT/s)	8.7	13.1	N/A		1, 2, 8
	$t_{jphPCIeG6-IR}$	PCIe Gen 6 (64.0 GT/s)	6.2	9.2	N/A		1, 2, 8
	$t_{jphPCIeG7-IR}$	PCIe Gen 7 (128.0 GT/s)	4.4	6.5	N/A		1, 2, 8

[1] The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 7.0, Revision 0.7. See the Test Loads section of the datasheet for the exact measurement setup. The total Ref Clk jitter limits for each data rate are listed for convenience. The additive jitter may be subtracted from the limit using RSS subtraction to determine remaining margin.

[2] Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

[3] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

[4] Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

[5] Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

[6] Note that 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.

[7] Note that 0.10ps RMS is to be used in channel simulations to account for additional noise in a real system.

[8] The PCI Express Base Specification 7.0, Revision 0.7 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Specification Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.

Table 9. Random Phase Jitter

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Additive Phase Jitter	$t_{jph100M}$	100MHz, 12kHz to 20MHz, VDD = 1.8V	-	97	158	fs (rms)	1,2,3
		100MHz, 12kHz to 20MHz, VDD = 2.5V or 3.3V	-	78	111	fs (rms)	1,2,3
	$t_{jph156M}$	156.25MHz, 12kHz to 20MHz, VDD = 1.8V	-	66	91	fs (rms)	1,2,3
		156.25MHz, 12kHz to 20MHz, VDD = 2.5V or 3.3V	-	58	71	fs (rms)	1,2,3

[1] Confirmed by design and characterization, not 100% tested in production.

[2] Driven by Rhode & Schwartz SMA100.

[3] For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 - (input jitter)^2].

Table 10. Channel to Channel Isolation

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Channel to Channel Isolation	t_{ISO}	1.8V operation.	-58	-	-	dBc	1, 2
		2.5V or 3.3Voperation.	-66	-	-	dBc	1, 2

[1] Confirmed by design and characterization, not 100% tested in production.

[2] Measured with 3 channels at 100MHz non-spreading and one channel at 100MHz, -0.5% spread. Value represents worst case combination of inputs and outputs.

Table 11. Input/Supply/Common Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Supply Voltage	V_{DDx}	Supply voltage for core and outputs, 3.3V operation.	3.135	3.3	3.465	V	
		Supply voltage for core and outputs, 2.5V operation.	2.375	2.5	2.625	V	
		Supply voltage for core and outputs, 1.8V operation.	1.71	1.8	1.89	V	
Ambient Operating Temperature	T_{AMB}	Industrial range.	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus.	0.75 V_{DD}	-	V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus.	-0.3	-	0.25 V_{DD}	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DD}.	-5	-	5	µA	
	I_{INP}	Single-ended inputs. V_{IN} = 0 V; inputs with internal pull-up resistors. V_{IN} = V_{DD}; inputs with internal pull-down resistors.	-150	-	150	µA	
Input Frequency	F_{IN}		1 PPS	-	350	MHz	4
PPM Error	f_{ERROR}	Input to output ppm error.		0		ppm	5
DC Output Impedance	ZO-DC	85Ω setting (single-ended value).	34	42.5	51	Ω	1
		100Ω setting (single-ended value).	40	50	60	Ω	1
Pin Inductance	L_{pin}		-	-	7	nH	1
Capacitance	C_{IN}	Logic inputs, including CLK.	2.2	2.8	3.2	pF	1
	C_{OUT}	Output pin capacitance.	-	-	6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} reaching 90% of target, input clock present.	-	-	3	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable frequency for PCIe applications (Triangular modulation)	30	31.5	33	kHz	
OE Latency	t_{LATOE}	Q start after OE assertion. Q stop after OE deassertion.	2	-	10	clocks	1,3
Tfall	t_F	Fall time of single-ended control inputs.	-	-	5	ns	2
Trise	t_R	Rise time of single-ended control inputs.	-	-	5	ns	2

[1] Confirmed by design and characterization, not 100% tested in production

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] “PPS” means Pulse Per Second or Hertz.

[5] This device does not alter the ppm accuracy of the input clock.

Table 12. Source-Terminated LP-HCSL Driver with High-Impedance Receiver

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions. See Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Unit	Notes
Rising/Falling Slew Rate	dV/dt	100MHz, IOA_tri, IOB_tri = M VDD = 1.8V	1.4	2.3	3.2	1 to 4	V/ns	2, 3,10
Rising Edge (REFCLK+) to Falling Edge (REFCLK-) Matching	$\Delta t_R/t_F$		-	3.2	12	20	%	1,10,12
Absolute Max Output Voltage	V_{MAX}		-	-	900	1150	mV	1, 7, 10
Absolute Min Output Voltage	V_{MIN}		-142	-	-	-300	mV	1, 8, 10
Output High Voltage	V_{OH}		564	708	881	N/A	mV	1,7
Output Low Voltage	V_{OL}		-104	-6	99	N/A	mV	1,8
Absolute Crossing Point Voltage	V_{CROSS}		255	355	446	250 to 550	mV	1, 4, 5,10
V_{CROSS} Variation over all Rising Clock Edges	ΔV_{CROSS}		-	28	124	140	mV	1, 4, 9, 10
Rising/Falling Slew Rate	dV/dt	100MHz, IOA_tri, IOB_tri = 0 VDD = 1.8V	1.7	2.5	3.5	1 to 4	V/ns	2, 3,10
Rising Edge (REFCLK+) to Falling Edge (REFCLK-) Matching	$\Delta t_R/t_F$		-	3.1	12	20	%	1,10,12
Absolute Max Output Voltage	V_{MAX}		-	-	990	1150	mV	1, 7,10
Absolute Min Output Voltage	V_{MIN}		-157	-	-	-300	mV	1, 8,10
Output High Voltage	V_{OH}		614	766	969	N/A	mV	1, 7
Output Low Voltage	V_{OL}		-121	-10	96	N/A	mV	1, 8
Absolute Crossing Point Voltage	V_{CROSS}		285	380	490	250 to 550	mV	1, 4, 5,10
V_{CROSS} Variation over all Rising Clock Edges	ΔV_{CROSS}		-	29	107	140	mV	1, 4, 9, 10
Rising/Falling Slew Rate	dV/dt	100MHz, IOA_tri, IOB_tri = 1 VDD = 1.8V	1.6	2.6	3.9	1 to 4	V/ns	2, 3, 10
Rising Edge (REFCLK+) to Falling Edge (REFCLK-) Matching	$\Delta t_R/t_F$		-	3.3	12	20	%	1,10,12
Absolute Max Output Voltage	V_{MAX}		-	-	1093	1150	mV	1, 7,10
Absolute Min Output Voltage	V_{MIN}		-175	-	-	-300	mV	1, 8,10
Output High Voltage	V_{OH}		650	825	1069	N/A	mV	1, 7
Output Low Voltage	V_{OL}		-130	-14	101	N/A	mV	1, 8
Absolute Crossing Point Voltage	V_{CROSS}		303	403	512	250 to 550	mV	1, 4, 5, 10
V_{CROSS} Variation over all Rising Clock Edges	ΔV_{CROSS}		-	31	119	140	mV	1, 4, 9, 10

Table 12. Source-Terminated LP-HCSL Driver with High-Impedance Receiver (Cont.)

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions. See Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Unit	Notes
Rising/Falling Slew Rate	dV/dt	100MHz, IOA_tri, IOB_tri = M VDD = 2.5V or 3.3V	2.0	2.5	3.3	1 to 4	V/ns	2, 3,10
Rising Edge (REFCLK+) to Falling Edge (REFCLK-) Matching	$\Delta t_R/t_F$		-	3.3	10	20	%	1,10,12
Absolute Max Output Voltage	V_{MAX}		-	-	932	1150	mV	1, 7,10
Absolute Min Output Voltage	V_{MIN}		-162	-	-	-300	mV	1, 8,10
Output High Voltage	V_{OH}		616	749	906	N/A	mV	1, 7
Output Low Voltage	V_{OL}		-119	-22	79	N/A	mV	1, 8
Absolute Crossing Point Voltage	V_{CROSS}		279	372	463	250 to 550	mV	1, 4, 5,10
V_{CROSS} Variation over all Rising Clock Edges	ΔV_{CROSS}		-	32	125	140	mV	1, 4, 9, 10
Rising/Falling Slew Rate	dV/dt	100MHz, IOA_tri, IOB_tri = 0 VDD = 2.5V or 3.3V	2.1	2.8	3.6	1 to 4	V/ns	2, 3, 10
Rising Edge (REFCLK+) to Falling Edge (REFCLK-) Matching	$\Delta t_R/t_F$		-	3.4	10	20	%	1,10,12
Absolute Max Output Voltage	V_{MAX}		-	-	1007	1150	mV	1, 7, 10
Absolute Min Output Voltage	V_{MIN}		-175	-	-	-300	mV	1, 8, 10
Output High Voltage	V_{OH}		700	827	979	N/A	mV	1, 7
Output Low Voltage	V_{OL}		-136	-27	93	N/A	mV	1, 8
Absolute Crossing Point Voltage	V_{CROSS}		311	405	464	250 to 550	mV	1, 4, 5, 10
V_{CROSS} Variation over all Rising Clock Edges	ΔV_{CROSS}		-	36	128	140	mV	1, 4, 9, 10
Rising/Falling Slew Rate	dV/dt	100MHz, IOA_tri, IOB_tri = 1 VDD = 2.5V or 3.3V	2.3	3.0	3.9	1 to 4	V/ns	2, 3, 10
Rising Edge (REFCLK+) to Falling Edge (REFCLK-) Matching	$\Delta t_R/t_F$		-	3.5	10	20	%	1, 10, 12
Absolute Max Output Voltage	V_{MAX}		-	-	1097	1150	mV	1, 7, 10
Absolute Min Output Voltage	V_{MIN}		-191	-	-	-300	mV	1, 8, 10
Output High Voltage	V_{OH}		807	917	1075	N/A	mV	1, 7
Output Low Voltage	V_{OL}		-149	-30	98	N/A	mV	1, 8
Absolute Crossing Point Voltage	V_{CROSS}		347	439	503	250 to 550	mV	1, 4, 5, 10
V_{CROSS} Variation over all Rising Clock Edges	ΔV_{CROSS}		-	39	137	140	mV	1, 4, 9, 10

[1] Measurement taken from single-ended waveform.

[2] Measurement taken from differential waveform.

[3] Measured from -75mV to +75mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 150 mV measurement window is centered on the differential zero crossing. See Figure 6 "Rise/Fall Measurement Points (Differential Waveform)".

[4] Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 2 “Absolute Cross Point and Swing Measurement Points (Single-ended Waveform)”.

[5] Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 2 “Absolute Cross Point and Swing Measurement Points (Single-ended Waveform)”.

[6] Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation. See Figure 5 “Duty Cycle and Clock Period Measurement Points (Differential Waveform)”.

[7] Defined as the maximum instantaneous voltage including overshoot. See Figure 2 “Absolute Cross Point and Swing Measurement Points (Single-ended Waveform)”.

[8] Defined as the minimum instantaneous voltage including undershoot. See Figure 2 “Absolute Cross Point and Swing Measurement Points (Single-ended Waveform)”.

[9] Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 3 “VCROSSDELTA Measurement Points (Single-ended Waveform)”.

[10] System board compliance measurements must use the test load card. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL = 2pF.

[11] PPM refers to parts per million and is a DC absolute period accuracy specification. 1PPM is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For example for 300PPM, then we have an error budget of 100Hz/PPM × 300PPM = 30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater.

[12] Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 4 “Rise/Fall Matching Measurement Points (Single-ended Waveform)”.

Figure 2. Absolute Cross Point and Swing Measurement Points (Single-ended Waveform)

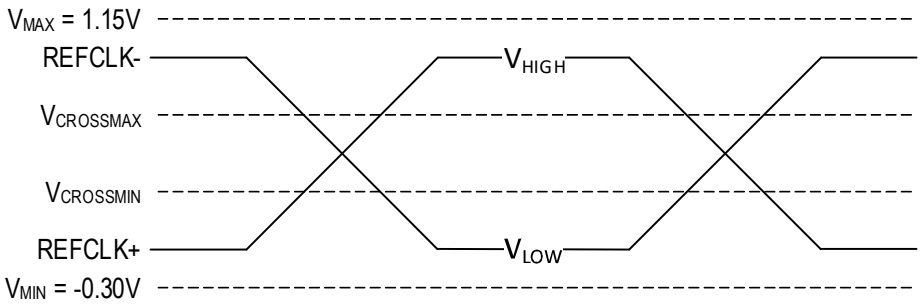


Figure 3. VCROSSDELTA Measurement Points (Single-ended Waveform)

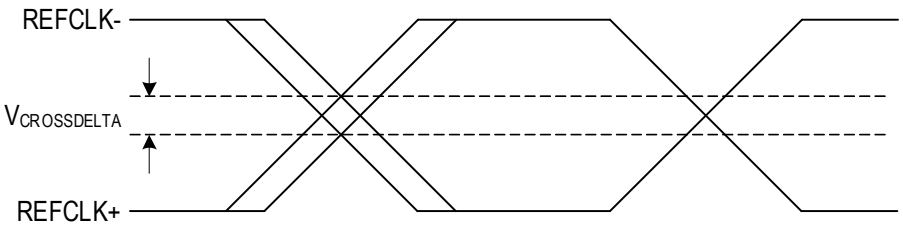


Figure 4. Rise/Fall Matching Measurement Points (Single-ended Waveform)

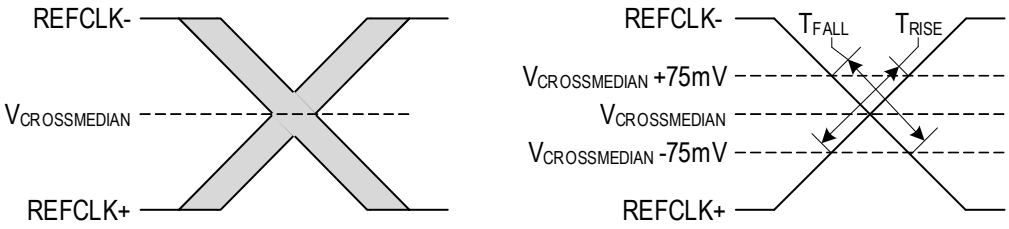


Figure 5. Duty Cycle and Clock Period Measurement Points (Differential Waveform)

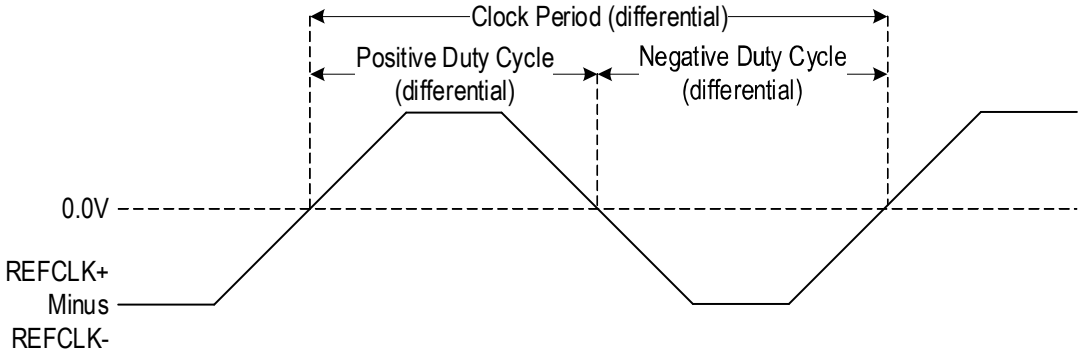


Figure 6. Rise/Fall Measurement Points (Differential Waveform)

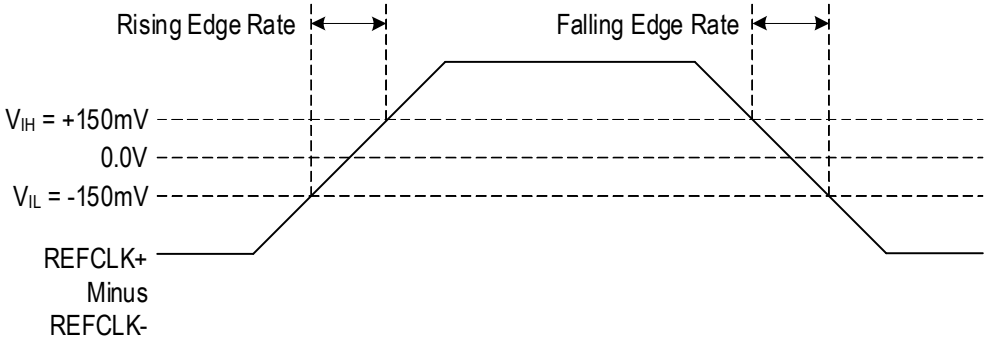


Table 13. Source-Terminated LP-HCSL Driver with Receiver Terminated Load (Double-Terminated)

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions. See Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Unit	Notes
Rising/Falling Slew Rate	dV/dt	100MHz, IOA_tri, IOB_tri = M VDD = 1.8V	1.7	2.6	3.6	1 to 4	V/ns	2, 3,10
Rising Edge (REFCLK+) to Falling Edge (REFCLK-) Matching	$\Delta t_R/t_F$		-	3	14	20	%	1, 11, 12
Absolute Max Output Voltage	V_{MAX}		-	-	453	575	mV	1, 7,10
Absolute Min Output Voltage	V_{MIN}		-27	-	-	-150	mV	1, 8,10
Output High Voltage	V_{OH}		289	367	441	N/A	mV	1, 7
Output Low Voltage	V_{OL}		-17	10	38	N/A	mV	1, 8
Absolute Crossing Point Voltage	V_{CROSS}		138	188	246	125 to 275	mV	1, 4, 5, 10
V_{CROSS} Variation over all Rising Clock Edges	ΔV_{CROSS}		-	11	48	70	mV	1, 4, 9, 10
Rising/Falling Slew Rate	dV/dt	100MHz, IOA_tri, IOB_tri = 0 VDD = 1.8V	1.8	2.8	4.1	1.5 to 4.5	V/ns	2, 3,10
Rising Edge (REFCLK+) to Falling Edge (REFCLK-) Matching	$\Delta t_R/t_F$		-	3	13	20	%	1, 11, 12
Absolute Max Output Voltage	V_{MAX}		-	-	492	575	mV	1, 7, 10
Absolute Min Output Voltage	V_{MIN}		-27	-	-	-150	mV	1, 8, 10
Output High Voltage	V_{OH}		309	396	478	N/A	mV	1, 7
Output Low Voltage	V_{OL}		-13	10	36	N/A	mV	1, 8
Absolute Crossing Point Voltage	V_{CROSS}		146	201	264	125 to 275	mV	1, 4, 5, 10
V_{CROSS} Variation over all Rising Clock Edges	ΔV_{CROSS}		-	11	51	70	mV	1, 4, 9, 10
Rising/Falling Slew Rate	dV/dt	100MHz, IOA_tri, IOB_tri = 1 VDD = 1.8V	1.9	3.0	4.3	1.5 to 4.5	V/ns	2, 3, 10
Rising Edge (REFCLK+) to Falling Edge (REFCLK-) Matching	$\Delta t_R/t_F$		-	3	15	20	%	1, 11, 12
Absolute Max Output Voltage	V_{MAX}		-	-	535	575	mV	1, 7, 10
Absolute Min Output Voltage	V_{MIN}		-30	-	-	-150	mV	1, 8, 10
Output High Voltage	V_{OH}		317	423	517	N/A	mV	1, 7
Output Low Voltage	V_{OL}		-14	11	37	N/A	mV	1, 8
Absolute Crossing Point Voltage	V_{CROSS}		150	215	286	140 to 290	mV	1, 4, 5, 10
V_{CROSS} Variation over all Rising Clock Edges	ΔV_{CROSS}		-	12	54	70	mV	1, 4, 9, 10

Table 13. Source-Terminated LP-HCSL Driver with Receiver Terminated Load (Double-Terminated) (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Unit	Notes
Rising/Falling Slew Rate	dV/dt	100MHz, IOA_tri, IOB_tri = M VDD = 2.5V or 3.3V	1.9	2.7	3.8	1 to 4	V/ns	2, 3, 10
Rising Edge (REFCLK+) to Falling Edge (REFCLK-) Matching	$\Delta t_R/t_F$		-	3	13	20	%	1, 11, 12
Absolute Max Output Voltage	V_{MAX}		-	-	463	575	mV	1, 7, 10
Absolute Min Output Voltage	V_{MIN}		-27	-	-	-150	mV	1, 8, 10
Output High Voltage	V_{OH}		336	391	451	N/A	mV	1, 7
Output Low Voltage	V_{OL}		-14	9	35	N/A	mV	1,8
Absolute Crossing Point Voltage	V_{CROSS}		163	203	254	125 to 275	mV	1, 4, 5, 10
V_{CROSS} Variation over all Rising Clock Edges	ΔV_{CROSS}		-	11	48	70	mV	1, 4, 9, 10
Rising/Falling Slew Rate	dV/dt	100MHz, IOA_tri, IOB_tri = 0 VDD = 2.5V or 3.3V	2.2	3.0	4.0	1 to 4	V/ns	2, 3, 10
Rising Edge (REFCLK+) to Falling Edge (REFCLK-) Matching	$\Delta t_R/t_F$		-	3	13	20	%	1, 11, 12
Absolute Max Output Voltage	V_{MAX}		-	-	493	575	mV	1, 7, 10
Absolute Min Output Voltage	V_{MIN}		-26	-	-	-150	mV	1, 8, 10
Output High Voltage	V_{OH}		379	429	482	N/A	mV	1, 7
Output Low Voltage	V_{OL}		-13	10	34	N/A	mV	1, 8
Absolute Crossing Point Voltage	V_{CROSS}		182	221	271	125 to 275	mV	1, 4, 5, 10
V_{CROSS} Variation over all Rising Clock Edges	ΔV_{CROSS}		-	12	50	70	mV	1, 4, 9, 10
Rising/Falling Slew Rate	dV/dt	100MHz, IOA_tri, IOB_tri = 1 VDD = 2.5V or 3.3V	1.9	3.0	4.5	1.5 to 4.5	V/ns	2, 3, 10
Rising Edge (REFCLK+) to Falling Edge (REFCLK-) Matching	t_R/t_F		-	3	13	20	%	1, 11, 12
Absolute Max Output Voltage	V_{MAX}		-	-	529	575	mV	1, 7, 10
Absolute Min Output Voltage	V_{MIN}		-30	-	-	-150	mV	1, 8, 10
Output High Voltage	$V_{OH\ 1}$		427	469	511	N/A	mV	1, 7
Output Low Voltage	$V_{OL\ 1}$		-11	11	36	N/A	mV	1, 8
Absolute Crossing Point Voltage	V_{CROSS}		200	242	293	150 to 300	mV	1, 4, 5, 10
V_{CROSS} Variation over all Rising Clock Edges	ΔV_{CROSS}		-	14	57	70	mV	1, 4, 9, 10

[1] Measurement taken from single-ended waveform.

[2] Measurement taken from differential waveform.

[3] Measured from -75mV to +75mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 150mV measurement window is centered on the differential zero crossing. See Figure 11 "Rise/Fall Measurement Points (Differential Waveform)".

[4] Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 7 "Absolute Cross Point and Swing Measurement Points (Single-Ended Waveform)".

[5] Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 7 “Absolute Cross Point and Swing Measurement Points (Single-Ended Waveform)”.

[6] Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation. See Figure 10 “Duty Cycle and Clock Period Measurement Points (Differential Waveform)”.

[7] Defined as the maximum instantaneous voltage including overshoot. See Figure 7 “Absolute Cross Point and Swing Measurement Points (Single-Ended Waveform)”.

[8] Defined as the minimum instantaneous voltage including undershoot. See Figure 7 “Absolute Cross Point and Swing Measurement Points (Single-Ended Waveform)”.

[9] Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 8 “VCROSSDELTA Measurement Points (Single-Ended Waveform)”.

[10] System board compliance measurements must use the test load card. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL = 2pF.

[11] PPM refers to parts per million and is a DC absolute period accuracy specification. 1PPM is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For example for 300PPM, then we have an error budget of 100Hz/PPM × 300PPM = 30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater.

[12] Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 9 “Rise/Fall Matching Measurement Points (Single-Ended Waveform)”.

Figure 7. Absolute Cross Point and Swing Measurement Points (Single-ended Waveform)

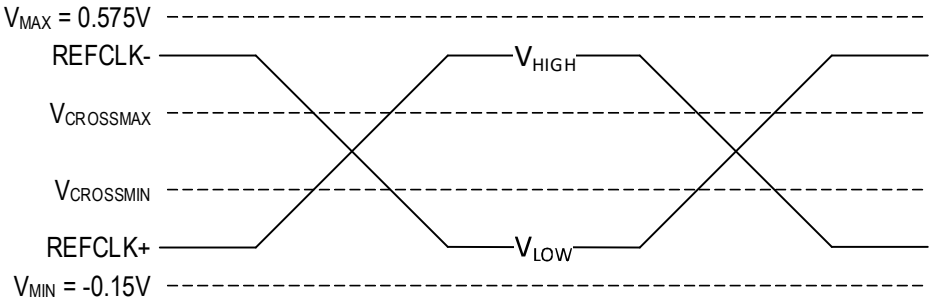


Figure 8. VCROSSDELTA Measurement Points (Single-ended Waveform)

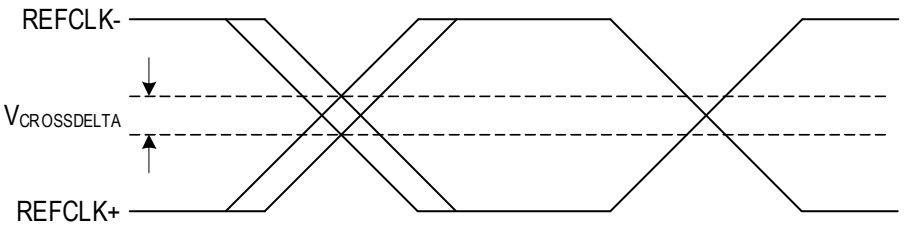


Figure 9. Rise/Fall Matching Measurement Points (Single-ended Waveform)

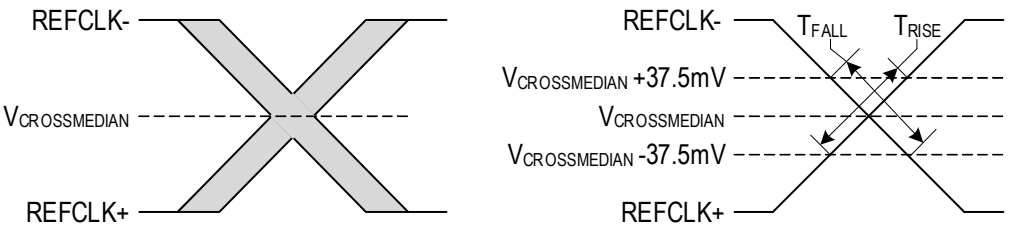


Figure 10. Duty Cycle and Clock Period Measurement Points (Differential Waveform)

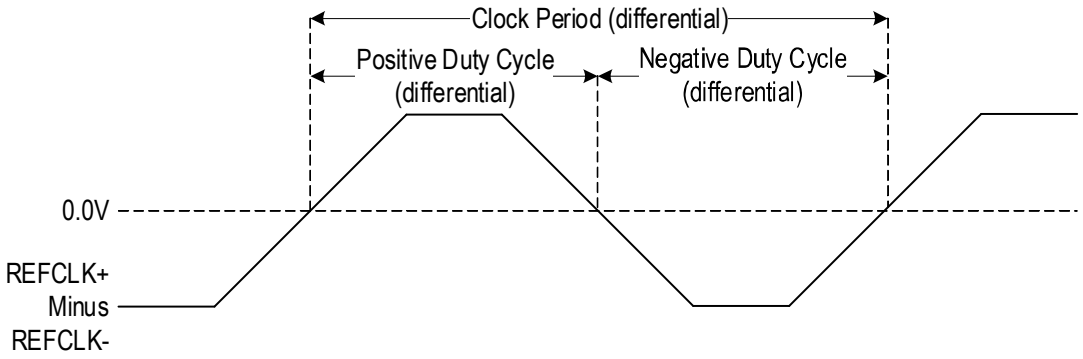


Figure 11. Rise/Fall Measurement Points (Differential Waveform)

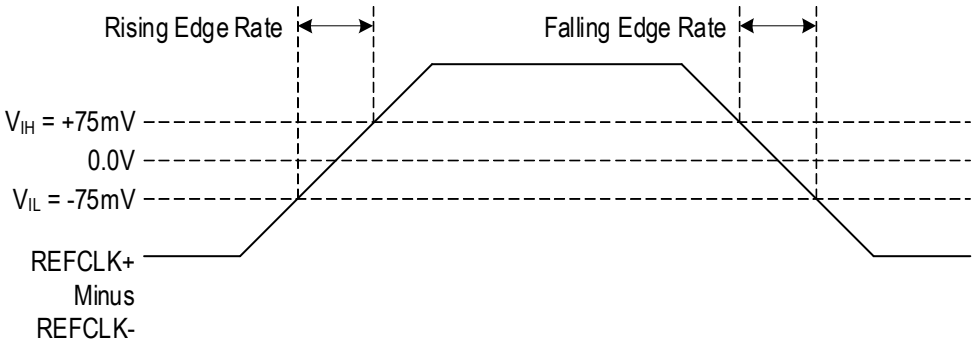


Table 14. Differential Clock Input Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Input High Current–CLKINx, CLKINx#	I_{IH}	V_{DDCLKx} = 3.465V, 2.625V or 1.89V = V_{IN}.	-	-	150	µA	1
Input Low Current–CLKINx	I_{IL}	V_{DD} = 3.465V, 2.625V or 1.89V, V_{IN} = 0V.	-5	-	-	µA	1
Input Low Current–CLKINx#		V_{DD} = 3.465V, 2.625V or 1.89V, V_{IN} = 0V.	-150	-	-	µA	1
Peak-to-peak Voltage	V_{P2P}	Single-ended input swing.	0.15	-	1.3	V	2
Common Mode Input Voltage	V_{CMR}		0.075	-	V_{DDCLKx} – 1.2	V	2,3

[1] CLKINx denotes input clocks where x = 0 to 3.

[2] V_{IL} should not be less than –0.3V. V_{IH} should not be higher than V_{DDCLKx}.

[3] Common mode voltage is defined as the cross-point.

Table 15. Output Duty Cycle, Jitter, and Skew Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Duty Cycle Distortion	t_{DCD}	Measured differentially at 100MHz.	-0.9	-0.4	0.2	%	1,3
Skew, Input to Output	t_{PD}	V_T = 50%.	0.73	1.2	1.6	ns	1
Skew, Output to Output	t_{SK3}	V_T = 50%.	-	4.9	22	ps	1

[1] Confirmed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock.

Table 16. Current Consumption

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Operating Supply Current, VDD = 1.8V	I_{DDCORE}	V_{DDCORE}, All outputs active at 100MHz.	-	13	16	mA	
	I_{DDOx}	Total V_{DDO}, All outputs active at 100MHz.	-	46	60	mA	
	I_{DDCLKx}	Total V_{DDCLK}, All CLK inputs active at 100MHz.	-	10	12	mA	
Operating Supply Current, VDD = 2.5V or 3.3V	I_{DDCORE}	V_{DDCORE}, All outputs active at 100MHz.	-	16	21	mA	
	I_{DDOx}	Total V_{DDO}, All outputs active at 100MHz.	-	66	82	mA	
	I_{DDCLKx}	Total V_{DDCLK}, All CLK inputs active at 100MHz.	-	12	16	mA	
Standby Current, VDD = 1.8V	I_{DDCORE}	V_{DDCORE}, all outputs disabled.	-	13	16	mA	1
	I_{DDOx}	Total V_{DDO}, all outputs disabled.	-	24	34	mA	1
	I_{DDCLKx}	Total V_{DDCLKx}, all outputs disabled.	-	6	8	mA	1
Standby Current, VDD = 2.5V or 3.3V	I_{DDCORE}	V_{DDCORE}, all outputs disabled.	-	16	21	mA	1
	I_{DDOx}	Total V_{DDO}, all outputs disabled.	-	35	42	mA	1
	I_{DDCLKx}	Total V_{DDCLKx}, all outputs disabled.	-	7	9	mA	1

[1] CLKINx/CLKINx# set low/low.

Test Loads

Figure 12. Source-Terminated Driver with High-Impedance Receiver

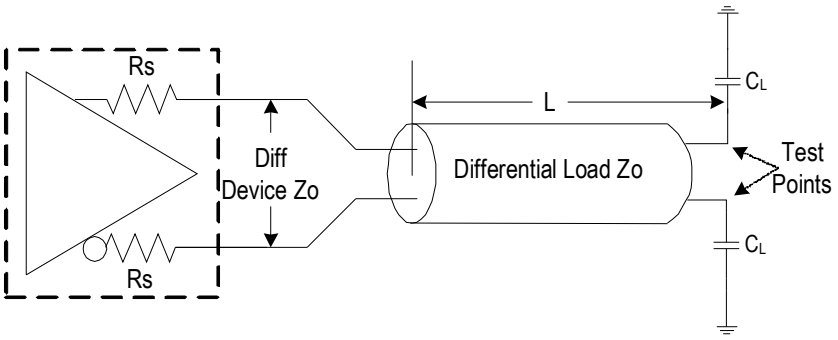


Table 17. Parameters for Source-Terminated Driver with High-Impedance Receiver[a]

ZOUTSEL	Differential Device Zo (Ω)	Rs (Ω)	Differential Load Zo (Ω)	L (Inches)	C_L (pF)
0	85	Internal	85	10	2
0	85	External 7.5	100	10	2
1	100	Internal	100	10	2

[a] This load is only used for signal integrity measurements at 100MHz into a 10 inch load (PCIe). Higher frequencies use the Double-Terminated test load for signal integrity measurements.

Figure 13. Source-Terminated Driver with Receiver Termination (Double-Terminated)

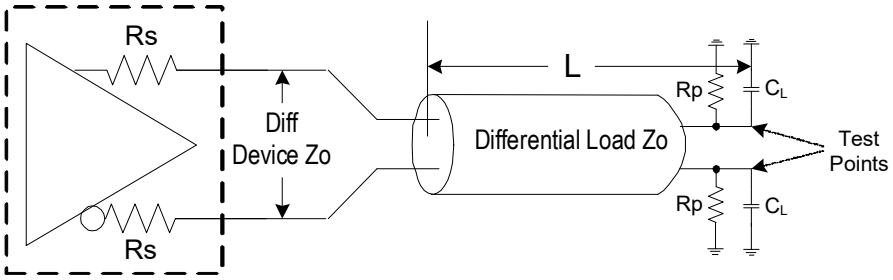


Table 18. Parameters for Source-Terminated Driver with Receiver Termination (Double Terminated)[a]

ZOUTSEL	Differential Device Zo (Ω)	Rs (Ω)	Differential Load Zo (Ω)	L (Inches)	C_L (pF)	R_P (pF)
0	85	Internal	85	10	2	42.5
0	85	External 7.5	100	10	2	50
1	100	Internal	100	10	2	50

[a] This load is used for signal integrity measurements at frequencies higher than 100MHz. It may also be used at 100MHz.

Alternate Terminations

The LP-HCSL output can easily drive other logic families. See "AN-891 Driving LVPECL, LVDS, and CML Logic with "Universal" Low-Power HCSL Outputs" for termination schemes for LVPECL, LVDS, CML and SSTL.

Phase Jitter Test Loads

Figure 14. Test Setup for Additive Phase Jitter Measurements

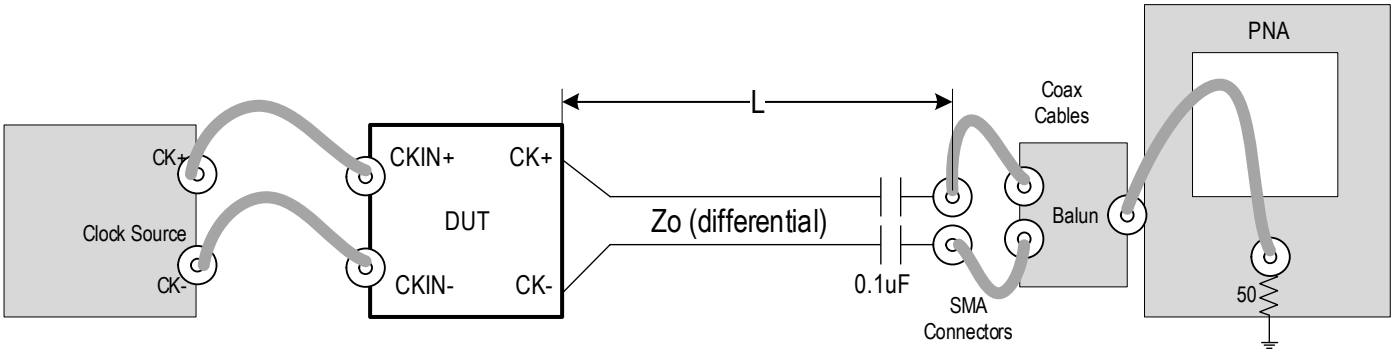


Table 19. Parameters for Phase Jitter Measurements

Clock Source	ZOUTSEL	Differential Device Zo (Ω)	Rs (Ω)	Differential Load Zo (Ω)	L (Inches)
SMA100B	0	85	Internal	85	10
SMA100B	1	100	Internal	100	10

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

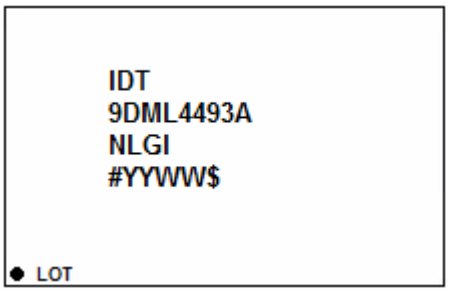
Thermal Characteristics

Table 20. Thermal Characteristics[1]

Parameter	Symbol	Parameter	Package	Value	Unit
Thermal Resistance	θ_{JB}	Junction to base.	NLG32	1.9	°C/W
	θ_{JC}	Junction to case.		34.6	°C/W
	θ_{JA0}	Junction to Air, still air.		43.5	°C/W
	θ_{JA1}	Junction to Air, 1 m/s air flow.		36.7	°C/W
	θ_{JA3}	Junction to Air, 3 m/s air flow.		32.9	°C/W
	θ_{JA5}	Junction to Air, 5 m/s air flow.		31.4	°C/W

[1] EPAD soldered to ground.

Marking Diagram



- Lines 2 and 3 indicate the part number.
- Line 4 indicates the following:
  - "#" denotes the stepping.
  - "YY" is the last two digits of the year; "WW" is the work week number when the part was assembled.
  - "$" denotes the mark code.

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature Range
9DML4493ANLGI	5 × 5 mm 32-VFQFPN	Tray	-40° to +85°C
9DML4493ANLGI8	5 × 5 mm 32-VFQFPN	Tape and Reel	-40° to +85°C

"G" suffix denotes Pb-free configuration, RoHS compliant.

Revision History

Revision Date	Description of Change
May 20, 2025	▪ Updated title on page 1 to Gen1–7 from Gen1–6. ▪ Updated additive phase jitter specification to Gen7 in Key Specifications. ▪ Updated Table 8.
February 24, 2022	▪ Added PCIe Gen6 specifications to the device and changed units from picoseconds to femtoseconds. See PCIe Refclk Jitter. ▪ Changed “SRIS” nomenclature to “IR”.
February 19, 2021	▪ Updated 1st page description. ▪ Updated 1st page Features list. ▪ Added Clock Input Bias Network diagram.
June 17, 2020	▪ Updated footnote 2 on table 10. ▪ Updated Output High Voltage values for 100MHz, IOA_tri, IOB_tri = 0, VDD = 1.8V. ▪ Updated Absolute Max Output Voltage values for 100MHz, IOA_tri, IOB_tri = 1, VDD = 1.8V. ▪ Updated values in tables 8, 12, 13, and 16. ▪ Changed ZOUTSEL from an internal pull-down to an internal pull-up resistor in Block Diagram, Pin Assignments, and Pin Descriptions. ▪ Corrected pull-up typo in pin descriptions for pin 1, 24, 28, and 29; changed to pull-down. ▪ Updated maximum values for standby and supply current specifications.
June 1, 2020	Re-arranged and updated electrical tables and moved to final.
May 19, 2020	Updated typical values in electrical tables.
May 15, 2020	Updated electrical tables, added typical values and moved to preliminary.
April 6, 2020	Initial release.