

Description

The 9DBU0431 is a member of Renesas' 1.5V Ultra-Low-Power (ULP) PCIe family. The device has 4 output enables for clock management, and 3 selectable SMBus addresses.

Recommended Application

1.5V PCIe Gen1-2-3 Zero-Delay/Fan-out Buffer (ZDB/FOB)

Output Features

- 4 – 1-167MHz Low-Power (LP) HCSL DIF pairs

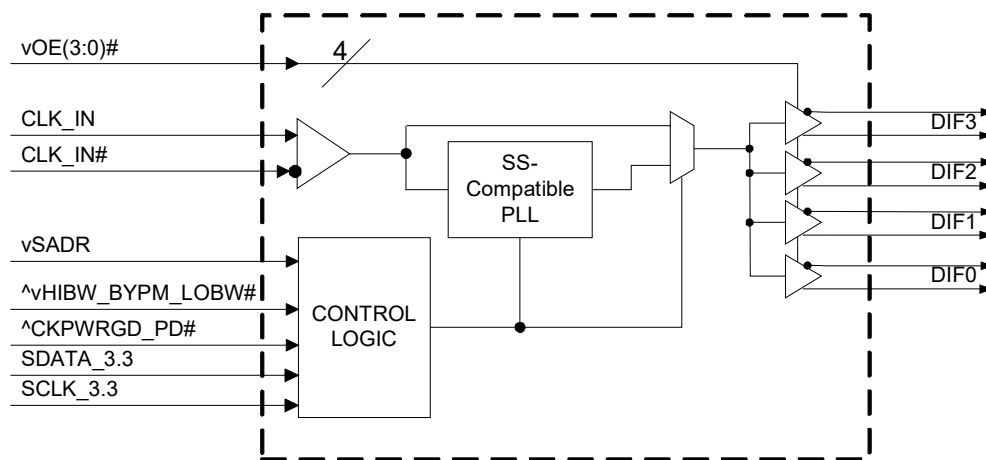
Key Specifications

- DIF cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 50ps
- DIF phase jitter is PCIe Gen1–3 compliant
- DIF bypass mode additive phase jitter is < 300fs RMS for PCIe Gen3
- DIF bypass mode additive phase jitter < 350fs RMS for 12kHz–20MHz

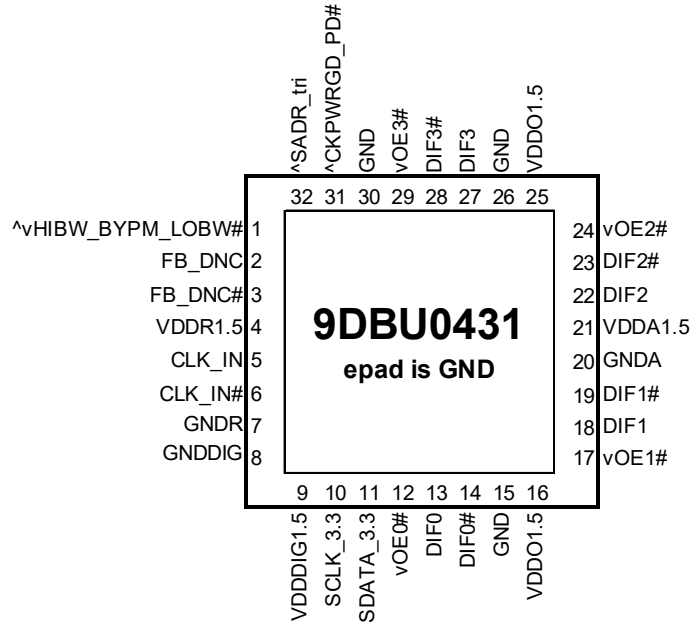
Features/Benefits

- LP-HCSL outputs; save 8 resistors compared to standard HCSL outputs
- 45mW typical power consumption in PLL mode; eliminates thermal concerns
- Spread Spectrum (SS) compatible; allows SS for EMI reduction
- OE# pins; support DIF power management
- HCSL-compatible differential input; can be driven by common clock sources
- SMBus-selectable features; optimize signal integrity to application
 - slew rate for each output
 - differential output amplitude
- Pin/software selectable PLL bandwidth and PLL Bypass; optimize PLL to application
- Outputs blocked until PLL is locked; clean system start-up
- Device contains default configuration; SMBus interface not required for device control
- 3.3V tolerant SMBus interface works with legacy controllers
- Three selectable SMBus addresses; multiple devices can easily share an SMBus segment
- Space saving 32-pin 5 x 5 mm VFQFPN; minimal board space

Block Diagram



Pin Configuration



32-pin VFQFPN, 5x5 mm, 0.5mm pitch

- ^ prefix indicates internal 120KOhm pull up resistor
- ^v prefix indicates internal 120KOhm pull up AND pull down resistor (biased to VDD/2)
- v prefix indicates internal 120KOhm pull down resistor

SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

Power Management Table

CKPWRGD_PD#	CLK_IN	SMBus OEx bit	OEx# Pin	DIFx		PLL
				True O/P	Comp. O/P	
0	X	X	X	Low	Low	Off
1	Running	0	X	Low	Low	On ¹
1	Running	1	0	Running	Running	On ¹
1	Running	1	1	Low	Low	On ¹

1. If Bypass mode is selected, the PLL will be off, and outputs will be running.

Power Connections

Pin Number		Description
VDD	GND	
4	7	Input receiver analog
9	8	Digital Power
16, 25	15,20,26,30	DIF outputs
21	20	PLL Analog

Note: epad on this device is not electrically connected to the die. It should be connected to ground for best thermal performance.

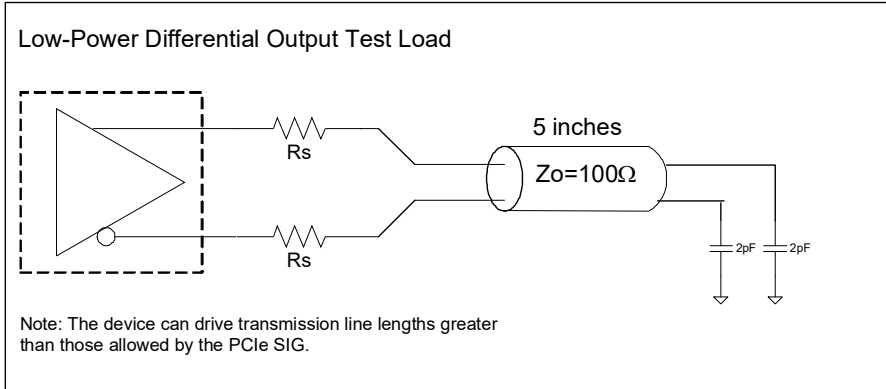
PLL Operating Mode

HiBW_BypM_LoBW#	MODE	Byte1 [7:6] Readback	Byte1 [4:3] Control
0	PLL Lo BW	00	00
M	Bypass	01	01
1	PLL Hi BW	11	11

Pin Descriptions

Pin#	Pin Name	Type	Pin Description
1	^vHIBW_BYPM_LOBW#	LATCHED IN	Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.
2	FB_DNC	DNC	True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
3	FB_DNC#	DNC	Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
4	VDDR1.5	PWR	1.5V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
5	CLK_IN	IN	True Input for differential reference clock.
6	CLK_IN#	IN	Complementary Input for differential reference clock.
7	GNDR	GND	Analog Ground pin for the differential input (receiver)
8	GNDDIG	GND	Ground pin for digital circuitry
9	VDDDIG1.5	PWR	1.5V digital power (dirty power)
10	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
11	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
12	vOE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
13	DIF0	OUT	Differential true clock output
14	DIF0#	OUT	Differential Complementary clock output
15	GND	GND	Ground pin.
16	VDDO1.5	PWR	Power supply for outputs, nominally 1.5V.
17	vOE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
18	DIF1	OUT	Differential true clock output
19	DIF1#	OUT	Differential Complementary clock output
20	GND	GND	Ground pin for the PLL core.
21	VDDA1.5	PWR	1.5V power for the PLL core.
22	DIF2	OUT	Differential true clock output
23	DIF2#	OUT	Differential Complementary clock output
24	vOE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
25	VDDO1.5	PWR	Power supply for outputs, nominally 1.5V.
26	GND	GND	Ground pin.
27	DIF3	OUT	Differential true clock output
28	DIF3#	OUT	Differential Complementary clock output
29	vOE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
30	GND	GND	Ground pin.
31	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
32	^SADR_tri	LATCHED IN	Tri-level latch to select SMBus Address. See SMBus Address Selection Table.
33	EPAD	GND	Connect ePAD to ground.

Test Loads



Alternate Differential Output Terminations

Rs	Zo	Units
33	100	Ohms
27	85	

Alternate Terminations

The output can easily drive other logic families. See [“AN-891 Driving LVPECL, LVDS, CML, and SSTL Logic with Universal Low-Power HCSL Outputs”](#) for LVPECL, LVDS, CML, and SSTL.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBU0431. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx		-0.5		2	V	1,2
Input Voltage	V _{IN}		-0.5		V _{DD} +0.5	V	1,3
Input High Voltage, SMBus	V _{IHSMB}	SMBus clock and data pins			3.3	V	1
Storage Temperature	T _s		-65		150	°C	1
Junction Temperature	T _j				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

³Not to exceed 2.0V.

Electrical Characteristics—Clock Input Parameters

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Common Mode Voltage - DIF_IN	V _{COM}	Common Mode Input Voltage	200		725	mV	1
Input Swing - DIF_IN	V _{SWING}	Differential value	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I _{IN}	V _{IN} = V _{DD} , V _{IN} = GND	-5		5	uA	
Input Duty Cycle	d _{tin}	Measurement from differential waveform	45	50	55	%	1
Input Jitter - Cycle to Cycle	J _{DIFIN}	Differential Measurement	0		150	ps	1

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx	Supply voltage for core and analog	1.425	1.5	1.575	V	
Ambient Operating Temperature	T _{AMB}	Commercial range	0	25	70	°C	1
		Industrial range	-40	25	85	°C	1
Input High Voltage	V _{IH}	Single-ended inputs, except SMBus	0.75 V _{DD}		V _{DD} + 0.3	V	
Input Mid Voltage	V _{IM}	Single-ended tri-level inputs ('_tri' suffix)	0.4 V _{DD}		0.6 V _{DD}	V	
Input Low Voltage	V _{IL}	Single-ended inputs, except SMBus	-0.3		0.25 V _{DD}	V	
Input Current	I _{IN}	Single-ended inputs, V _{IN} = GND, V _{IN} = VDD	-5		5	uA	
	I _{INP}	Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	
Input Frequency	F _{ibyp}	Bypass mode	1		167	MHz	2
	F _{ipll}	100MHz PLL mode	20	100.00	110	MHz	2
Pin Inductance	L _{pin}				7	nH	1
Capacitance	C _{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C _{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,5
	C _{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T _{STAB}	From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Input SS Modulation Frequency PCIe	f _{MODINPCIe}	Allowable Frequency for PCIe Applications (Triangular Modulation)	30		33	kHz	
Input SS Modulation Frequency non-PCIe	f _{MODIN}	Allowable Frequency for non-PCIe Applications (Triangular Modulation)	0		66	kHz	
OE# Latency	t _{LATOE#}	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	clocks	1,3
Tdrive_PD#	t _{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t _F	Fall time of single-ended control inputs			5	ns	2
Trise	t _R	Rise time of single-ended control inputs			5	ns	2
SMBus Input Low Voltage	V _{ILSMB}				0.6	V	
SMBus Input High Voltage	V _{IHSMB}	V _{DD} SMB = 3.3V, see note 4 for V _{DD} SMB < 3.3V	2.1		3.3	V	4
SMBus Output Low Voltage	V _{OLSMB}	@ I _{PULLUP}			0.4	V	
SMBus Sink Current	I _{PULLUP}	@ V _{OL}	4			mA	
Nominal Bus Voltage	V _{DD} SMB	Bus Voltage	1.425		3.3	V	
SCLK/SDATA Rise Time	t _{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t _{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f _{MAXSMB}	Maximum SMBus operating frequency			400	kHz	6

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

⁴ For V_{DD}SMB < 3.3V, V_{IHSMB} >= 0.8xV_{DD}SMB

⁵DIF_IN input

⁶The differential input clock must be running for the SMBus to be active

Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on, fast setting	1.4	2.2	3.5	V/ns	1,2,3
	dV/dt	Scope averaging on, slow setting	0.9	1.7	2.5	V/ns	1,2,3
Slew rate matching	Δ dV/dt	Slew rate matching, Scope averaging on		2.7	20	%	1,2,4
Voltage High	V _{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	630	735	850	mV	7
Voltage Low	V _{LOW}		-150	-16	150		7
Max Voltage	V _{max}	Measurement on single ended signal using absolute value. (Scope averaging off)		779	1150	mV	7
Min Voltage	V _{min}		-300	-45			7
Vswing	Vswing	Scope averaging off	300	1503		mV	1,2
Crossing Voltage (abs)	V _{cross_abs}	Scope averaging off	250	405	550	mV	1,5
Crossing Voltage (var)	Δ -V _{cross}	Scope averaging off		12	140	mV	1,6

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of V_{cross_min}/max (V_{cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting Δ -V_{cross} to be smaller than V_{cross} absolute.

⁷ At default SMBus settings.

Electrical Characteristics–Current Consumption

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I _{DDR}	VDDR @100MHz		4	6	mA	1
	I _{DDDIG}	VDDIG, All outputs @100MHz		0.125	0.25	mA	1
	I _{DDAO}	VDDA+VDDO, PLL Mode, All outputs @100MHz		24	30	mA	1
Powerdown Current	I _{DDRPD}	VDDR, CKPWRGD_PD# = 0		0.1	0.3	mA	1,2,3
	I _{DDDIGPD}	VDDDIG, CKPWRGD_PD# = 0		0.1	0.2	mA	1,2
	I _{DDAOPD}	VDDA+VDDO, CKPWRGD_PD# = 0		0.5	1	mA	1,2

¹ Guaranteed by design and characterization, not 100% tested in production.

² Input clock stopped.

³ In bypass mode, the PLL is off and IDDAO is ~50% of this value.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PLL Bandwidth	BW	-3dB point in High BW Mode (100MHz)	2.2	3.6	4.8	MHz	1,5
		-3dB point in Low BW Mode (100MHz)	1	1.6	2.5	MHz	1,5
PLL Jitter Peaking	t _{JPEAK}	Peak Pass band Gain (100MHz)		1.3	2.5	dB	1
Duty Cycle	t _{DC}	Measured differentially, PLL Mode	45	50.2	55	%	1
Duty Cycle Distortion	t _{DCD}	Measured differentially, Bypass Mode @100MHz	-1	-0.6	0	%	1,3
Skew, Input to Output	t _{pdBYP}	Bypass Mode, V _T = 50%	3400	4300	5200	ps	1
	t _{pdPLL}	PLL Mode V _T = 50%	0	50	150	ps	1,4
Skew, Output to Output	t _{sk3}	V _T = 50%		37	50	ps	1,4
Jitter, Cycle to cycle	t _{jyc-cyc}	PLL mode		24	50	ps	1,2
		Additive Jitter in Bypass Mode		0.1	5	ps	1,2

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform

³ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

⁴ All outputs at default slew rate

⁵ The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

Electrical Characteristics–Phase Jitter Parameters

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	t _{jphPCIEG1}	PCIe Gen 1		30	58	86	ps (p-p)	1,2,3,5
	t _{jphPCIEG2}	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.9	1.4	3	ps (rms)	1,2,3,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.1	2.6	3.1	ps (rms)	1,2,3,5
	t _{jphPCIEG3}	PCIe Gen 3 Common Clock Architecture (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)		0.5	0.6	1	ps (rms)	1,2,3,5
	t _{jphPCIEG3SRns}	PCIe Gen 3 Separate Reference No Spread (SRnS) (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)		0.5	0.6	0.7	ps (rms)	1,2,3,5
Additive Phase Jitter, Bypass Mode	t _{jphPCIEG1}	PCIe Gen 1		0.1	5	N/A	ps (p-p)	1,2,3,5
	t _{jphPCIEG2}	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.1	0.5	N/A	ps (rms)	1,2,3,4,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.1	0.3	N/A	ps (rms)	1,2,3,4
	t _{jphPCIEG3}	PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)		0.2	0.3	N/A	ps (rms)	1,2,3,4
	t _{jph125M0}	125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		200	300	N/A	fs (rms)	1,6
	t _{jph125M1}	125MHz, 12KHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		313	350	N/A	fs (rms)	1,6

¹ Guaranteed by design and characterization, not 100% tested in production.

² See <http://www.pcisig.com> for complete specs

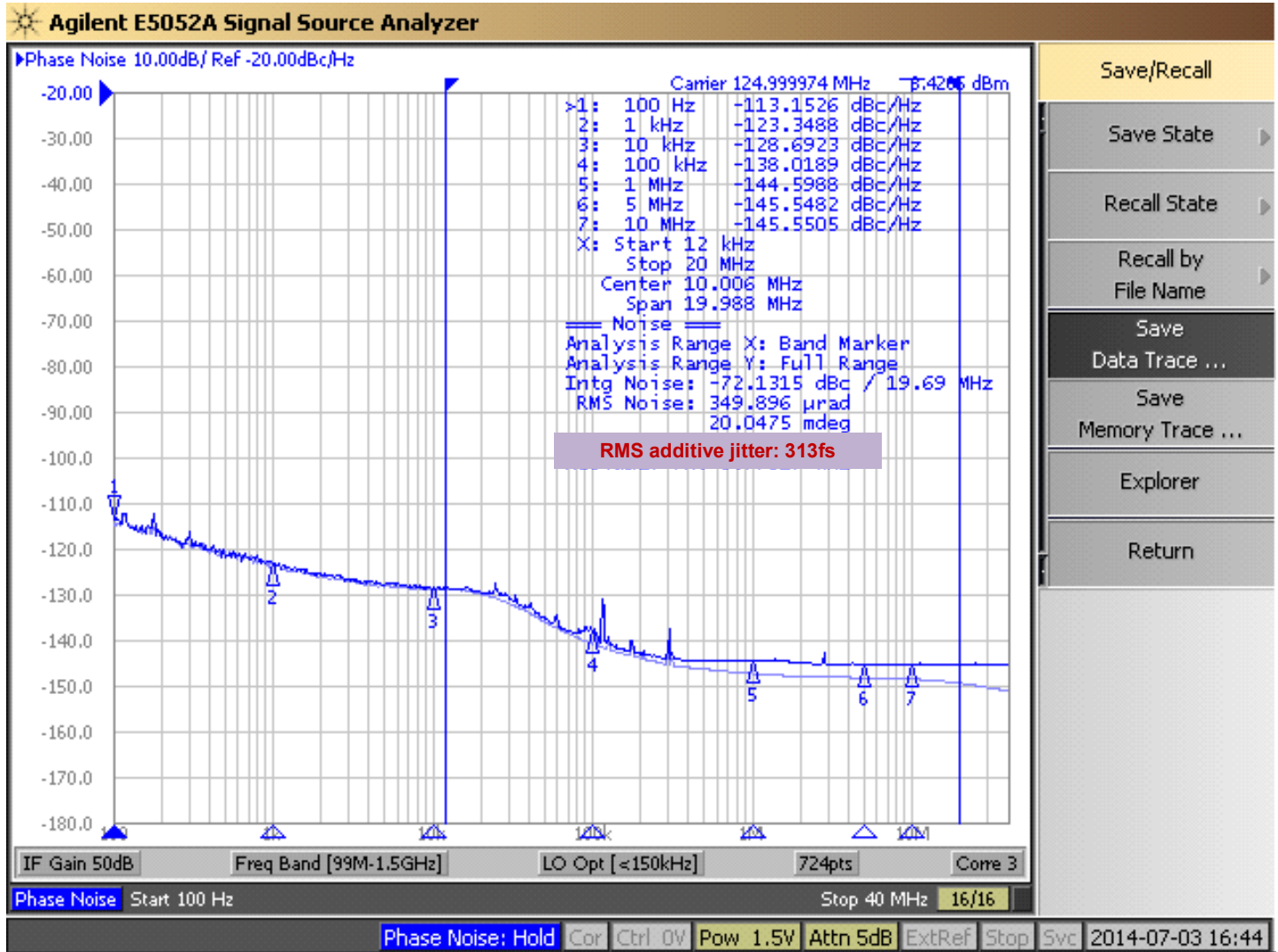
³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)² - (input jitter)²]

⁵ Driven by 9FGU0831 or equivalent

⁶ Rohde&Schartz SMA100

Additive Phase Jitter Plot: 125M (12kHz to 20MHz)



SMBus Table: Output Enable Register ¹

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	DIF OE3	Output Enable	RW	Low/Low	Enabled	1
Bit 5	DIF OE2	Output Enable	RW	Low/Low	Enabled	1
Bit 4	Reserved					1
Bit 3	DIF OE1	Output Enable	RW	Low/Low	Enabled	1
Bit 2	Reserved					1
Bit 1	DIF OE0	Output Enable	RW	Low/Low	Enabled	1
Bit 0	Reserved					1

1. A low on these bits will override the OE# pin and force the differential output Low/Low

SMBus Table: PLL Operating Mode and Output Amplitude Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	PLLMODERB1	PLL Mode Readback Bit 1	R	See PLL Operating Mode Table		Latch
Bit 6	PLLMODERB0	PLL Mode Readback Bit 0	R			Latch
Bit 5	PLLMODE_SWCNTRL	Enable SW control of PLL Mode	RW	Values in B1[7:6] set PLL Mode	Values in B1[4:3] set PLL Mode	0
Bit 4	PLLMODE1	PLL Mode Control Bit 1	RW ¹	See PLL Operating Mode Table		0
Bit 3	PLLMODE0	PLL Mode Control Bit 0	RW ¹			0
Bit 2	Reserved					1
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.55V	01 = 0.65V	1
Bit 0	AMPLITUDE 0		RW	10 = 0.75V	11 = 0.85V	0

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: DIF Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	SLEWRATESEL DIF3	Slew Rate Selection	RW	Slow Setting	Fast Setting	1
Bit 5	SLEWRATESEL DIF2	Slew Rate Selection	RW	Slow Setting	Fast Setting	1
Bit 4	Reserved					1
Bit 3	SLEWRATESEL DIF1	Slew Rate Selection	RW	Slow Setting	Fast Setting	1
Bit 2	Reserved					1
Bit 1	SLEWRATESEL DIF0	Slew Rate Selection	RW	Slow Setting	Fast Setting	1
Bit 0	Reserved					1

SMBus Table: FB Slew Rate Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Reserved					1
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					1
Bit 1	Reserved					1
Bit 0	SLEWRATESEL FB	Adjust Slew Rate of FB	RW	Slow Setting	Fast Setting	1

1. B3[5] must be set to a 1 for these bits to have any effect on the part.

Byte 4 is Reserved and reads back 'hFF'

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	A rev = 0000		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			0
Bit 3	VID3	VENDOR ID	R	0001 = IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

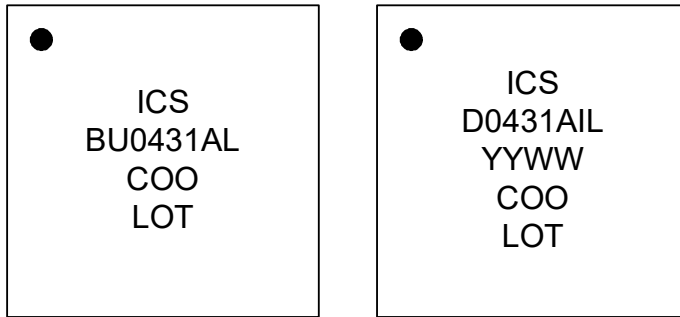
SMBus Table: Device Type/Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device Type1	Device Type	R	00 = FGx, 01 = DBx, 10 = DMx, 11= Reserved		0
Bit 6	Device Type0		R			1
Bit 5	Device ID5	Device ID	R	000100 binary or 04 hex		0
Bit 4	Device ID4		R			0
Bit 3	Device ID3		R			0
Bit 2	Device ID2		R			1
Bit 1	Device ID1		R			0
Bit 0	Device ID0		R			0

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7		Reserved				0
Bit 6		Reserved				0
Bit 5		Reserved				0
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Marking Diagrams



Notes:

1. "LOT" is the lot sequence number.
2. "COO" denotes country of origin.
3. YYWW is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. "L" denotes RoHS compliant package.
6. "I" denotes industrial temperature range device.

Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	NLG32	42	°C/W	1
	θ_{Jb}	Junction to Base		2.4	°C/W	1
	θ_{JA0}	Junction to Air, still air		39	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		33	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		28	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		27	°C/W	1

¹ePad soldered to board

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

32-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.5mm Pitch

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DBU0431AKLF	Trays	32-pin VFQFPN	0 to +70° C
9DBU0431AKLFT	Tape and Reel	32-pin VFQFPN	0 to +70° C
9DBU0431AKILF	Trays	32-pin VFQFPN	-40 to +85° C
9DBU0431AKILFT	Tape and Reel	32-pin VFQFPN	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Revision Date	Description
7/15/2014	<ol style="list-style-type: none"> Updated electrical tables with char data. Added an additive phase jitter plot. Added 12kHz to 20MHz <i>additive</i> phase jitter spec. Updated Amplitude control bit <i>descriptions</i> in Byte 1.
9/19/2014	Updated SMBus Input High/Low parameters conditions, MAX values, and footnotes.
4/22/2015	<ol style="list-style-type: none"> Updated pin out and pin descriptions to show ePad on package connected to ground. Updated front page text to standard format for these devices. Added explicit bullet indicated Spread Spectrum compatibility. Updated Clock Input Parameters table to be consistent with PCIe Vswing parameter. Minor updates to front page text for family consistency. Add note about epad to Power Connections table.
12/2/2025	<ol style="list-style-type: none"> Rebranded datasheet to Renesas. Updated "Alternate Terminations" section. Updated "Package Outline Drawings" section.

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