

## Four Output Differential Fanout Buffer for PCI Express Gen 1 & 2

*ICS9DBL411A*

### Recommended Application:

PCI-Express fanout buffer

### Output Features:

- 4 - low power differential output pairs
- Individual OE# control of each output pair

### Key Specifications:

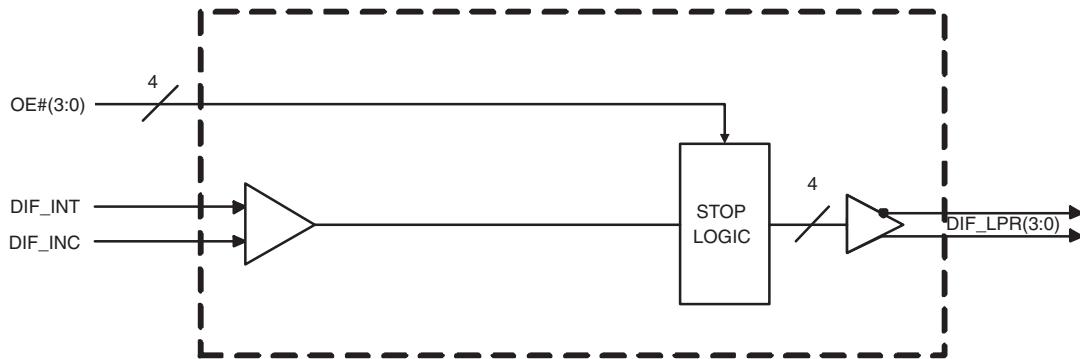
- Output cycle-cycle jitter < 25ps additive
- Output to output skew: < 50ps

### Power Groups

Pin Number (TSSOP)		Description
VDD	GND	
9,18	10,17	VDD_IO for DIF(3:0)
4	5	3.3V Analog VDD & GND

Pin Number (MLF)		Description
VDD	GND	
6,15	7,14	VDD_IO for DIF(3:0)
1	2	3.3V Analog VDD & GND

### Functional Block Diagram



## Pin Configuration

OE0#	1	20	DIF0T_LPR
DIF_INC	2	19	DIF0C_LPR
DIF_INT	3	18	VDD_IO
VDDA	4	17	GND
GNDA	5	16	OE1#
OE3#	6	15	DIF1T_LPR
DIF3C_LPR	7	14	DIF1C_LPR
DIF3T_LPR	8	13	OE2#
VDD_IO	9	12	DIF2T_LPR
GND	10	11	DIF2C_LPR

**ICS9DBL411**

20-pin TSSOP

DIF_INT	DIF_INC	OE0#	DIF0T_LPR	DIF0C_LPR
20	19	18	17	16
VDDA	1			15
GNDA	2			14
OE3#	3	9DBL411		13
DIF3C_LPR	4			12
DIF3T_LPR	5			11
VDD_IO	6	GND	DIF2C_LPR	DIF1T_LPR
	7		DIF2T_LPR	DIF1C_LPR
	8			OE1#
	9			OE2#
	10			

20-pin MLF

## TSSOP Pin Description

PIN # (TSSOP)	PIN NAME	PIN TYPE	DESCRIPTION
1	OE0#	IN	Output Enable for DIF0 output. Control is as follows: 0 = enabled, 1 = Low-Low
2	DIF_INC	IN	Complement side of differential input clock
3	DIF_INT	IN	True side of differential input clock
4	VDDA	PWR	3.3V Power for the Analog Core
5	GNDA	GND	Ground for the Analog Core
6	OE3#	IN	Output Enable for DIF3 output. Control is as follows: 0 = enabled, 1 = Low-Low
7	DIF3C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
8	DIF3T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
9	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
10	GND	GND	Ground pin
11	DIF2C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
12	DIF2T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
13	OE2#	IN	Output Enable for DIF2 output. Control is as follows: 0 = enabled, 1 = Low-Low
14	DIF1C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
15	DIF1T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
16	OE1#	IN	Output Enable for DIF1 output. Control is as follows: 0 = enabled, 1 = Low-Low
17	GND	GND	Ground pin
18	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
19	DIF0C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
20	DIF0T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)

## MLF Pin Description

PIN # (MLF)	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDA	PWR	3.3V Power for the Analog Core
2	GNDA	GND	Ground for the Analog Core
3	OE3#	IN	Output Enable for DIF3 output. Control is as follows: 0 = enabled, 1 = Low-Low
4	DIF3C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
5	DIF3T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
6	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
7	GND	GND	Ground pin
8	DIF2C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
9	DIF2T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
10	OE2#	IN	Output Enable for DIF2 output. Control is as follows: 0 = enabled, 1 = Low-Low
11	DIF1C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
12	DIF1T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
13	OE1#	IN	Output Enable for DIF1 output. Control is as follows: 0 = enabled, 1 = Low-Low
14	GND	GND	Ground pin
15	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
16	DIF0C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
17	DIF0T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
18	OE0#	IN	Output Enable for DIF0 output. Control is as follows: 0 = enabled, 1 = Low-Low
19	DIF_INC	IN	Complement side of differential input clock
20	DIF_INT	IN	True side of differential input clock

**Absolute Maximum Ratings**

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Maximum Supply Voltage	VDDA	Core Supply Voltage		4.6	V	1,7
Maximum Supply Voltage	VDD_IO	Low-Voltage Differential I/O Supply	0.99	3.8	V	1,7
Maximum Input Voltage	V <sub>IH</sub>	3.3V LVCMOS Inputs		4.6	V	1,7,8
Minimum Input Voltage	V <sub>IL</sub>	Any Input	V <sub>SS</sub> - 0.5		V	1,7
Storage Temperature	T <sub>S</sub>	-	-65	150	°C	1,7
Input ESD protection	ESD prot	Human Body Model	2000		V	1,7

**Electrical Characteristics - Input/Supply/Common Output Parameters**

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Ambient Operating Temp	T <sub>ambient</sub>	-	0	70	°C	1
Supply Voltage	VDDxxx	Supply Voltage	3.135	3.465	V	1
Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply	0.99	3.465	V	1
Input High Voltage	V <sub>IHSE</sub>	Single-ended inputs	2	V <sub>DD</sub> + 0.3	V	1
Input Low Voltage	V <sub>ILSE</sub>	Single-ended inputs	V <sub>SS</sub> - 0.3	0.8	V	1
Differential Input High Voltage	V <sub>IHDIF</sub>	Differential inputs (single-ended measurement)	600	1.15	V	1
Differential Input Low Voltage	V <sub>ILDIF</sub>	Differential inputs (single-ended measurement)	V <sub>SS</sub> - 0.3	300	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4	8	V/ns	2
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND	-5	5	uA	1
Operating Supply Current	I <sub>DD_3.3V</sub>	3.3V supply		25	mA	1
	I <sub>DD_IO+100M</sub>	VDD_IO supply @ fOP = 100MHz		15	mA	1
	I <sub>DD_IO_400M</sub>	VDD_IO supply @ fOP = 400MHz		54	mA	1
Standby Current	I <sub>DD_SB33</sub>	3.3V supply, Input stopped, OE# pins all high		1	mA	1
	I <sub>DD_SBIO</sub>	VDD_IO supply, Input stopped		0.1	mA	1
Input Frequency	F <sub>i</sub>	V <sub>DD</sub> = 3.3 V	33	400	MHz	2
Pin Inductance	L <sub>pin</sub>			7	nH	1
Input Capacitance	C <sub>IN</sub>	Logic Inputs	1.5	5	pF	1
	C <sub>OUT</sub>	Output pin capacitance		6	pF	1
OE# latency	T <sub>OE#LAT</sub>	Number of clocks to enable or disable output from assertion/deassertion of OE#	1	3	periods	1
Tdrive_OE#	T <sub>DROE#</sub>	Output enable after OE# de-assertion		10	ns	1
Tfall_OE#	T <sub>FALL</sub>	Fall/rise time of OE# inputs		5	ns	1
Trise_OE#	T <sub>RISE</sub>			5	ns	1

## AC Electrical Characteristics - DIF Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	$t_{SLR}$	Differential Measurement	1	2.5	V/ns	1,2
Falling Edge Slew Rate	$t_{FLR}$	Differential Measurement	1	2.5	V/ns	1,2
Slew Rate Variation	$t_{SLVAR}$	Single-ended Measurement		20	%	1
Maximum Output Voltage	$V_{HIGH}$	Includes overshoot		1150	mV	1
Minimum Output Voltage	$V_{LOW}$	Includes undershoot	-300		mV	1
Differential Voltage Swing	$V_{SWING}$	Differential Measurement	1200		mV	1
Crossing Point Voltage	$V_{XABS}$	Single-ended Measurement	300	550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		140	mV	1,3,5
Duty Cycle Distortion	$D_{CYCDIS0}$	Differential Measurement, $fIN \leq 100\text{MHz}$		0.5	%	1,6
	$D_{CYCDIS1}$	Differential Measurement $100\text{MHz} < fIN \leq 267\text{MHz}$		+5	%	1,6
	$D_{CYCDIS2}$	Differential Measurement, $fIN > 267\text{MHz}$		+7	%	1,6
DIF Jitter - Cycle to Cycle	$DIFJ_{C2C}$	Differential Measurement, <b>Additive</b>		25	ps	1
DIF[3:0] Skew	$DIF_{SKEW}$	Differential Measurement		50	ps	1
Propagation Delay	$t_{PD}$	Input to output Delay	2.5	3.5	ns	1
PCIe Gen2 Phase Jitter - Addtive	$t_{phase\_addHI}$	$1.5\text{MHz} < fIN < \text{Nyquist (50MHz)}$		0.8	ps rms	1
PCIe Gen2 Phase Jitter - Addtive	$t_{phase\_addLO}$	$10\text{KHz} < fIN < 1.5\text{MHz}$		0.1	ps rms	1

### Notes on Electrical Characteristics:

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Slew rate measured through Vswing centered around differential zero

<sup>3</sup>Vxabs is defined as the voltage where CLK = CLK#

<sup>4</sup>Only applies to the differential rising edge (CLK rising and CLK# falling)

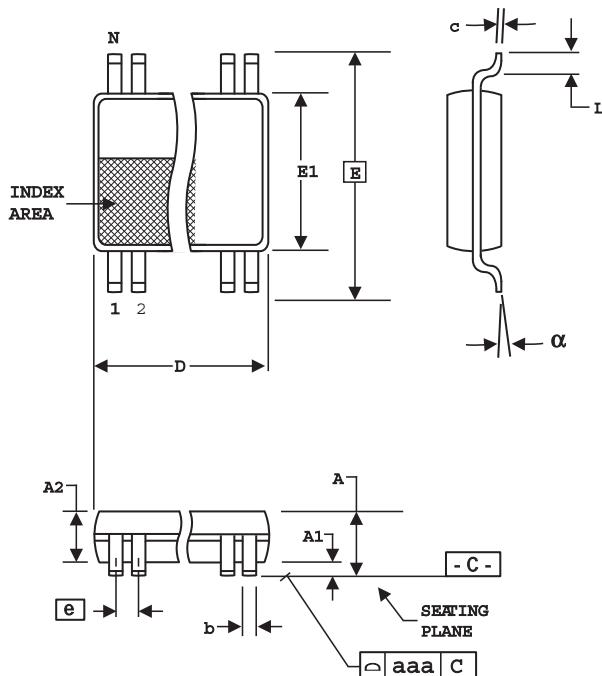
<sup>5</sup>Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

<sup>6</sup>This is the figure refers to the maximum distortion of the input wave form.

<sup>7</sup>Operation under these conditions is neither implied, nor guaranteed.

<sup>8</sup>Maximum input voltage is not to exceed maximum VDD

## 20-pin TSSOP Package Drawing and Dimensions



20-Lead, 4.40 mm. Body, 0.65 mm. Pitch TSSOP

(173 mil) (25.6 mil)

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS		COMMON DIMENSIONS	
A	—	1.20	—	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	—	0.10	—	.004

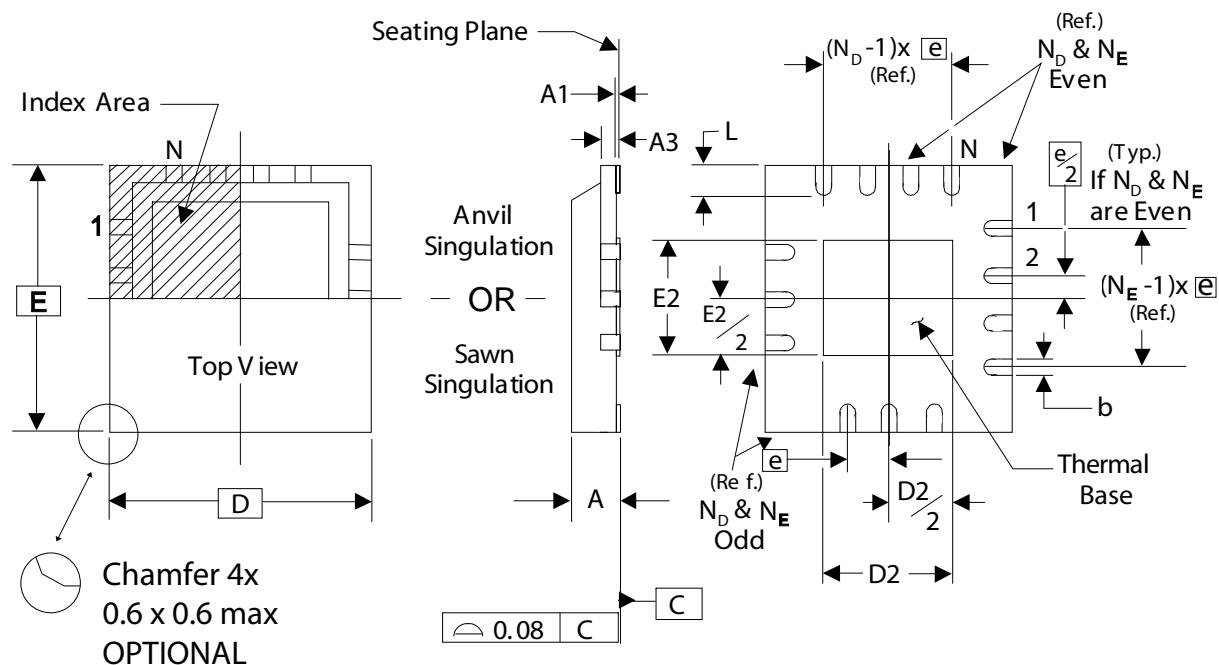
## VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
20	6.40	6.60	.252	.260

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

## 20-pin MLF Package Drawing and Dimensions



THERMALLY ENHANCED, VERY THIN, FINE PITCH  
QUAD FLAT / NO LEAD PLASTIC PACKAGE

### DIMENSIONS

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.3
e	0.50 BASIC	

### DIMENSIONS

SYMBOL	ICS 20L TOLERANCE
N	20
$N_D$	5
$N_E$	5
D x E BASIC	4.00 x 4.00
D2 MIN. / MAX.	2.00 / 2.25
E2 MIN. / MAX.	2.00 / 2.25
L MIN. / MAX.	0.45 / 0.65

## Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DBL411AKLF	Tubes	20-pin MLF	0 to +70°C
9DBL411AKLFT	Tape and Reel	20-pin MLF	0 to +70°C
9DBL411AGLF	Tubes	20-pin TSSOP	0 to +70°C
9DBL411AGLFT	Tape and Reel	20-pin TSSOP	0 to +70°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"A" is the device revision designator (will not correlate to the datasheet revision).

**Revision History**

Rev.	Issue Date	Description	Page #
0.1	8/1/2006	Initial Release.	-
0.2	9/22/2006	Updated MLF Package Dimensions.	8
A	7/31/2007	1. Updated electrical characteristics - additive jitter, cycle-to-cycle, tpd, skews, slew rates, Idd, etc. 2. Corrected power grouping table for TSSOP pkg 3. Final Release	1,5,6
B	2/21/2008	1. Highlighted that $V_{IHDF}$ and $V_{LDIF}$ are single ended measurements. 2. Corrected VSWING parameter from 300mV to 1200mV. 3. Updated duty cycle distortion table with a 3rd figure for speeds $\leq 100\text{MHz}$ .	5
C	6/28/2012	Typo for "Differential Input Low Voltage" units; changed "V" to "mV"	

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).