General Description
The ICS9DB803D is compatible with the Intel DB800v2 Differential Buffer Specification. This buffer provides 8 PCI-Express Gen2 clocks. The ICS9DB803D is driven by a differential output pair from a CK410B+, CK505 or CK509B main clock generator.

Recommended Application
DB800v2 compatible part with PCIe Gen1 and Gen2 Support

Output Features
• 8 - 0.7V current-mode differential output pairs
• Supports zero delay buffer mode and fanout mode
• Bandwidth programming available
• 50-100 MHz operation in PLL mode
• 50-400 MHz operation in Bypass mode

Features/Benefits
• Spread spectrum modulation tolerant, 0 to -0.5% down spread and +/- 0.25% center spread
• Supports undriven differential outputs in PD# and SRC_STOP# modes for power management

Key Specifications
• Outputs cycle-cycle jitter < 50ps
• Output to Output skew <50ps
• Phase jitter: PCIe Gen1 < 86ps peak to peak
• Phase jitter: PCIe Gen2 < 3.0/3.1ps rms

Functional Block Diagram

Note: Polarities shown are for OE_INV=0.
# Pin Configuration

<table>
<thead>
<tr>
<th>SRC_DIV#</th>
<th>VDDA</th>
<th>SRC_DIV#</th>
<th>VDDA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>48</td>
<td>2</td>
<td>47</td>
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<tr>
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<td>24</td>
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### Power Groups

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Description</th>
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<tbody>
<tr>
<td>2</td>
<td>SRC_IN/SRC_IN#</td>
</tr>
<tr>
<td>6, 11, 19, 31, 39</td>
<td>DIF(7:0)</td>
</tr>
<tr>
<td>10, 18, 25, 32</td>
<td>Analog VDD &amp; GND for PLL core</td>
</tr>
</tbody>
</table>

### Polarity Inversion Pin List Table

<table>
<thead>
<tr>
<th>Pins</th>
<th>OE_INV</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<tr>
<td>6</td>
<td>OE_0</td>
</tr>
<tr>
<td>7</td>
<td>OE_1</td>
</tr>
<tr>
<td>14</td>
<td>OE_3</td>
</tr>
<tr>
<td>15</td>
<td>OE_1</td>
</tr>
<tr>
<td>26</td>
<td>PD#</td>
</tr>
<tr>
<td>35</td>
<td>OE_4</td>
</tr>
<tr>
<td>36</td>
<td>OE_6</td>
</tr>
<tr>
<td>43</td>
<td>OE_7</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pins</th>
<th>OE_INV</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>OE_0#</td>
</tr>
<tr>
<td>7</td>
<td>OE_6#</td>
</tr>
<tr>
<td>14</td>
<td>OE_3#</td>
</tr>
<tr>
<td>15</td>
<td>OE_1#</td>
</tr>
<tr>
<td>26</td>
<td>PD</td>
</tr>
<tr>
<td>35</td>
<td>OE_4#</td>
</tr>
<tr>
<td>36</td>
<td>OE_7#</td>
</tr>
</tbody>
</table>

**IDS® EIGHT OUTPUT DIFFERENTIAL BUFFER FOR PCIe GEN1 AND GEN2**

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**Pin Descriptions for OE_INV=0**

<table>
<thead>
<tr>
<th>PIN #</th>
<th>PIN NAME</th>
<th>PIN TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SRC_DIV#</td>
<td>IN</td>
<td>Active low Input for determining SRC output frequency SRC or SRC/2. 0 = SRC/2, 1= SRC</td>
</tr>
<tr>
<td>2</td>
<td>VDD</td>
<td>PWR</td>
<td>3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>PWR</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>4</td>
<td>SRC_IN</td>
<td>IN</td>
<td>0.7 V Differential SRC TRUE input</td>
</tr>
<tr>
<td>5</td>
<td>SRC_IN#</td>
<td>IN</td>
<td>0.7 V Differential SRC COMPLEMENTARY input</td>
</tr>
<tr>
<td>6</td>
<td>OE_0</td>
<td>IN</td>
<td>Active high input for enabling output 0. 0 = disable outputs, 1 = enable outputs</td>
</tr>
<tr>
<td>7</td>
<td>OE_3</td>
<td>IN</td>
<td>Active high input for enabling output 3. 0 = disable outputs, 1 = enable outputs</td>
</tr>
<tr>
<td>8</td>
<td>DIF_0</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>9</td>
<td>DIF_0#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>PWR</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>11</td>
<td>VDD</td>
<td>PWR</td>
<td>Power supply, nominal 3.3V</td>
</tr>
<tr>
<td>12</td>
<td>DIF_1</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>13</td>
<td>DIF_1#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>14</td>
<td>OE_1</td>
<td>IN</td>
<td>Active high input for enabling output 1. 0 = disable outputs, 1 = enable outputs</td>
</tr>
<tr>
<td>15</td>
<td>OE_2</td>
<td>IN</td>
<td>Active high input for enabling output 2. 0 = disable outputs, 1 = enable outputs</td>
</tr>
<tr>
<td>16</td>
<td>DIF_2</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>17</td>
<td>DIF_2#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>PWR</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>19</td>
<td>VDD</td>
<td>PWR</td>
<td>Power supply, nominal 3.3V</td>
</tr>
<tr>
<td>20</td>
<td>DIF_3</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>21</td>
<td>DIF_3#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>22</td>
<td>BYPASS#/PLL</td>
<td>IN</td>
<td>Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode</td>
</tr>
<tr>
<td>23</td>
<td>SCLK</td>
<td>IN</td>
<td>Clock pin of SMBus circuitry, 5V tolerant.</td>
</tr>
<tr>
<td>24</td>
<td>SDATA</td>
<td>I/O</td>
<td>Data pin for SMBus circuitry, 5V tolerant.</td>
</tr>
</tbody>
</table>
## Pin Descriptions for OE_INV=0 (cont.)

<table>
<thead>
<tr>
<th>PIN #</th>
<th>PIN NAME</th>
<th>PIN TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>GND</td>
<td>PWR</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>26</td>
<td>PD#</td>
<td>IN</td>
<td>Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal osc. (if any) are stopped.</td>
</tr>
<tr>
<td>27</td>
<td>DIF_STOP#</td>
<td>IN</td>
<td>Active low input to stop differential output clocks.</td>
</tr>
<tr>
<td>28</td>
<td>HIGH_BW#</td>
<td>PWR</td>
<td>3.3V input for selecting PLL Band Width 0 = High, 1 = Low</td>
</tr>
<tr>
<td>29</td>
<td>DIF_4#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>30</td>
<td>DIF_4</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>31</td>
<td>VDD</td>
<td>PWR</td>
<td>Power supply, nominal 3.3V</td>
</tr>
<tr>
<td>32</td>
<td>GND</td>
<td>PWR</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>33</td>
<td>DIF_5#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>34</td>
<td>DIF_5</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>35</td>
<td>OE_5</td>
<td>IN</td>
<td>Active high input for enabling output 5. 0 = disable outputs, 1 = enable outputs</td>
</tr>
<tr>
<td>36</td>
<td>OE_6</td>
<td>IN</td>
<td>Active high input for enabling output 6. 0 = disable outputs, 1 = enable outputs</td>
</tr>
<tr>
<td>37</td>
<td>DIF_6#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>38</td>
<td>DIF_6</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>39</td>
<td>VDD</td>
<td>PWR</td>
<td>Power supply, nominal 3.3V</td>
</tr>
<tr>
<td>40</td>
<td>OE_INV</td>
<td>IN</td>
<td>This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#)</td>
</tr>
<tr>
<td>41</td>
<td>DIF_7#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>42</td>
<td>DIF_7</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>43</td>
<td>OE_4</td>
<td>IN</td>
<td>Active high input for enabling output 4. 0 = disable outputs, 1 = enable outputs</td>
</tr>
<tr>
<td>44</td>
<td>OE_7</td>
<td>IN</td>
<td>Active high input for enabling output 7. 0 = disable outputs, 1 = enable outputs</td>
</tr>
<tr>
<td>45</td>
<td>LOCK</td>
<td>OUT</td>
<td>3.3V output indicating PLL Lock Status. This pin goes high when lock is achieved.</td>
</tr>
<tr>
<td>46</td>
<td>IREF</td>
<td>IN</td>
<td>This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet.</td>
</tr>
<tr>
<td>47</td>
<td>GNDA</td>
<td>PWR</td>
<td>Ground pin for the PLL core.</td>
</tr>
<tr>
<td>48</td>
<td>VDDA</td>
<td>PWR</td>
<td>3.3V power for the PLL core.</td>
</tr>
</tbody>
</table>
## Pin Descriptions for OE_INV=1

<table>
<thead>
<tr>
<th>PIN #</th>
<th>PIN NAME</th>
<th>PIN TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SRC_DIV#</td>
<td>IN</td>
<td>Active low Input for determining SRC output frequency SRC or SRC/2. 0 = SRC/2, 1 = SRC</td>
</tr>
<tr>
<td>2</td>
<td>VDDR</td>
<td>PWR</td>
<td>3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>PWR</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>4</td>
<td>SRC_IN</td>
<td>IN</td>
<td>0.7 V Differential SRC TRUE input</td>
</tr>
<tr>
<td>5</td>
<td>SRC_IN#</td>
<td>IN</td>
<td>0.7 V Differential SRC COMPLEMENTARY input</td>
</tr>
<tr>
<td>6</td>
<td>OE0#</td>
<td>IN</td>
<td>Active low input for enabling DIF pair 0. 1 = disable outputs, 0 = enable outputs</td>
</tr>
<tr>
<td>7</td>
<td>OE3#</td>
<td>IN</td>
<td>Active low input for enabling DIF pair 3. 1 = disable outputs, 0 = enable outputs</td>
</tr>
<tr>
<td>8</td>
<td>DIF_0</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>9</td>
<td>DIF_0#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>PWR</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>11</td>
<td>VDD</td>
<td>PWR</td>
<td>Power supply, nominal 3.3V</td>
</tr>
<tr>
<td>12</td>
<td>DIF_1</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>13</td>
<td>DIF_1#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>14</td>
<td>OE1#</td>
<td>IN</td>
<td>Active low input for enabling DIF pair 1. 1 = disable outputs, 0 = enable outputs</td>
</tr>
<tr>
<td>15</td>
<td>OE2#</td>
<td>IN</td>
<td>Active low input for enabling DIF pair 2. 1 = disable outputs, 0 = enable outputs</td>
</tr>
<tr>
<td>16</td>
<td>DIF_2</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>17</td>
<td>DIF_2#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>PWR</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>19</td>
<td>VDD</td>
<td>PWR</td>
<td>Power supply, nominal 3.3V</td>
</tr>
<tr>
<td>20</td>
<td>DIF_3</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>21</td>
<td>DIF_3#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>22</td>
<td>BYPASS#/PLL</td>
<td>IN</td>
<td>Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1 = PLL mode</td>
</tr>
<tr>
<td>23</td>
<td>SCLK</td>
<td>IN</td>
<td>Clock pin of SMBus circuitry, 5V tolerant.</td>
</tr>
<tr>
<td>24</td>
<td>SDATA</td>
<td>I/O</td>
<td>Data pin for SMBus circuitry, 5V tolerant.</td>
</tr>
</tbody>
</table>
### Pin Descriptions for OE_INV=1 (cont.)

<table>
<thead>
<tr>
<th>PIN #</th>
<th>PIN NAME</th>
<th>PIN TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>GND</td>
<td>PWR</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>26</td>
<td>PD</td>
<td>IN</td>
<td>Asynchronous active high input pin used to power down the device. The internal clocks are disabled and the VCO is stopped.</td>
</tr>
<tr>
<td>27</td>
<td>DIF_STOP</td>
<td>IN</td>
<td>Active High input to stop differential output clocks.</td>
</tr>
<tr>
<td>28</td>
<td>HIGH_BW#</td>
<td>PWR</td>
<td>3.3V input for selecting PLL Band Width 0 = High, 1= Low</td>
</tr>
<tr>
<td>29</td>
<td>DIF_4#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>30</td>
<td>DIF_4</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>31</td>
<td>VDD</td>
<td>PWR</td>
<td>Power supply, nominal 3.3V</td>
</tr>
<tr>
<td>32</td>
<td>GND</td>
<td>PWR</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>33</td>
<td>DIF_5#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>34</td>
<td>DIF_5</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>35</td>
<td>OE5#</td>
<td>IN</td>
<td>Active low input for enabling DIF pair 5. 1 = disable outputs, 0 = enable outputs</td>
</tr>
<tr>
<td>36</td>
<td>OE6#</td>
<td>IN</td>
<td>Active low input for enabling DIF pair 6. 1 = disable outputs, 0 = enable outputs</td>
</tr>
<tr>
<td>37</td>
<td>DIF_6#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>38</td>
<td>DIF_6</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>39</td>
<td>VDD</td>
<td>PWR</td>
<td>Power supply, nominal 3.3V</td>
</tr>
<tr>
<td>40</td>
<td>OE_INV</td>
<td>IN</td>
<td>This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#)</td>
</tr>
<tr>
<td>41</td>
<td>DIF_7#</td>
<td>OUT</td>
<td>0.7V differential Complementary clock output</td>
</tr>
<tr>
<td>42</td>
<td>DIF_7</td>
<td>OUT</td>
<td>0.7V differential true clock output</td>
</tr>
<tr>
<td>43</td>
<td>OE4#</td>
<td>IN</td>
<td>Active low input for enabling DIF pair 4 1 = disable outputs, 0 = enable outputs</td>
</tr>
<tr>
<td>44</td>
<td>OE7#</td>
<td>IN</td>
<td>Active low input for enabling DIF pair 7. 1 = disable outputs, 0 = enable outputs</td>
</tr>
<tr>
<td>45</td>
<td>LOCK</td>
<td>OUT</td>
<td>3.3V output indicating PLL Lock Status. This pin goes high when lock is achieved.</td>
</tr>
<tr>
<td>46</td>
<td>IREF</td>
<td>IN</td>
<td>This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet.</td>
</tr>
<tr>
<td>47</td>
<td>GNDA</td>
<td>PWR</td>
<td>Ground pin for the PLL core.</td>
</tr>
<tr>
<td>48</td>
<td>VDDA</td>
<td>PWR</td>
<td>3.3V power for the PLL core.</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS9DB803D. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDA/R</td>
<td>3.3V Core Supply Voltage</td>
<td>4.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>3.3V Logic Supply Voltage</td>
<td>4.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>GND-0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>VDD+0.5V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Ts</td>
<td>Storage Temperature</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Tambient</td>
<td>Commercial Operating Range</td>
<td>0</td>
<td>70</td>
<td>°C</td>
</tr>
<tr>
<td>Tcase</td>
<td>Case Temperature</td>
<td>115</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>ESD prot</td>
<td>Input ESD protection human body model</td>
<td>2000</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Electrical Characteristics—Clock Input Parameters

\( T_A = \) Tambient for the desired operating range, Supply Voltage \( V_{DD} = 3.3 \) V +/-5%

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input High Voltage - DIF_IN</td>
<td>( V_{IHDF} )</td>
<td>Differential inputs (single-ended measurement)</td>
<td>600</td>
<td>800</td>
<td>1150</td>
<td>mV</td>
<td>1</td>
</tr>
<tr>
<td>Input Low Voltage - DIF_IN</td>
<td>( V_{ILDF} )</td>
<td>Differential inputs (single-ended measurement)</td>
<td>( V_{SS} ) - 300</td>
<td>0</td>
<td>300</td>
<td>mV</td>
<td>1</td>
</tr>
<tr>
<td>Input Common Mode Voltage - DIF_IN</td>
<td>( V_{COM} )</td>
<td>Common Mode Input Voltage</td>
<td>300</td>
<td>1000</td>
<td>mV</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Input Amplitude - DIF_IN</td>
<td>( V_{SWING} )</td>
<td>Peak to Peak value (single-ended measurement)</td>
<td>300</td>
<td>1450</td>
<td>mV</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Input Slew Rate - DIF_IN</td>
<td>( dv/dt )</td>
<td>Measured differentially</td>
<td>0.4</td>
<td>8</td>
<td>V/ns</td>
<td>1,2</td>
<td></td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>( I_{IN} )</td>
<td>( V_{IN} = V_{DD}, V_{IN} = GND )</td>
<td>-5</td>
<td>5</td>
<td>uA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Input Duty Cycle</td>
<td>( d_{in} )</td>
<td>Measurement from differential waveform</td>
<td>45</td>
<td>55</td>
<td>%</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Input Jitter - Cycle to Cycle</td>
<td>( J_{DFin} )</td>
<td>Differential Measurement</td>
<td>0</td>
<td>125</td>
<td>ps</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

1 Guaranteed by design and characterization, not 100% tested in production.
2 Slew rate measured through \( V_{swing} \) min centered around differential zero
## Electrical Characteristics—Input/Supply/Common Output Parameters

\( T_A = \text{Tambient for the desired operating range, Supply Voltage } V_{DD} = 3.3 \text{ V} \pm/5\% \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input High Voltage</td>
<td>( V_{IHSE} )</td>
<td>Single Ended Inputs, 3.3 V +/-5%</td>
<td>2</td>
<td></td>
<td></td>
<td>( V_{DD} + 0.3 ) V</td>
<td>1</td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>( V_{ILSE} )</td>
<td></td>
<td>GND - 0.3</td>
<td>0.8</td>
<td>V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Input High Current</td>
<td>( I_{IL1} )</td>
<td>( V_{IN} = V_{DD} ); Inputs with no pull-up resistors</td>
<td>-5</td>
<td>5</td>
<td>uA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Input Low Current</td>
<td>( I_{IL2} )</td>
<td>( V_{IN} = 0 \text{ V} ); Inputs with pull-up resistors</td>
<td>-200</td>
<td>uA</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9DB803 Supply Current</td>
<td>( I_{DD3.3PDC} )</td>
<td>Full Active, ( C_L ) = Full load; Commercial Temp Range</td>
<td>175</td>
<td>200</td>
<td>mA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>9DB803 Powerdown Current</td>
<td>( I_{DD3.3PDI} )</td>
<td>Full Active, ( C_L ) = Full load; Industrial Temp Range</td>
<td>190</td>
<td>225</td>
<td>mA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>9DB403 Supply Current</td>
<td>( I_{DD3.3PDC} )</td>
<td>Full Active, ( C_L ) = Full load; Commercial Temp Range</td>
<td>105</td>
<td>125</td>
<td>mA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>9DB403 Powerdown Current</td>
<td>( I_{DD3.3PDI} )</td>
<td>Full Active, ( C_L ) = Full load; Industrial Temp Range</td>
<td>115</td>
<td>150</td>
<td>mA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Input Frequency</td>
<td>( F_{PLL} )</td>
<td>PCIe Mode (Bypass#/PLL= 1)</td>
<td>50</td>
<td>100</td>
<td>MHz</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( F_{BYPASS} )</td>
<td>Bypass Mode ((Bypass#/PLL= 0)</td>
<td>33</td>
<td>400</td>
<td>MHz</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Pin Inductance</td>
<td>( L_{PIN} )</td>
<td></td>
<td>7</td>
<td></td>
<td>nH</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Capacitance</td>
<td>( C_{IN} )</td>
<td>Logic Inputs, except SRC_IN</td>
<td>1.5</td>
<td>5</td>
<td>pF</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( C_{INSRC_IN} )</td>
<td>SRC_IN differential clock inputs</td>
<td>1.5</td>
<td>2.7</td>
<td>pF</td>
<td>1,4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( C_{OUT} )</td>
<td>Output pin capacitance</td>
<td></td>
<td>6</td>
<td>pF</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>PLL Bandwidth</td>
<td>( BW )</td>
<td>-3dB point in High BW Mode</td>
<td>2</td>
<td>3</td>
<td>MHz</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>-3dB point in Low BW Mode</td>
<td>0.7</td>
<td>1</td>
<td>1.4</td>
<td>MHz</td>
<td>1</td>
</tr>
<tr>
<td>PLL Jitter Peaking</td>
<td>( t_{JPEAK} )</td>
<td>Peak Pass band Gain</td>
<td>1.5</td>
<td>2</td>
<td>dB</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Cik Stabilization</td>
<td>( t_{STAB} )</td>
<td>From ( V_{DD} ) Power-Up and after input clock stabilization or de-assertion of ( PD# ) to 1st clock</td>
<td>1</td>
<td></td>
<td>ms</td>
<td>1,2</td>
<td></td>
</tr>
<tr>
<td>Input SS Modulation Frequency</td>
<td>( f_{MODN} )</td>
<td>Allowable Frequency (Triangular Modulation)</td>
<td>30</td>
<td>33</td>
<td>kHz</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>OE# Latency</td>
<td>( t_{LATDEA} )</td>
<td>DIF start after OE# assertion</td>
<td>1</td>
<td>3</td>
<td>cycles</td>
<td>1,3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DIF stop after OE# deassertion</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tdrive_SRC_STOP#</td>
<td>( t_{DRVSTP} )</td>
<td>DIF output enable after SRC_STOP# de-assertion</td>
<td>10</td>
<td>ns</td>
<td>1,3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tdrive_PD#</td>
<td>( t_{DRVPD} )</td>
<td>DIF output enable after ( PD# ) de-assertion</td>
<td>300</td>
<td>us</td>
<td>1,3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tfall</td>
<td>( t_{F} )</td>
<td>Fall time of ( PD# ) and SRC_STOP#</td>
<td>5</td>
<td>ns</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Trise</td>
<td>( t_{R} )</td>
<td>Rise time of ( PD# ) and SRC_STOP#</td>
<td>5</td>
<td>ns</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBus Voltage</td>
<td>( V_{MAX} )</td>
<td>Maximum input voltage</td>
<td>5.5</td>
<td>V</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low-level Output Voltage</td>
<td>( V_{OL} )</td>
<td>@ ( I_{PULLUP} )</td>
<td>0.4</td>
<td>V</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current sinking at ( V_{OL} )</td>
<td>( I_{PULLUP} )</td>
<td></td>
<td>4</td>
<td>mA</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCLK/SDATA Clock/Data Rise Time</td>
<td>( t_{RISMB} )</td>
<td>(Max ( VIL - 0.15 ) to (Min ( VIH + 0.15 )</td>
<td>1000</td>
<td>ns</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCLK/SDATA Clock/Data Fall Time</td>
<td>( t_{RISMB} )</td>
<td>(Min ( VIH + 0.15 ) to (Max ( VIL - 0.15 )</td>
<td>300</td>
<td>ns</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBus Operating Frequency</td>
<td>( f_{MAXSMB} )</td>
<td>Maximum SMBus operating frequency</td>
<td>100</td>
<td>kHz</td>
<td>1,5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1Guaranteed by design and characterization, not 100% tested in production.

2See timing diagrams for timing requirements.

3Time from deassertion until outputs are >200 mV

4SRC_IN input

5The differential input clock must be running for the SMBus to be active
## Electrical Characteristics—DIF 0.7V Current Mode Differential Pair

\( T_A = \text{Tambient}; \ V_{DD} = 3.3 \ \text{V +/-5\%}; \ C_L = 2 \text{pF}; \ R_S = 33\Omega; \ R_P = 49.9\Omega; \ R_{REF} = 475\Omega \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Source Output</td>
<td>Zo</td>
<td></td>
<td>3000</td>
<td></td>
<td></td>
<td>Ω</td>
<td>1</td>
</tr>
<tr>
<td>Impedance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage High</td>
<td>VHigh</td>
<td>Statistical measurement on single ended signal using oscilloscope math function.</td>
<td>660</td>
<td>850</td>
<td></td>
<td>mV</td>
<td>1,2</td>
</tr>
<tr>
<td>Voltage Low</td>
<td>VLow</td>
<td></td>
<td>-150</td>
<td>150</td>
<td></td>
<td>mV</td>
<td>1,2</td>
</tr>
<tr>
<td>Max Voltage</td>
<td>Vovs</td>
<td>Measurement on single ended signal using absolute value.</td>
<td></td>
<td></td>
<td>1150</td>
<td>mV</td>
<td>1</td>
</tr>
<tr>
<td>Min Voltage</td>
<td>Vuds</td>
<td></td>
<td></td>
<td></td>
<td>-300</td>
<td>mV</td>
<td>1</td>
</tr>
<tr>
<td>Crossing Voltage (abs)</td>
<td>Vcross(abs)</td>
<td></td>
<td>250</td>
<td>550</td>
<td></td>
<td>mV</td>
<td>1</td>
</tr>
<tr>
<td>Crossing Voltage (var)</td>
<td>d-Vcross</td>
<td>Variation of crossing over all edges</td>
<td></td>
<td>140</td>
<td></td>
<td>mV</td>
<td>1</td>
</tr>
<tr>
<td>Rise Time</td>
<td>tr</td>
<td>V_{OL} = 0.175V; V_{OH} = 0.525V</td>
<td>175</td>
<td>700</td>
<td></td>
<td>ps</td>
<td>1</td>
</tr>
<tr>
<td>Fall Time</td>
<td>tf</td>
<td>V_{OH} = 0.525V; V_{OL} = 0.175V</td>
<td>175</td>
<td>700</td>
<td></td>
<td>ps</td>
<td>1</td>
</tr>
<tr>
<td>Rise Time Variation</td>
<td>d-tr</td>
<td></td>
<td>125</td>
<td></td>
<td></td>
<td>ps</td>
<td>1</td>
</tr>
<tr>
<td>Fall Time Variation</td>
<td>d-tf</td>
<td></td>
<td>125</td>
<td></td>
<td></td>
<td>ps</td>
<td>1</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>d_{3}</td>
<td>Measurement from differential waveform</td>
<td>45</td>
<td>55</td>
<td></td>
<td>%</td>
<td>1</td>
</tr>
<tr>
<td>Skew, Input to Output</td>
<td>t_{dBYP}</td>
<td>Bypass Mode, \ V_T = 50%</td>
<td>2500</td>
<td>4500</td>
<td></td>
<td>ps</td>
<td>1</td>
</tr>
<tr>
<td>Skew, Output to Output</td>
<td>t_{dPLL}</td>
<td>PLL Mode \ V_T = 50%</td>
<td>-250</td>
<td>250</td>
<td></td>
<td>ps</td>
<td>1</td>
</tr>
<tr>
<td>Jitter, Cycle to cycle</td>
<td>t_{j-cyc}</td>
<td>Additive Jitter in Bypass Mode</td>
<td>50</td>
<td></td>
<td></td>
<td>ps</td>
<td>1,3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td></td>
<td>ps</td>
<td>1,3</td>
</tr>
</tbody>
</table>

\( ^1 \text{Guaranteed by design and characterization, not 100\% tested in production.} \)

\( ^2 \text{IRE} = \frac{V_{DD}}{3 \times R_R}. \text{ For } R_R = 475\Omega (1\%), \text{ I_{REF} = 2.32mA}. \text{ I_{OH} = 6 \times I_{REF} and V_{OH} = 0.7V @ Z_O=50\Omega.} \)

\( ^3 \text{Measured from differential waveform} \)

\( ^4 \text{See http://www.pcisig.com for complete specs} \)

\( ^5 \text{Device driven by 932S421C or equivalent.} \)

\( ^6 \text{First number is High Bandwidth Mode, second number is Low Bandwidth Mode} \)
### Clock Periods–Differential Outputs with Spread Spectrum Enabled

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Measurement Window</th>
<th>Symbol</th>
<th>Absolute Period</th>
<th>Short-term Average</th>
<th>Long-Term Average</th>
<th>Period</th>
<th>Long-Term Average</th>
<th>Short-term Average</th>
<th>Period</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIF 100</td>
<td></td>
<td>Lg-</td>
<td>9.87400</td>
<td>9.99900</td>
<td>9.99900</td>
<td>10.00000</td>
<td>10.00100</td>
<td>10.05130</td>
<td>ns</td>
<td>1,2,3</td>
<td></td>
</tr>
<tr>
<td>DIF 133</td>
<td></td>
<td>Lg-</td>
<td>7.41425</td>
<td>7.49925</td>
<td>7.49925</td>
<td>7.50000</td>
<td>7.50075</td>
<td>7.53845</td>
<td>ns</td>
<td>1,2,4</td>
<td></td>
</tr>
<tr>
<td>DIF 166</td>
<td></td>
<td>Lg-</td>
<td>5.91440</td>
<td>5.99940</td>
<td>5.99940</td>
<td>6.00000</td>
<td>6.00060</td>
<td>6.03076</td>
<td>ns</td>
<td>1,2,4</td>
<td></td>
</tr>
<tr>
<td>DIF 200</td>
<td></td>
<td>Lg-</td>
<td>4.91450</td>
<td>4.99950</td>
<td>4.99950</td>
<td>5.00000</td>
<td>5.00050</td>
<td>5.02563</td>
<td>ns</td>
<td>1,2,4</td>
<td></td>
</tr>
<tr>
<td>DIF 266</td>
<td></td>
<td>Lg-</td>
<td>3.66463</td>
<td>3.74963</td>
<td>3.74963</td>
<td>3.75000</td>
<td>3.75038</td>
<td>3.76922</td>
<td>ns</td>
<td>1,2,4</td>
<td></td>
</tr>
<tr>
<td>DIF 333</td>
<td></td>
<td>Lg-</td>
<td>2.91470</td>
<td>2.99970</td>
<td>2.99970</td>
<td>3.00000</td>
<td>3.00030</td>
<td>3.01538</td>
<td>ns</td>
<td>1,2,4</td>
<td></td>
</tr>
<tr>
<td>DIF 400</td>
<td></td>
<td>Lg-</td>
<td>2.41475</td>
<td>2.49975</td>
<td>2.49975</td>
<td>2.50000</td>
<td>2.50025</td>
<td>2.51282</td>
<td>ns</td>
<td>1,2,4</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. Guaranteed by design and characterization, not 100% tested in production.
2. All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK409/CK410/CK505 accuracy requirements. The 9DB403/803 itself does not contribute to ppm error.
3. Driven by SRC output of main clock, PLL or Bypass mode
4. Driven by CPU output of CK410/CK505 main clock, **Bypass mode only**

### Clock Periods–Differential Outputs with Spread Spectrum Disabled

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Measurement Window</th>
<th>Symbol</th>
<th>Absolute Period</th>
<th>Short-term Average</th>
<th>Long-Term Average</th>
<th>Period</th>
<th>Long-Term Average</th>
<th>Short-term Average</th>
<th>Period</th>
<th>Units</th>
<th>Notes</th>
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<tbody>
<tr>
<td>DIF 100</td>
<td></td>
<td>Lg-</td>
<td>9.87400</td>
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<td>DIF 133</td>
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<td>Lg-</td>
<td>7.41425</td>
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<td>7.50075</td>
<td>7.62345</td>
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<td>DIF 166</td>
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<td>5.99940</td>
<td>5.99940</td>
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<td>6.00060</td>
<td>6.11576</td>
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<td>1,2,4</td>
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<tr>
<td>DIF 200</td>
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<td>Lg-</td>
<td>4.91450</td>
<td>4.99950</td>
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<td>DIF 266</td>
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<td>Lg-</td>
<td>3.66463</td>
<td>3.74963</td>
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<td>3.75000</td>
<td>3.75038</td>
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<tr>
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<td>Lg-</td>
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<td>2.50025</td>
<td>2.59782</td>
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### SRC Reference Clock

<table>
<thead>
<tr>
<th>Common Recommendations for Differential Routing</th>
<th>Dimension or Value</th>
<th>Unit</th>
<th>Figure</th>
</tr>
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<tbody>
<tr>
<td>L1 length, route as non-coupled 50ohm trace</td>
<td>0.5 max</td>
<td>inch</td>
<td>1</td>
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<tr>
<td>L2 length, route as non-coupled 50ohm trace</td>
<td>0.2 max</td>
<td>inch</td>
<td>1</td>
</tr>
<tr>
<td>L3 length, route as non-coupled 50ohm trace</td>
<td>0.2 max</td>
<td>inch</td>
<td>1</td>
</tr>
<tr>
<td>Rs</td>
<td>33</td>
<td>ohm</td>
<td>1</td>
</tr>
<tr>
<td>Rt</td>
<td>48.9</td>
<td>ohm</td>
<td>1</td>
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### Down Device Differential Routing

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<th>Unit</th>
<th>Figure</th>
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<tr>
<td>L4 length, route as coupled microstrip 100ohm differential trace</td>
<td>2 min to 16 max</td>
<td>inch</td>
<td>1</td>
</tr>
<tr>
<td>L4 length, route as coupled stripline 100ohm differential trace</td>
<td>1.8 min to 14.4 max</td>
<td>inch</td>
<td>1</td>
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### Differential Routing to PCI Express Connector

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<th>Dimension or Value</th>
<th>Unit</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>L4 length, route as coupled microstrip 100ohm differential trace</td>
<td>0.25 to 14 max</td>
<td>inch</td>
<td>2</td>
</tr>
<tr>
<td>L4 length, route as coupled stripline 100ohm differential trace</td>
<td>0.225 min to 12.6 max</td>
<td>inch</td>
<td>2</td>
</tr>
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</table>
Alternative Termination for LVDS and other Common Differential Signals (figure 3)

<table>
<thead>
<tr>
<th>Vdiff</th>
<th>Vp-p</th>
<th>Vcm</th>
<th>R1</th>
<th>R2</th>
<th>R3</th>
<th>R4</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.45v</td>
<td>0.22v</td>
<td>1.08</td>
<td>33</td>
<td>150</td>
<td>100</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>0.58</td>
<td>0.28</td>
<td>0.6</td>
<td>33</td>
<td>78.7</td>
<td>137</td>
<td>100</td>
<td>ICS874003i-02 input compatible</td>
</tr>
<tr>
<td>0.80</td>
<td>0.40</td>
<td>0.6</td>
<td>33</td>
<td>78.7</td>
<td>none</td>
<td>100</td>
<td>Standard LVDS</td>
</tr>
<tr>
<td>0.60</td>
<td>0.3</td>
<td>1.2</td>
<td>33</td>
<td>174</td>
<td>140</td>
<td>100</td>
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</tr>
</tbody>
</table>

R1a = R1b = R1
R2a = R2b = R2

Cable Connected AC Coupled Application (figure 4)

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>R5a, R5b</td>
<td>8.2K 5%</td>
<td></td>
</tr>
<tr>
<td>R6a, R6b</td>
<td>1K   5%</td>
<td></td>
</tr>
<tr>
<td>Cc</td>
<td>0.1 µF</td>
<td></td>
</tr>
<tr>
<td>Vcm</td>
<td>0.350 volts</td>
<td></td>
</tr>
</tbody>
</table>
General SMBus Serial Interface Information

How to Write
- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) sends the byte count = X
- IDT clock will acknowledge
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will acknowledge each byte one at a time
- Controller (host) sends a Stop bit

How to Read
- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will acknowledge
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends Byte 0 through Byte X (if X(H) was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

<table>
<thead>
<tr>
<th>Controller (Host)</th>
<th>IDT (Slave/Receiver)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T starT bit</td>
<td>ACK</td>
</tr>
<tr>
<td>Slave Address</td>
<td>ACK</td>
</tr>
<tr>
<td>WR WRite</td>
<td>ACK</td>
</tr>
<tr>
<td>Beginning Byte = N</td>
<td>ACK</td>
</tr>
<tr>
<td>Data Byte Count = X</td>
<td>ACK</td>
</tr>
<tr>
<td>Beginning Byte N</td>
<td>ACK</td>
</tr>
<tr>
<td>O</td>
<td>ACK</td>
</tr>
<tr>
<td>O</td>
<td>ACK</td>
</tr>
<tr>
<td>O</td>
<td>ACK</td>
</tr>
<tr>
<td>Byte N + X - 1</td>
<td>ACK</td>
</tr>
<tr>
<td>P stopP bit</td>
<td>ACK</td>
</tr>
</tbody>
</table>

Index Block Read Operation

<table>
<thead>
<tr>
<th>Controller (Host)</th>
<th>IDT (Slave/Receiver)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T starT bit</td>
<td>ACK</td>
</tr>
<tr>
<td>Slave Address</td>
<td>ACK</td>
</tr>
<tr>
<td>WR WRite</td>
<td>ACK</td>
</tr>
<tr>
<td>Beginning Byte = N</td>
<td>ACK</td>
</tr>
<tr>
<td>RT Repeat starT</td>
<td>ACK</td>
</tr>
<tr>
<td>Slave Address</td>
<td>ACK</td>
</tr>
<tr>
<td>RD ReaD</td>
<td>ACK</td>
</tr>
<tr>
<td>Data Byte Count=X</td>
<td>ACK</td>
</tr>
<tr>
<td>ACK</td>
<td>X Byte</td>
</tr>
<tr>
<td>O</td>
<td>Byte N + X - 1</td>
</tr>
<tr>
<td>O</td>
<td></td>
</tr>
<tr>
<td>O</td>
<td></td>
</tr>
<tr>
<td>P stopP bit</td>
<td></td>
</tr>
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</table>

Read Address | Write Address
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DD(H)</td>
<td>DC(H)</td>
</tr>
<tr>
<td>N</td>
<td>Not acknowledge</td>
</tr>
<tr>
<td>P</td>
<td>stopP bit</td>
</tr>
</tbody>
</table>
### SMBus Table: Frequency Select Register, READ/ WRITE ADDRESS (DC/DD)

<table>
<thead>
<tr>
<th>Byte 0</th>
<th>Pin #</th>
<th>Name</th>
<th>Control Function</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>PWD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>-</td>
<td>PD_Mode</td>
<td>PD# drive mode</td>
<td>RW</td>
<td>driven</td>
<td>Hi-Z</td>
<td>0</td>
</tr>
<tr>
<td>Bit 6</td>
<td>-</td>
<td>STOP_Mode</td>
<td>DIF_Stop# drive mode</td>
<td>RW</td>
<td>driven</td>
<td>Hi-Z</td>
<td>0</td>
</tr>
<tr>
<td>Bit 5</td>
<td>-</td>
<td>Reserved</td>
<td>Reserved</td>
<td>RW</td>
<td>Reserved</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Bit 4</td>
<td>-</td>
<td>Reserved</td>
<td>Reserved</td>
<td>RW</td>
<td>Reserved</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Bit 3</td>
<td>-</td>
<td>Reserved</td>
<td>Reserved</td>
<td>RW</td>
<td>Reserved</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Bit 2</td>
<td>-</td>
<td>PLL_BW#</td>
<td>Select PLL BW</td>
<td>RW</td>
<td>High BW</td>
<td>Low BW</td>
<td>1</td>
</tr>
<tr>
<td>Bit 1</td>
<td>-</td>
<td>BYPASS#</td>
<td>BYPASS#/PLL</td>
<td>RW</td>
<td>fan-out</td>
<td>ZDB</td>
<td>1</td>
</tr>
<tr>
<td>Bit 0</td>
<td>-</td>
<td>SRC_DIV#</td>
<td>SRC Divide by 2 Select</td>
<td>RW</td>
<td>x/2</td>
<td>1x</td>
<td>1</td>
</tr>
</tbody>
</table>

### SMBus Table: Output Control Register

<table>
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<th>Pin #</th>
<th>Name</th>
<th>Control Function</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>PWD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>DIF_7</td>
<td>Output Enable</td>
<td>RW Disable Stoppeable</td>
<td>RW</td>
<td>Disable</td>
<td>Enable</td>
<td>1</td>
</tr>
<tr>
<td>Bit 6</td>
<td>DIF_6</td>
<td>Output Enable</td>
<td>RW Disable Stoppeable</td>
<td>RW</td>
<td>Disable</td>
<td>Enable</td>
<td>1</td>
</tr>
<tr>
<td>Bit 5</td>
<td>DIF_5</td>
<td>Output Enable</td>
<td>RW Disable Stoppeable</td>
<td>RW</td>
<td>Disable</td>
<td>Enable</td>
<td>1</td>
</tr>
<tr>
<td>Bit 4</td>
<td>DIF_4</td>
<td>Output Enable</td>
<td>RW Disable Stoppeable</td>
<td>RW</td>
<td>Disable</td>
<td>Enable</td>
<td>1</td>
</tr>
<tr>
<td>Bit 3</td>
<td>DIF_3</td>
<td>Output Enable</td>
<td>RW Disable Stoppeable</td>
<td>RW</td>
<td>Disable</td>
<td>Enable</td>
<td>1</td>
</tr>
<tr>
<td>Bit 2</td>
<td>DIF_2</td>
<td>Output Enable</td>
<td>RW Disable Stoppeable</td>
<td>RW</td>
<td>Disable</td>
<td>Enable</td>
<td>1</td>
</tr>
<tr>
<td>Bit 1</td>
<td>DIF_1</td>
<td>Output Enable</td>
<td>RW Disable Stoppeable</td>
<td>RW</td>
<td>Disable</td>
<td>Enable</td>
<td>1</td>
</tr>
<tr>
<td>Bit 0</td>
<td>DIF_0</td>
<td>Output Enable</td>
<td>RW Disable Stoppeable</td>
<td>RW</td>
<td>Disable</td>
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### SMBus Table: OE Pin Control Register Control Register

<table>
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<th>Pin #</th>
<th>Name</th>
<th>Control Function</th>
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<th>PWD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>DIF_7</td>
<td>DIF_7 Stoppeable with DIFSTOP</td>
<td>RW Free-run Stoppeable</td>
<td>RW</td>
<td>Free-run</td>
<td>Stoppable</td>
<td>0</td>
</tr>
<tr>
<td>Bit 6</td>
<td>DIF_6</td>
<td>DIF_6 Stoppeable with DIFSTOP</td>
<td>RW Free-run Stoppeable</td>
<td>RW</td>
<td>Free-run</td>
<td>Stoppable</td>
<td>0</td>
</tr>
<tr>
<td>Bit 5</td>
<td>DIF_5</td>
<td>DIF_5 Stoppeable with DIFSTOP</td>
<td>RW Free-run Stoppeable</td>
<td>RW</td>
<td>Free-run</td>
<td>Stoppable</td>
<td>0</td>
</tr>
<tr>
<td>Bit 4</td>
<td>DIF_4</td>
<td>DIF_4 Stoppeable with DIFSTOP</td>
<td>RW Free-run Stoppeable</td>
<td>RW</td>
<td>Free-run</td>
<td>Stoppable</td>
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<td>Bit 3</td>
<td>DIF_3</td>
<td>DIF_3 Stoppeable with DIFSTOP</td>
<td>RW Free-run Stoppeable</td>
<td>RW</td>
<td>Free-run</td>
<td>Stoppable</td>
<td>0</td>
</tr>
<tr>
<td>Bit 2</td>
<td>DIF_2</td>
<td>DIF_2 Stoppeable with DIFSTOP</td>
<td>RW Free-run Stoppeable</td>
<td>RW</td>
<td>Free-run</td>
<td>Stoppable</td>
<td>0</td>
</tr>
<tr>
<td>Bit 1</td>
<td>DIF_1</td>
<td>DIF_1 Stoppeable with DIFSTOP</td>
<td>RW Free-run Stoppeable</td>
<td>RW</td>
<td>Free-run</td>
<td>Stoppable</td>
<td>0</td>
</tr>
<tr>
<td>Bit 0</td>
<td>DIF_0</td>
<td>DIF_0 Stoppeable with DIFSTOP</td>
<td>RW Free-run Stoppeable</td>
<td>RW</td>
<td>Free-run</td>
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### SMBus Table: Reserved Register

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<th>Pin #</th>
<th>Name</th>
<th>Control Function</th>
<th>Type</th>
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<th>1</th>
<th>PWD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td></td>
<td>Reserved</td>
<td>RW Reserved</td>
<td>RW</td>
<td>Reserved</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Bit 6</td>
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<td>Reserved</td>
<td>RW Reserved</td>
<td>RW</td>
<td>Reserved</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Bit 5</td>
<td></td>
<td>Reserved</td>
<td>RW Reserved</td>
<td>RW</td>
<td>Reserved</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Bit 4</td>
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<td>RW Reserved</td>
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<td>Reserved</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Bit 3</td>
<td></td>
<td>Reserved</td>
<td>RW Reserved</td>
<td>RW</td>
<td>Reserved</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Bit 2</td>
<td></td>
<td>Reserved</td>
<td>RW Reserved</td>
<td>RW</td>
<td>Reserved</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Bit 1</td>
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<td>Reserved</td>
<td>RW Reserved</td>
<td>RW</td>
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<td>Bit 0</td>
<td></td>
<td>Reserved</td>
<td>RW Reserved</td>
<td>RW</td>
<td>Reserved</td>
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</table>
### SMBus Table: Vendor & Revision ID Register

<table>
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<th>Byte 4</th>
<th>Pin #</th>
<th>Name</th>
<th>Control Function</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>PWD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>-</td>
<td>RID3</td>
<td>REVISION ID</td>
<td>R</td>
<td>-</td>
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<td>X</td>
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<tr>
<td>Bit 6</td>
<td>-</td>
<td>RID2</td>
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<td>R</td>
<td>-</td>
<td>-</td>
<td>X</td>
</tr>
<tr>
<td>Bit 5</td>
<td>-</td>
<td>RID1</td>
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<td>R</td>
<td>-</td>
<td>-</td>
<td>X</td>
</tr>
<tr>
<td>Bit 4</td>
<td>-</td>
<td>RID0</td>
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<td>R</td>
<td>-</td>
<td>-</td>
<td>X</td>
</tr>
<tr>
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<td>VID3</td>
<td>VENDOR ID</td>
<td>R</td>
<td>-</td>
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</tr>
<tr>
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<tr>
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<td>VID1</td>
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<tr>
<td>Bit 0</td>
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<td>VID0</td>
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<td>R</td>
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<td>-</td>
<td>1</td>
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</tbody>
</table>

### SMBus Table: DEVICE ID

<table>
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<tr>
<th>Byte 5</th>
<th>Pin #</th>
<th>Name</th>
<th>Control Function</th>
<th>Type</th>
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<th>1</th>
<th>PWD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>-</td>
<td>Device ID 7</td>
<td>Device ID 7 (MSB)</td>
<td>RW</td>
<td>0</td>
<td></td>
<td>0</td>
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<tr>
<td>Bit 6</td>
<td>-</td>
<td>Device ID 6</td>
<td></td>
<td>RW</td>
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<td></td>
<td>X</td>
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<tr>
<td>Bit 5</td>
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<td>RW</td>
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<td>X</td>
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<td>Bit 4</td>
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<tr>
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<td>1</td>
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<tr>
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<td>-</td>
<td>Device ID 0</td>
<td></td>
<td>RW</td>
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Device ID is 83 Hex for 9DB803 and 43 Hex for 9DB403

### SMBus Table: Byte Count Register

<table>
<thead>
<tr>
<th>Byte 6</th>
<th>Pin #</th>
<th>Name</th>
<th>Control Function</th>
<th>Type</th>
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<th>PWD</th>
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</thead>
<tbody>
<tr>
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<td>RW</td>
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<td>Bit 6</td>
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<td>BC6</td>
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<td>BC5</td>
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<td>Bit 4</td>
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<td>BC4</td>
<td>Writing to this register configures how many bytes will be read back.</td>
<td>RW</td>
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<td>0</td>
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<td>Bit 3</td>
<td>-</td>
<td>BC3</td>
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<td>-</td>
<td>0</td>
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<td>Bit 2</td>
<td>-</td>
<td>BC2</td>
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<td>RW</td>
<td>-</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Bit 1</td>
<td>-</td>
<td>BC1</td>
<td></td>
<td>RW</td>
<td>-</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Bit 0</td>
<td>-</td>
<td>BC0</td>
<td></td>
<td>RW</td>
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<td>-</td>
<td>1</td>
</tr>
</tbody>
</table>
Note: Polarities in timing diagrams are shown OE_INV = 0. They are similar to OE_INV = 1.

**PD#, Power Down**

The PD# pin cleanly shuts off all clocks and places the device into a power saving mode. PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown. PD is asynchronous active-low input for both powering down the device and powering up the device. When PD# is asserted, all clocks will be driven high, or tri-stated (depending on the PD# drive mode and Output control bits) before the PLL is shut down.

**PD# Assertion**

When PD# is sampled low by two consecutive rising edges of DIF#, all DIF outputs must be held High, or tri-stated (depending on the PD# drive mode and Output control bits) on the next High-Low transition of the DIF# outputs. When the PD# drive mode bit is set to ‘0’, all clock outputs will be held with DIF driven High with 2 x IREF and DIF# tri-stated. If the PD# drive mode bit is set to ‘1’, both DIF and DIF# are tri-stated.

**PD# De-assertion**

Power-up latency is less than 1 ms. This is the time from de-assertion of the PD# pin, or VDD reaching 3.3V, or the time from valid SRC_IN clocks until the time that stable clocks are output from the device (PLL Locked). If the PD# drive mode bit is set to ‘1’, all the DIF outputs must driven to a voltage of >200 mV within 300 us of PD# de-assertion.
**SRC_STOP#**

The SRC_STOP# signal is an active-low asynchronous input that cleanly stops and starts the DIF outputs. A valid clock must be present on SRC_IN for this input to work properly. The SRC_STOP# signal is de-bounced and must remain stable for two consecutive rising edges of DIF# to be recognized as a valid assertion or de-assertion.

**SRC_STOP# - Assertion**

Asserting SRC_STOP# causes all DIF outputs to stop after their next transition (if the control register settings allow the output to stop). When the SRC_STOP# drive bit is ‘0’, the final state of all stopped DIF outputs is DIF = High and DIF# = Low. There is no change in output drive current. DIF is driven with 6xIREF. DIF# is not driven, but pulled low by the termination. When the SRC_STOP# drive bit is ‘1’, the final state of all DIF output pins is Low. Both DIF and DIF# are not driven.

**SRC_STOP# - De-assertion (transition from '0' to '1')**

All stopped differential outputs resume normal operation in a glitch-free manner. The de-assertion latency to active outputs is 2-6 DIF clock periods, with all DIF outputs resuming simultaneously. If the SRC_STOP# drive control bit is ‘1’ (tri-state), all stopped DIF outputs must be driven High (>200 mV) within 10 ns of de-assertion.

**SRC_STOP_1 (SRC_Stop = Driven, PD = Driven)**

![Diagram of SRC_STOP_1](image)

**SRC_STOP_2 (SRC_Stop = Tristate, PD = Driven)**

![Diagram of SRC_STOP_2](image)
**SRC_STOP_3 (SRC_Stop = Driven, PD = Tristate)**

![Waveform Diagram for SRC_STOP_3](image1)

**SRC_STOP_4 (SRC_Stop = Tristate, PD = Tristate)**

![Waveform Diagram for SRC_STOP_4](image2)
Package Outline and Package Dimensions (48-pin TSSOP)

Package dimensions are kept current with JEDEC Publication No. 95

<table>
<thead>
<tr>
<th>Symbol</th>
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<th>Min</th>
<th>Max</th>
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<td>0.15</td>
<td>0.002</td>
<td>0.006</td>
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<td>12.60</td>
<td>0.488</td>
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<td>E</td>
<td>8.10 BASIC</td>
<td>0.319 BASIC</td>
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<td>0.236</td>
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<td>e</td>
<td>0.50 Basic</td>
<td>0.020 Basic</td>
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<td>L</td>
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*For reference only. Controlling dimensions in mm.
Package Outline and Package Dimensions (48-pin SSOP)

Package dimensions are kept current with JEDEC Publication No. 95

<table>
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<th>Symbol</th>
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<th>Max</th>
<th>Min</th>
<th>Max</th>
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<td>.008</td>
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*For reference only. Controlling dimensions in mm.

Ordering Information

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<th>Part / Order Number</th>
<th>Marking</th>
<th>Shipping Packaging</th>
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<td>9DB803DGLF</td>
<td>9DB803DGLF</td>
<td>Tubes</td>
<td>48-pin TSSOP</td>
<td>0 to +70° C</td>
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<td>9DB803DGLFT</td>
<td>9DB803DGLF</td>
<td>Tape and Reel</td>
<td>48-pin TSSOP</td>
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<td>9DB803DGILF</td>
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<td>48-pin TSSOP</td>
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<td>9DB803DGILFT</td>
<td>9DB803DGILF</td>
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<td>48-pin SSOP</td>
<td>-40 to +85° C</td>
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<td>Tape and Reel</td>
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<td>-40 to +85° C</td>
</tr>
</tbody>
</table>

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.
“D” is the device revision designator (will not correlate with the datasheet revision).

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## Revision History

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<th>Rev</th>
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<th>Issuer</th>
<th>Description</th>
<th>Page #</th>
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<td>A</td>
<td>8/15/2006</td>
<td></td>
<td>Updated electrical characteristics for final data sheet</td>
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<td>B</td>
<td>2/29/2008</td>
<td></td>
<td>Added Input Clock Specs</td>
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<tr>
<td>C</td>
<td>3/18/2008</td>
<td></td>
<td>Fixed typo in Input Clock Parameters</td>
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<tr>
<td>D</td>
<td>3/28/2008</td>
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<td>Updated Electrical Char tables</td>
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<td>F</td>
<td>4/10/2008</td>
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<td>Updated Input Clock Specs</td>
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<tr>
<td>G</td>
<td>1/13/2009</td>
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<td>Corrected part ordering information</td>
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| H   | 10/7/2009  |        | 1. Clarified that Vih and Vil values were for Single ended inputs  
      2. Added Differential Clock input parameters.  
      3. Updated Electrical Characteristics to add propagation delay and  
         phase noise information.  
      4. Added SMBus electrical characteristics  
      5. Added foot note about DIF input running in order for the SMBus  
         interface to work  
      6. Added foot note to Byte 1 about functionality of OE bits and OE  
         pins.  
      7. Updated/Reformatted General Description | Various |
| J   | 1/27/2011  |        | Updated Termination Figure 4 | 12     |
| K   | 5/9/2011   |        | 1. Updated pin 2 pin-name and pin description from VDD to VDDR. This  
      highlights that optimal performance is obtained by treating VDDR as an  
      analog pin. This is a document update only, there is no silicon change. | Various |
| L   | 8/27/2012  |        | Updated Byte 2, bits 0–7 per char review. Outputs can be programmed  
      with Byte 2 to be Stoppable or Free-Run with DIF_Stop pin, not the OE  
      pins. | 7      |
| M   | 9/18/2012  |        | Typo discovered on front page "Output Features" section. Was: "50 –  
      110MHz operation in PLL mode"; changed to: "50 – 100MHz operation  
      in PLL mode" | 14     |
| N   | 7/10/2013  | R. Wei | Typo discovered on front page "Output Features" section. Was: "50 –  
      110MHz operation in PLL mode"; changed to: "50 – 100MHz operation  
      in PLL mode" | 1      |
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