Frequency Generator and Integrated Buffers for Intel Pentium and Pentium Pro™ µP's

General Description

The **ICS9169-01** generates all clocks required for high speed RISC or CISC microprocessor systems such as 486, Pentium/ Pentium Pro™, PowerPC™, etc. Four different reference frequency multiplying factors are externally selectable with smooth frequency transitions. These multiplying factors can be customized for specific applications. A test mode is provided to drive all clocks directly.

High drive BCLK outputs typically provide greater than 1V/ ns slew rate into 30pF loads. PCLK outputs typically provide better than 1V/ns slew rate into 20pF loads while maintaining 50±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates.

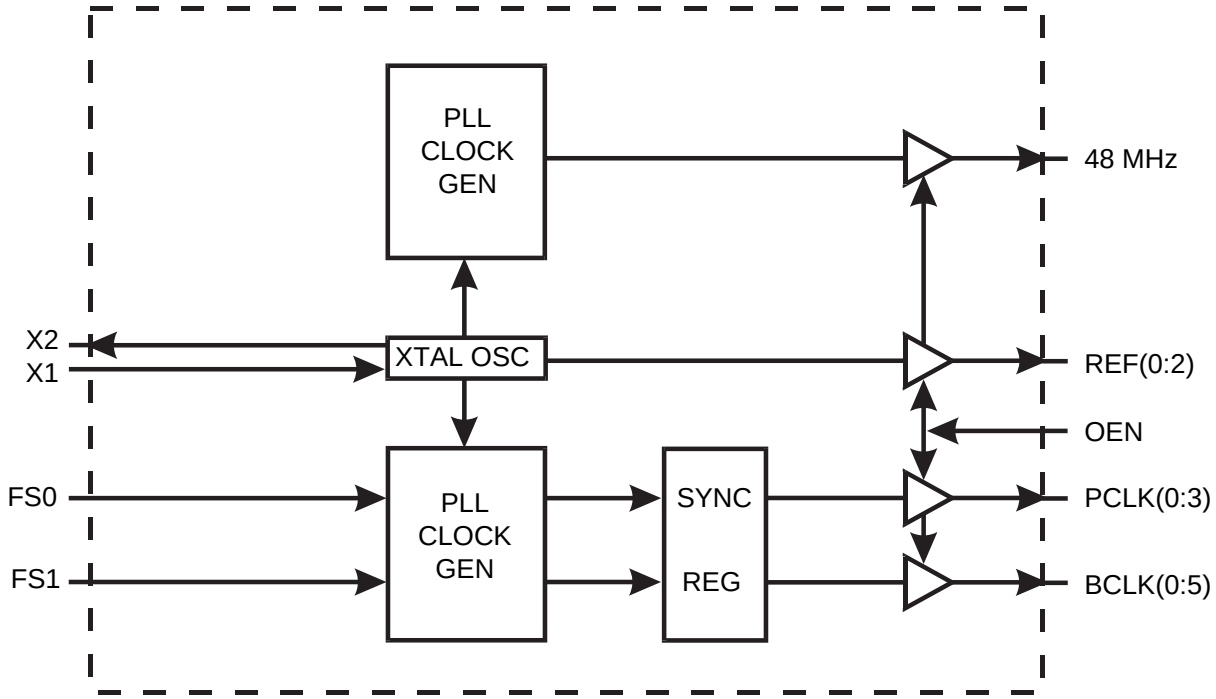
Features

- Generates four processor, six bus, three 14.318 MHz and one 48 MHz clock for ISA bus, audio, super I/O and bus bridge devices
- Supports the Intel MARS chip set
- Synchronous clocks skew matched to 250ps window on PCLKs and 500ps window on BCLKs
- Test clock mode eases system design
- Selectable multiplying ratios
- Custom configurations available
- Output frequency ranges to 100 MHz (depending on option)
- 3.0V - 5.5 V supply range
- 28-pin SOIC and 28-pin SSOP (209-mil) packages

Applications

- Ideal for high-speed RISC or CISC systems such as 486, Pentium, Pentium Pro, PowerPC, etc.

Block Diagram



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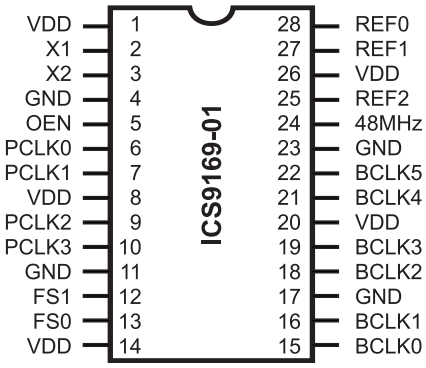
PowerPC is a trademark of Motorola Corporation

Pin Configuration



28 Pin SOIC

28 Pin SSOP

Functionality

FS1	FS0	*VCO	X1, REF (MHz)	PCLK(0:3) (MHz)
0	0	230/33x X1	14.31818	50 (49.7)
0	1	212/23x X1	14.31818	66 (66.5)
1	0	176/21x X1	14.31818	60 (59.9)
1	1	Test mode	TCLK	TCLK/2

*VCO range is limited from 60 - 200 MHz

PCLK(0:3)	BCLK(0:5)	48 MHz
VCO/2	PCLK/2	48 MHz
TCLK/2	TCLK/4	TCLK/2

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 12.16 MHz crystal, nominally 14.31818
3	X2	OUT	XTAL output which includes XTAL load capacitance.
4, 11, 23	GND	PWR	Ground for logic, PCLK and fixed frequency output buffers.
17	GND	PWR	Ground for BCLK output buffers.
1, 8, 26	VDD	PWR	Power for logic, PCLK and fixed frequency output buffers.
14, 20	VDD	PWR	Power for BCLK output buffers.
6, 7, 9, 10	PCLK(0:3)	OUT	Processor clock outputs which are a multiple of the input reference frequency as shown in the table above.
13, 12	FS(0:1)	IN	Frequency multiplier select pins. See table above. These inputs have internal pull-up devices.
15, 16, 18 19, 21, 22	BCLK(0:5)	OUT	Bus clock outputs are fixed at 1/2 the PCLK frequency.
5	OEN	IN	OEN tristates all outputs when low. This input has an internal pull-up device.
24	48MHz	OUT	Fixed 48 MHz clock (with 14.318 MHz input).
28, 27, 25	REF(0:2)	OUT	REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz.

Note 1: BCLK buffers cannot be supplied with 5 volts (pins 14 and 20) if CPU and fixed frequencies (pins 1, 8, and 26) are being supplied with 3.3 volts

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND - 0.5 V to VDD + 0.5 V

Ambient Operating Temperature ..... 0 to +70 C

Storage Temperature ..... -65 to +150 C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stess specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3 V

V_{DD} = 3.0 - 3.7 V, T_A = 0 - 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN} = 0 V	-28.0	-10.5	-	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5.0	-	5.0	µA
Output Low Current[1]	I_{OL}	V_{OL} = 0.8 V; for PCLKs & BCLKs	30.0	47.0	-	mA
Output High Current[1]	I_{OH}	V_{OL} = 2.0 V; for PCLKs & BCLKs	-	-66.0	-42.0	mA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for fixed CLKs	25.0	38.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V; for fixed CLKs	-	-47.0	-30.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL} = 15 mA; for PCLKs & BCLKs	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH} = -30 mA; for PCLKs & BCLKs	2.4	2.8	-	V
Output Low Voltage[1]	V_{OL}	I_{OL}=12.5mA; for fixed CLKs	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH} = -20mA; for fixed CLKs	2.4	2.8	-	V
Supply Current	I_{DD}	@ 66.5 MHz; all outputs unloaded	-	55	110	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3 V

V_{DD} = 3.0 - 3.7 V, T_A = 0 - 70°C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V PCLK & BCLK	-	0.9	1.5	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V PCLK & BCLK	-	0.8	1.4	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80% PCLK & BCLK	-	1.5	2.5	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20% PCLK & BCLK	-	1.4	2.4	ns
Duty Cycle[1]	D_t	20pF load @ V_{OUT} = 1.4 V	45	50	55	%
Jitter, One Sigma[1]	T_{j1s1}	PCLK & BCLK Clocks; Load=20pF, F_{OUT} >25 MHz	-	50	150	ps
Jitter, Absolute[1]	T_{jab1}	PCLK & BCLK Clocks; Load=20pF, F_{OUT} >25 MHz	-250	-	250	ps
Jitter, One Sigma[1]	T_{j1s2}	Fixed CLK; Load=20pF	-	1	3	%
Jitter, Absolute[1]	T_{jab2}	Fixed CLK; Load=20pF	-5	2	5	%
Input Frequency[1]	F_j		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]	C_{INX}	X1, X2 pins	-	18	-	pF
Power-on Time[1]	t_{on}	From V_{DD}=1.6V to 1st crossing of 66.5 MHz V_{DD} supply ramp < 40 ms	-	2.5	4.5	ms
Frequency Settling Time[1]	t_s	From 1st crossing of acquisition to < 1% settling	-	2.0	4.0	ms
Clock Skew Window[1]	T_{sk1}	PCLK to PCLK; Load=20pF; @1.4V	-	150	250	ps
Clock Skew Window[1]	T_{sk2}	BCLK to BCLK; Load=20pF; @1.4V	-	300	500	ps
Clock Skew Window[1]	T_{sk3}	PCLK to BCLK; Load=20pF; @1.4V	1	2.6	5	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 5.0 V

V_{DD} = 4.5 - 5.5 V, T_A = 0 - 70 °C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.4	-	-	V
Input Low Current	I_{IL}	V_{IN} = 0 V	-45	-15	-	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5.0	-	5.0	µA
Output Low Current[1]	I_{OL}	V_{OL} = 0.8 V; for PCLKs & BCLKs	36.0	62.0	-	mA
Output High Current[1]	I_{OH}	V_{OL} = 2.0 V; for PCLKs & BCLKs	-	-152	-90.0	mA
Output Low Current[1]	I_{OL}	V_{OL} = 0.8V; for fixed CLKs	30.0	50.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V; for fixed CLKs	-	-110.0	-65.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL} = 20 mA; for PCLKs & BCLKs	-	0.25	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH} = -70 mA; for PCLKs & BCLKs	2.4	4.0	-	V
Output Low Voltage[1]	V_{OL}	I_{OL} = 15mA; for fixed CLKs	-	0.2	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-50mA; for fixed CLKs	2.4	4.7	-	V
Supply Current[1]	I_{DD}	@ 66.5 MHz; all outputs unloaded	-	80.0	160.0	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

General Layout Precautions:

1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.

Notes:

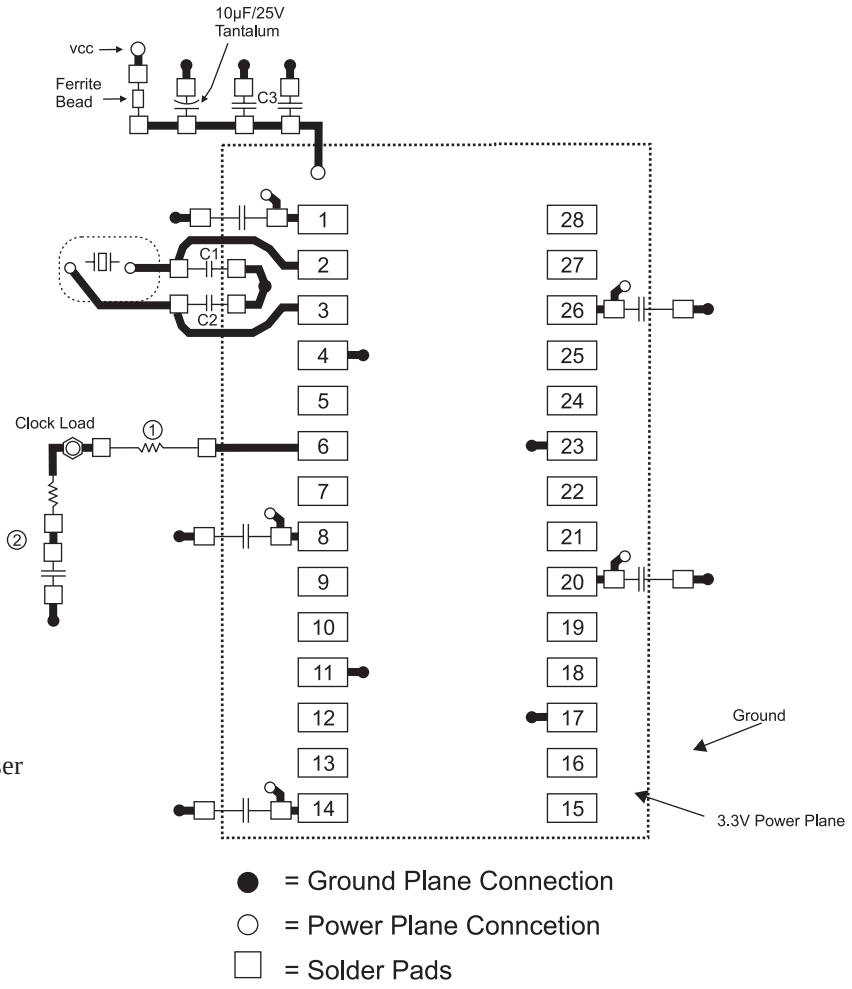
1) All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram.
2) 47 ohm / 56pf RC termination should be used at 50MHz and higher clock loads.
3) Optional crystal load capacitors are recommended.

Capacitor Values:

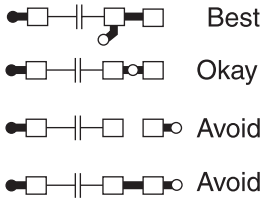
C1, C2 : Crystal load values determined by user

C3 : 100pF ceramic

All unmarked capacitors are 0.01µF ceramic



Connections to VDD:

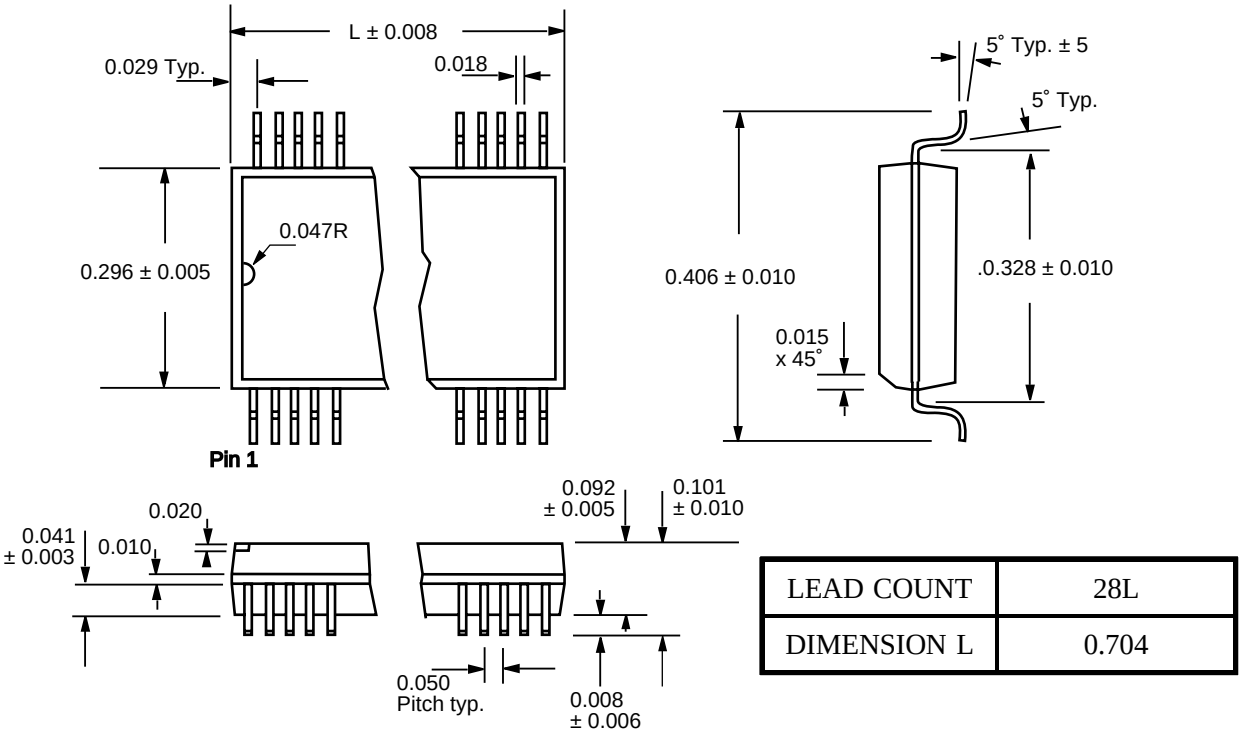


Electrical Characteristics at 5.0 V

V_{DD} = 4.5 - 5.5 V, T_A = 0 - 70 °C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V PCLK & BCLK	-	0.55	0.95	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V PCLK & BCLK	-	0.52	0.90	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80% PCLK & BCLK	-	1.2	2.1	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20% PCLK & BCLK	-	1.1	2.0	ns
Duty Cycle[1]	D_{t1}	20pF load @ VOUT = 50% of VDD	45	50	55	%
Duty Cycle[1]	D_{t2}	20pF load @ VOUT = 1.4 V	50	55	60	%
Jitter, One Sigma[1]	T_{j1s1}	PCLK & BCLK Clocks; Load=20pF; R=33 Ω FOUT > 25 MHz	-	50	150	ps
Jitter, Absolute[1]	T_{jab1}	PCLK & BCLK Clocks; Load=20pF; R=33 Ω FOUT > 25 MHz	-250	-	250	ps
Jitter, One Sigma[1]	T_{jis2}	Fixed CLK; Load=20pF R=33 Ω	-	1	3	%
Jitter, Absolute[1]	T_{jab2}	Fixed CLK; Load=20pF R=33 Ω	-5	2	5	%
Input Frequency[1]	F_i		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]	C_{INX}	X1, X2 pins	-	18	-	pF
Power-on Time[1]	t_{on}	From V=1.6V to 1st crossing of 66.5 MHz VDD supply ramp < 40 ms	-	2.5	4.5	ms
Frequency Settling Time[1]	t_s	From 1st crossing of acquisition to < 1% settling	-	2.0	4.0	ms
Clock Skew Window[1]	T_{sk1}	PCLK to PCLK; Load=20pF; @1.4V	-	150	250	ps
Clock Skew Window[1]	T_{sk2}	BCLK to BCLK; Load=20pF; @1.4V	-	300	500	ps
Clock Skew Window[1]	T_{sk3}	PCLK to BCLK; Load=20pF; @1.4V	1	2.6	5	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



LEAD COUNT	28L
DIMENSION L	0.704

SOIC Package

Ordering Information

ICS9169M-01

Example:

ICS XXXX M-PPP

Pattern Number (2 or 3-digit number for parts with ROM code pattern)

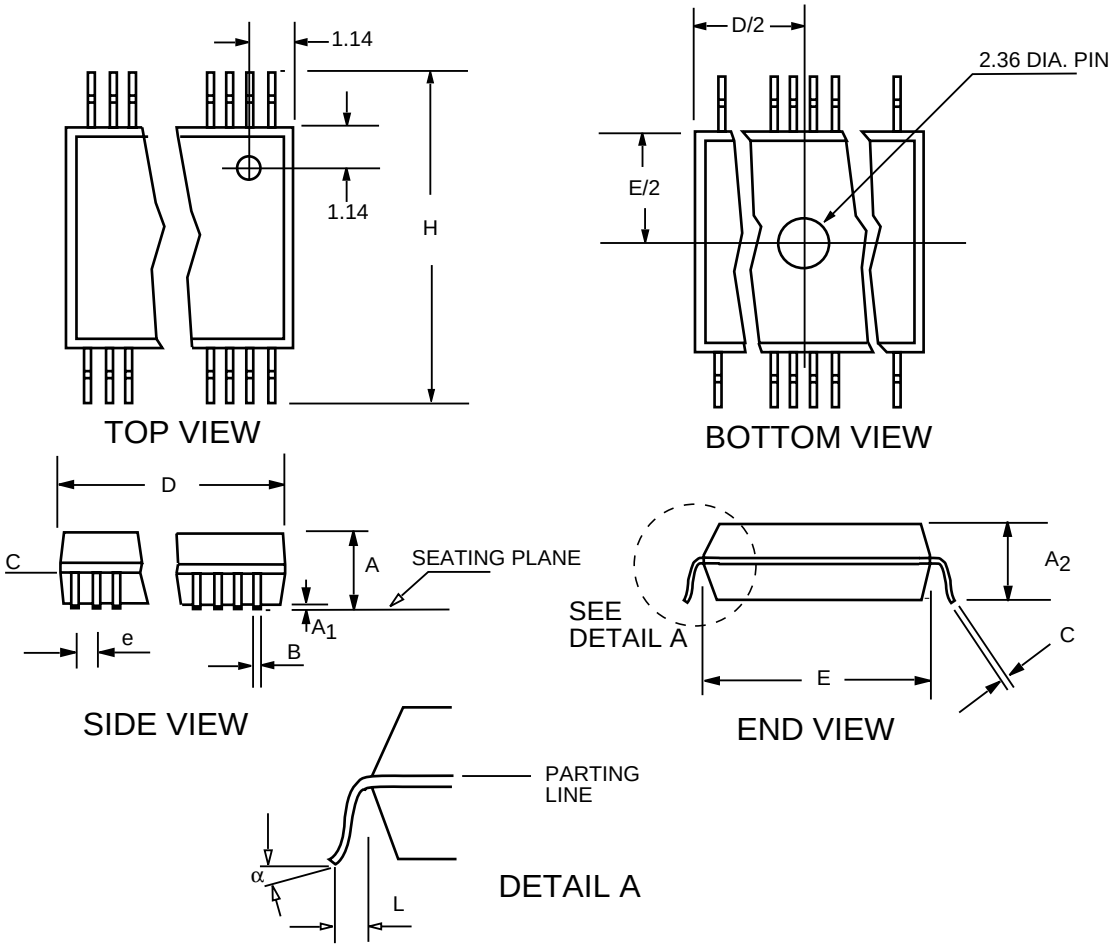
Package Type

M = SOIC

Device Type (consists of 3 or 4-digit numbers)

Prefix

ICS, AV=Standard Device



SSOP Package

Package dimensions - SSOP package

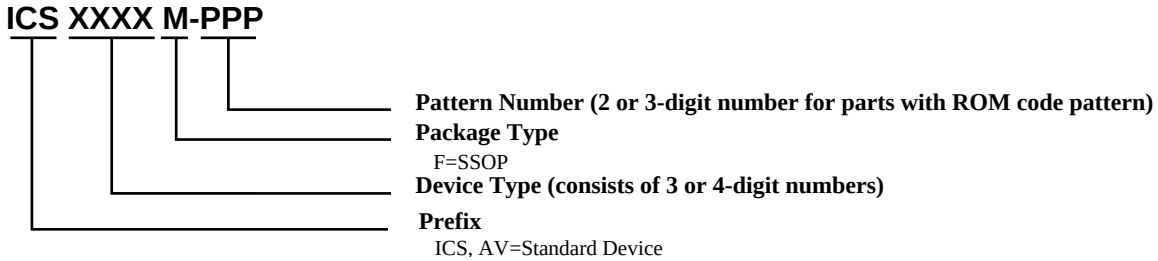
SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	VARIATIONS	4			6
							D			
	MIN.	NOM.	MAX.				MIN.	NOM.	MAX.	
A	0.68	0.73	0.78			AA	0.239	0.244	0.249	14
A	0.002	0.005	0.008			AB	0.239	0.244	0.249	16
A	0.066	0.068	0.070			AC	0.278	0.284	0.289	20
B	0.010	0.012	0.015			AD	0.318	0.323	0.328	24
C	0.005	0.006	0.008			AE	0.397	0.402	0.407	28
D	See Variations			4		AF	0.397	0.402	0.407	30
E	0.205	0.209	0.212	4						
e		0.0256 BSC								
H	0.301	0.307	0.311							
L	0.022	0.030	0.037	5						
N	See Variations			6						
	0	4	8							

Table dimensions in inches

Ordering Information

ICS9169F-01

Example:



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