

Description

The 8V97051L is a high-performance Wideband RF Synthesizer / PLL optimized for use as the local oscillator (LO) in Multi-Carrier, Multi-mode FDD, and TDD Base Station radio card. It is offered in a compact 5 × 5, 32-VFQFN package with 50Ω differential RF output impedances for ease of integration into the receiver or transmitter lineup.

The 8V97051L Wideband RF Synthesizer / PLL offers a default Fractional Mode with the option to use it with an Integer mode. It requires an external loop filter.

The 8V97051L with integrated Voltage Controlled Oscillator (VCO) supports output frequencies from 34.375MHz to 4400MHz, and maintains superior phase noise and spurious performance.

RF_OUT_[A:B] output drivers have independently programmable output power ranging from -4dBm to +7dBm. The RF_OUT outputs can be muted. The mute function is accessible via a SPI command or mute pin.

The operation of the 8V97051L is controlled by writing to registers through a three-wire SPI interface. The device also has an additional option that allows users to read back values from registers by configuring the MUX_OUT pin as a SDO for the SPI interface. The SPI interface is compatible with 1.8V logic and tolerant to 3.3V.

In multi-service base stations, very low noise oscillators are required to generate a large variety of frequencies to the mixers while maintaining excellent phase noise performance and low power. The 8V97051L offers a large tuning range capable of providing multi-band LO frequency synthesis in multi-mode base stations, thus limiting the use of multiple narrow band RF Synthesizers and reducing the BOM complexity and cost. The device can operate over -40°C to +85°C industrial temperature range.

Applications

- Wireless Infrastructure
- Test Equipment
- CATV Equipment
- Military and Aerospace
- Wireless LAN
- Clock Generation

Features

- Dual Differential Outputs
- Output frequency range: 34.375MHz to 4400MHz (continuous range)
- RF Output Divide by 1, 2, 4, 8, 16, 32, 64
- Open Drain Outputs (see [Output Distribution Section](#))
- Fractional-N synthesizer (also supports Integer-N mode)
- 16-bit integer and 12-bit fractional (16-bit fractional when using the extended registers)
- 3- or 4-wire SPI interface (compatible with 3.3V and 1.8V)
- Single 3.3V supply
- Logic compatibility: 1.8V
- Integrated high performance low dropout regulators (LDOs) for excellent power supply noise rejection
- Programmable output power level: -4dBm to +5dBm (up to +7 when using the extended registers)
- Mute Function
- Ultra low PN for 1.1GHz LO: -143dBc/Hz at 1MHz Offset, (typical)
- Lock Detect Indicators
- Input Reference frequency: 5MHz to 310MHz
- Power Consumption: 380mW (typical) (RF_OUT_B disabled)
- 32-Lead, 5x5 VFQFN package
- Automatic VCO band selection (Autocal feature)
- -40°C to +85°C ambient operating temperature
- Supports case temperature ≤ 105°C operations
- Lead-free (RoHS 6) packaging

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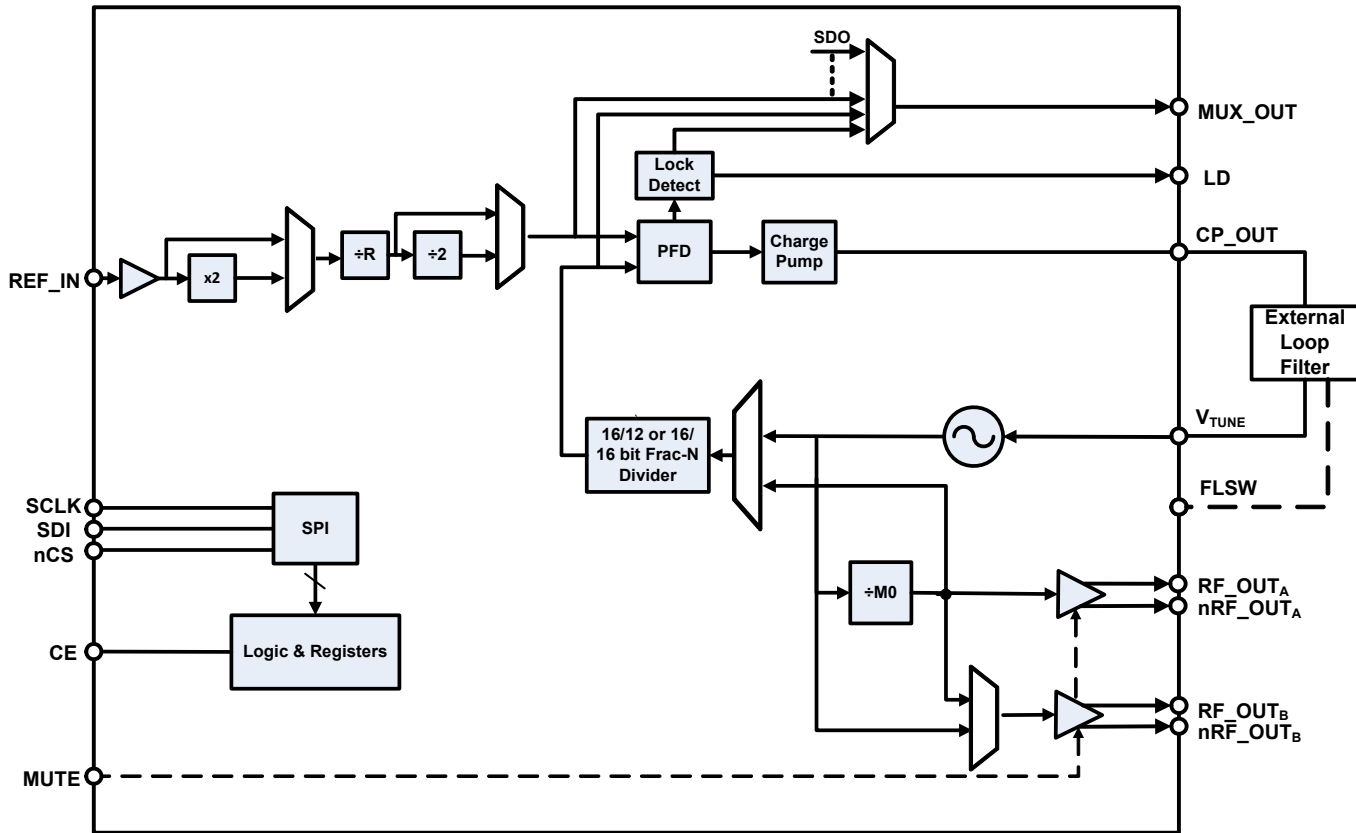
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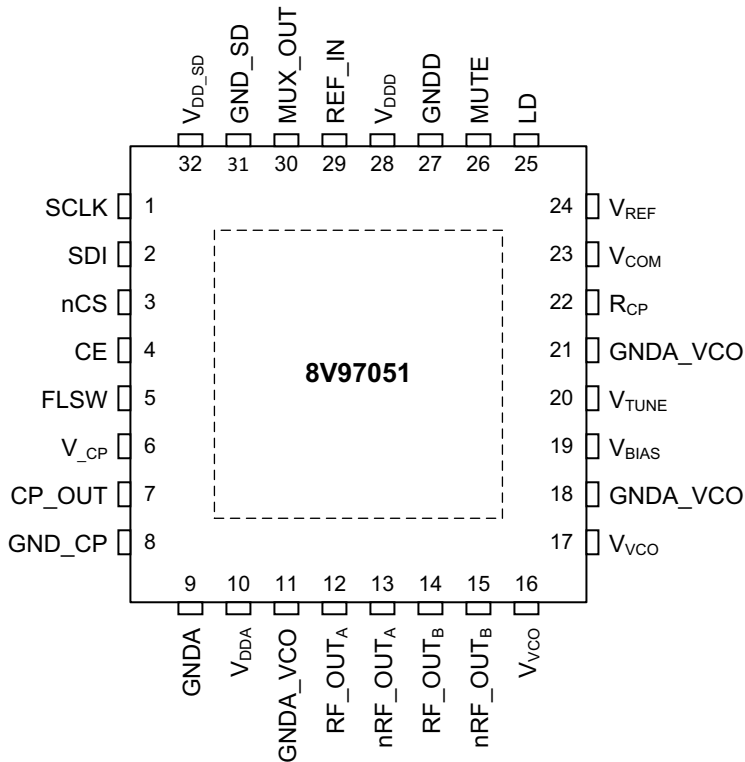
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8V97051L Block Diagram



NOTE: 16-Bit Integer / 16-Bit Fractional feedback divider is available when using extended register.

Pin Assignment



32-Lead 5mm x 5mm VFQFN

Pin Description and Characteristic Tables

Table 1. Pin Description¹

| Pin | Name | Type | | Description |
|-----|----------------------|----------------|----------|---|
| 1 | SCLK | LVC MOS Input | Pulldown | Serial Clock Input. High-Impedance CMOS input. 1.8V logic. 3.3V tolerant. |
| 2 | SDI | LVC MOS Input | Pullup | Serial Data Input. High-Impedance CMOS input. 1.8V logic. 3.3V tolerant. |
| 3 | nCS | LVC MOS Input | Pulldown | Load Enable. High-Impedance CMOS input. 1.8V logic. 3.3V tolerant. Active Low. |
| 4 | CE | LVC MOS Input | Pullup | Chip Enable. On logic Low, powers down the device and puts the charge pump into High-Impedance mode. Powers up the device on logic High. |
| 5 | FLSW | Analog | | Fast Lock Switch. A connection should be made from the loop filter to this pin when using the fast lock mode. |
| 6 | V _{CP} | Power | | Charge Pump Power Supply. V _{CP} must have the same value as V _{D DA} . Place decoupling capacitors to the ground plane as close to this pin as possible. |
| 7 | CP_OUT | Analog | | Charge Pump Output. When enabled, this output provides ±ICP to the external loop filter. The output of the loop filter is connected to V _{TUNE} to drive the internal VCO. |
| 8 | GND_CP | Ground | | Charge Pump Power Supply Ground. |
| 9 | GNDA | Ground | | Analog Power Supply Ground. |
| 10 | V _{D DA} | Power | | Analog Supply. This pin ranges from 3.3V ± 5%. V _{D DA} must have the same value as V _{D DD} . |
| 11 | GNDA_VCO | Ground | | VCO Analog Power Supply Ground. |
| 12 | RF_OUT _A | Output | | Clock Output pair A. The output level is programmable. |
| 13 | nRF_OUT _A | Output | | Clock Output pair A. The output level is programmable. |
| 14 | RF_OUT _B | Output | | Clock Output pair B. The output level is programmable. |
| 15 | nRF_OUT _B | Output | | Clock Output pair B. The output level is programmable. |
| 16 | V _{VCO} | Power | | VCO Supply. This pin ranges from 3.3V ± 5%. V _{VCO} must have the same value as V _{D DA} . |
| 17 | V _{VCO} | Power | | VCO Supply. This pin ranges from 3.3V ± 5%. V _{VCO} must have the same value as V _{D DA} . |
| 18 | GNDA_VCO | Ground | | VCO Analog Power Supply Ground. |
| 19 | V _{BIAS} | Analog | | Place decoupling capacitors (≥0.1μF) to ground, as close to this pin as possible. |
| 20 | V _{TUNE} | | | Control Input to tune the VCO. |
| 21 | GNDA_VCO | Ground | | VCO Analog Power Supply Ground. |
| 22 | R _{CP} | Analog | | Sets the charge pump current. Requires external resistor. |
| 23 | V _{COM} | Analog | | Place decoupling capacitors (≥0.1μF) to ground, as close to this pin as possible. |
| 24 | V _{REF} | Analog | | Place decoupling capacitors (≥0.1μF) to ground, as close to this pin as possible. |
| 25 | LD | LVC MOS Output | | Lock Detect. Logic High indicates PLL lock. Logic Low indicates loss of PLL lock. |
| 26 | MUTE | LVC MOS Input | Pullup | RF_OUT _A and RF_OUT _B Power-Down. A logic low on this pin mutes the RF_OUT outputs and puts them in High-Impedance. |

Table 1. Pin Description¹ (Continued)

| | | | | |
|----|--------------------|----------------|--------|---|
| 27 | GNDD | Ground | | Digital Power Supply Ground. |
| 28 | V _{DDD} | Power | | Digital Supply. V _{DDD} must have the same value as V _{DDA} . |
| 29 | REF_IN | LVC MOS Input | Analog | Reference Input. This CMOS input has a nominal threshold of V _{DDA} /2 and a DC equivalent input resistance of 100kΩ. This input can be driven from a TTL or CMOS crystal oscillator, or it can be AC-coupled. |
| 30 | MUX_OUT | LVC MOS Output | | Multiplexed Output and Serial Data Out. Refer to Table 4C, Page 14 . |
| 31 | GND_SD | Ground | | Digital Sigma Delta Modulator Power Supply Ground. |
| 32 | V _{DD_SD} | Power | | Digital Sigma Delta Modulator Supply. V _{DD_SD} must have the same value as V _{DDA} . |
| EP | Exposed Pad | Ground | | Must be connected to GND. |

NOTE 1. *Pullup* and *Pulldown* refer to internal input resistors. See [Table 2, Pin Characteristics](#), for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|--------------------------|-----------------|---------|---------|---------|-------|
| C _{in} | Input Capacitance | | | 4 | | pF |
| R _{OUT} | LVC MOS Output Impedance | MUX_OUT & LD | | 38 | | Ω |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

Table 3. Supply Pins and Associated Current Return Paths

| Power Supply Pin Number | Power Supply Pin Name | Associated Ground Pin Number | Associated Ground Pin Name |
|-------------------------|-----------------------|------------------------------|----------------------------|
| 10 | V _{DDA} | 9 | GNDA |
| 28 | V _{DDD} | 27 | GNDD |
| 32 | V _{DD_SD} | 31 | GND_SD |
| 16, 17 | V _{VCO} | 11, 18, 21 | GNDA_VCO |
| 6 | V _{_CP} | 8 | GND_CP |

Principles of Operation

Synthesizer Programming

The Fractional-N architecture is implemented via a cascaded programmable dual modulus prescaler. The N divider offers a division ratio in the feedback path of the PLL, and is given by programming the value of INT, FRAC and MOD in the following equation:

$$N = \text{INT} + \text{FRAC}/\text{MOD} \quad (1)$$

INT is the divide ratio of the binary 16-bits counter (refer to [Table 5B, Page 17](#)).

FRAC is the numerator value of the fractional divide ratio. It is programmable from 0 to (MOD – 1). Refer to [Table 5C](#) when in 12-bit mode, or [Table 12I](#) when in 16-bit mode.

MOD is the 12-bit or 16-bit modulus. It is programmable from 2 to 4095 in 12-bit mode, and 2 to 65535 in 16-bit mode. Refer to [Table 6D](#) when in 12-bit mode, or [Table 12H](#) when in 16-bit mode.

The **VCO** frequency (f_{VCO}) at RF_OUT_A or RF_OUT_B is given by the following equation:

$$f_{\text{VCO}} = f_{\text{PFD}} \times (\text{INT} + \text{FRAC}/\text{MOD}) \quad (2)$$

f_{PFD} is the frequency at the input of the Phase and Frequency Detector (PFD).

The 8V97051L offers an Integer mode. To enable that mode, the user has to program the FRAC value to 0.

The device's VCO features three VCO band-splits to cover the entire range with sufficient margin for process, voltage, and temperature variations. These are automatically selected by invoking the Autocal feature. The charge pump current is also programmable via the ICP SETTING register for maximum flexibility.

Via Register 4, one can enable RF_OUT_A or both outputs. Similarly, one can disable RF_OUT_B or both outputs.

Reference Input Stage

The 8V97051L features one single-ended reference clock input (REF_IN). This single-ended input can be driven by an ac-coupled sine wave or square wave.

In Power Down mode this input is set to High-Impedance to prevent loading of the reference source.

The reference input signal path also includes an optional doubler.

Reference Doubler

To improve the phase noise performance of the device, the reference doubler can be used. By using the doubler, the PFD frequency is also doubled and the phase noise performance typically improves by 3dB. When operating the device in Fractional mode, the speed of the Sigma Delta modulator of the N counter is limited to 125MHz, which is also the maximum PFD frequency that can be used in the fractional mode. When the part operates in Integer-N mode, the PFD frequency is limited to 310MHz.

The user has the possibility to select a higher PFD frequency (up to 310MHz in Integer mode) by doing the following steps using the extended registers (Register 6 and 7):

1. The user needs to increase the size of the Band Select Clock Divider (normally 8-bits) by setting the bit [D6:D3] in the Register 6 to divide down to a frequency lower than 500kHz and higher than 125kHz.
2. Use the Bit[D27:D26] to increase the lock detect precision for the faster PFD frequency.

The Lock Detect window should be set as large as possible but less than a period of the phase detector. The phase detector frequency should be greater than 500kHz.

Table 4A. Lock Detect Precision (LDP)

| LDP_Ext2 (D27 of Register 6) | LDP_Ext1 (D26 of Register 6) | LDP (D7 of Register 2) | LDP value (ns) |
|------------------------------------|------------------------------------|------------------------------|-------------------|
| 0 | 0 | 0 | 10 |
| 0 | 0 | 1 | 6 |
| Use of Extended Register 6 | | | |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 4.5 |
| 1 | 1 | 0 | 1.5 |
| 1 | 1 | 1 | 1.5 |

Feedback Divider

The feedback divider N supports fractional division capability in the PLL feedback path. It consists in an integer N divider of 16-bits, and a Fractional divider of 12-bits (FRAC) over 12-bits (MOD). FRAC and MOD can be extended to 16-bits when using extended registers.

To select an integer mode only, the user sets FRAC to 0.

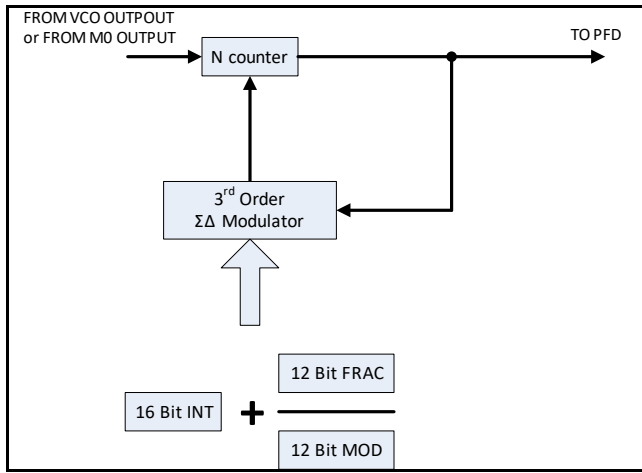


Figure 1. RF Feedback N Divider

The 16 INT bits (Bit[D30:D15] in Register 0) set the integer part of the feedback division ratio.

The 12 FRAC bits (Bit[D14:D3] in Register 0) set the numerator of the fraction that goes into the Sigma Delta modulator. FRAC can be extended to 16-bits using the EXT_FRAC bits in Register 7.

The 12 MOD bits (Bit[D14:D3] in Register 1) set the denominator of the fraction that goes into the Sigma Delta modulator. MOD can be extended to 16-bits using the EXT_MOD bits in Register 7.

From the relation (2), the VCO minimum step frequency is determined by $(1/MOD) * f_{PFD}$.

FRAC values from 0 to (MOD – 1) cover channels over a frequency range equal to the PFD reference frequency.

The PFD frequency is calculated as follows:

$$f_{PFD} = REF_{CLK} \frac{1+D}{R} \quad (3)$$

Use 2R instead of R if the Reference Divide by 2 is used.

- REF_{CLK}** = the input reference frequency (REF_IN)
- D** = the input reference doubler (0 if not active or 1 if active)
- R** = the 10-Bits programmable input reference pre-divider

The programmable modulus (MOD) is determined based on the input reference frequency (REF_IN) and the desired channelization (or output frequency resolution). The high resolution provided on the R counter and the Modulus allows the user to choose from several

configuration (by using the doubler or not) of the PLL to achieve the same channelization. Using the doubler may offer better phase noise performance. The high resolution Modulus also allows to use the same input reference frequency to achieve different channelization requirements. Using a unique PFD frequency for several needed channelization requirements allows the user to design a loop filter for the different needed setups and ensure the stability of the loop.

The channelization is given by $\frac{f_{PFD}}{MOD} \quad (4)$

In low noise mode (dither disabled), the Sigma Delta modulator can generate some fractional spurs that are due to the quantization noise.

The spurs are located at regular intervals equal to f_{PFD}/L where L is the repeat length of the code sequence in the Sigma Delta modulator. That repeat length depends on the MOD value, as described in [Table 4B](#).

Table 4B. Fractional Spurs Due to the Quantization Noise

| Condition (Dither Disabled) | L | Spur intervals |
|---------------------------------------|---------|---------------------------------|
| MOD can be divided by 2, but not by 3 | 2 x MOD | $f_{PFD}/(2*MOD)$ |
| MOD can be divided by 3, but not by 2 | 3 x MOD | $f_{PFD}/(3*MOD)$ |
| MOD can be divided by 6 | 6 x MOD | $f_{PFD}/(6*MOD)$ |
| Other conditions | MOD | f_{PFD}/MOD (channel step) |

In order to reduce the spurs, the user can enable the dither function to increase the repeat length of the code sequence in the Sigma Delta modulator. The increased repeat length is 2^{21} cycles so that the resulting quantization error is spread to appear like broadband noise. As a result, the in-band phase noise may be degraded when using the dither function.

When the application requires the lowest possible phase noise and when the loop bandwidth is low enough to filter most of the undesirable spurs, or if the spurs won't affect the system performance, it is recommended to use the low noise mode with dither disabled.

Phase and Frequency Detector (PFD) and Charge Pump

The phase detector compares the outputs from the R counter and from the N counter and generates an output corresponding to the phase and frequency difference between the two inputs the PFD. The charge pump current is programmable through the serial port (SPI) to several different levels.

The PFD offers an anti-backlash function that helps to avoid any dead zone in the PFD transfer function.

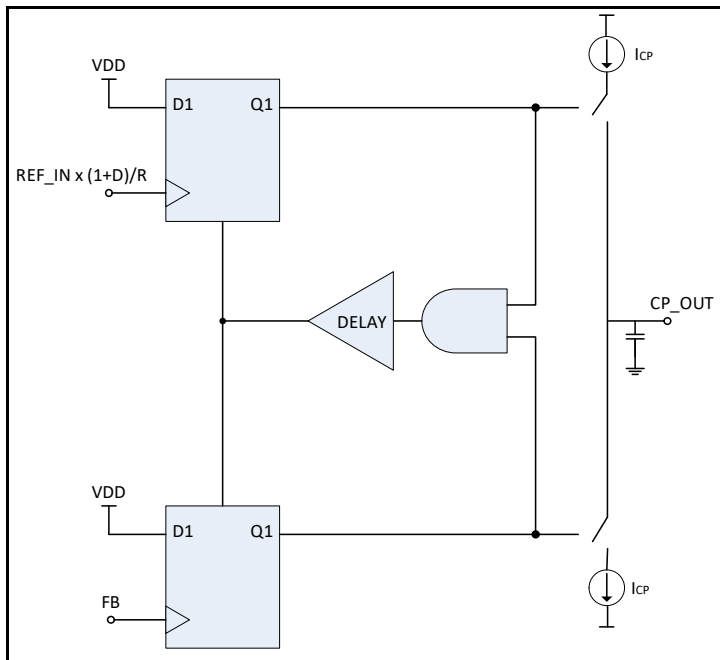


Figure 2. Simplified PFD Circuit using D-type Flip-flop

The Band Select logic operates between 125kHz and 500kHz. The Band Select clock divider needs to be set to divide down the PFD frequency to between 125kHz to 500kHz (logic maximum frequency).

PFD Frequency

The VCO Band Selection can be used while operating at PFD frequencies up to 310MHz.

If the application requires the PFD frequency to be higher than 125MHz, the user can use one of the following two techniques (Technique A is the recommended procedure):

A. The user can use the extended register ExtBndSelDiv[4:1] bits (Bits[D6:D3]) in Register 6. These additional band select divider bits extend the band select divider from 8-bits (available in Register 4) to 12-bits. The four additional band select divider bits

in Register 4 are the most significant bits of the divide value. For proper VCO band selection, the PFD frequency divided by the band select divide value must be $\leq 500\text{kHz}$ and $\geq 125\text{kHz}$.

B. If choosing this second technique, the user must follow the three following steps:

1. Disable the Phase Adjust function by setting the bit D28 In Register 1 to 0, keep the PFD frequency lower than 125MHz, and program the desired VCO frequency.
2. Enable the phase adjust function by setting BAND_SEL_DISABLE (Bit D28 in Register 1) to 1.
3. Set the desired PFD frequency and program the relevant R divider and N counter values.

In either technique, the Lock Detect Precision should be programmed to be lower than the PFD period using the bit [D7] in Register 2 and the bits [D27:D26] in Register 6 (Refer to [Table 4A, Page 9](#)).

External Loop Filter

The 8V97051L requires an external loop filter. The design of that filter is application specific. For additional information, refer to the [Applications Information](#) section.

Phase Detector Polarity

The phase detector polarity is set by bit D6 in Register 2. This bit should be set to 1 when using a passive loop filter or a non-inverting active loop filter. If an inverting active filter is used, this bit should be set to 0.

Charge Pump High-Impedance

In order to put the charge pump into three-state mode, the user must set the bit D4 [CP HIGHZ] in Register 2 to 1. This bit should be set to 0 for normal operation.

Integrated Low Noise VCO

The VCO function of the 8V97051L consists in three separate VCOs. This allows keeping narrow tuning ranges for the VCOs while offering a large frequency tuning range for VCO core. Keeping narrow VCO tuning ranges allows for lower VCO sensitivity (K_{VCO}), which results in the best possible VCO phase noise and spurious performance.

The user does not have to select the different VCO bands. The VCO band select logic of the 8V97051L will automatically select the most suitable band of operation at power up or when Register 0 is written.

For optimal performance, it is recommended to recalibrate the VCO by re-writing Register 0 when the temperature has varied more than 90°C from the temperature at which the previous calibration occurred.

Output Distribution Section

The 8V97051L device provides two outputs. These two outputs can generate the same frequency ($f_{VCO} / M0$) or two integer related different frequencies (in this case, RF_OUT_B would generate a frequency equal to the VCO frequency and RF_OUT_A would generate $f_{VCO} / M0$).

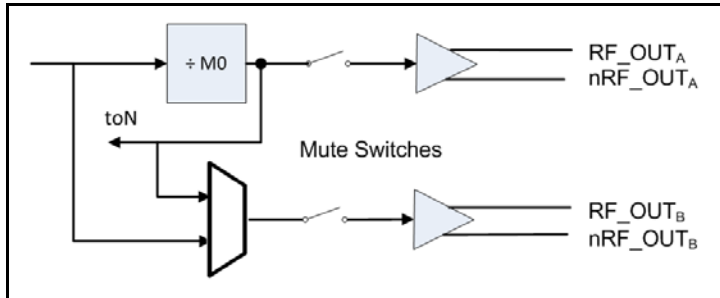


Figure 3. Output Clock Distribution

RF_OUT and nRF_OUT are derived from the drain of an NMOS differential pair driven by the VCO output (or by the M0 Divider), as shown in Figure 4, Output Stage.

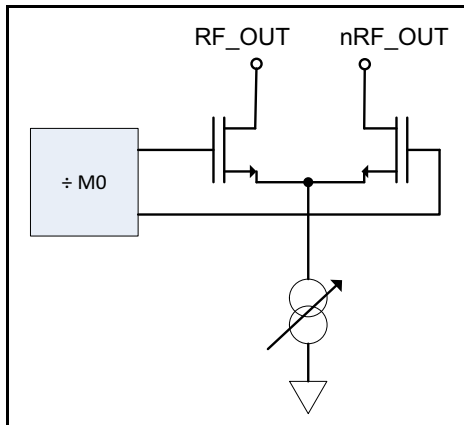


Figure 4. Output Stage

Eight programmable output power levels can be programmed from -4dBm to +7dBm (see RF Output Power section).

The 8V97051L offers an auxiliary output (RF_OUT_B). If the auxiliary output stage is not used, it can be powered down by using the RF_OutB_En bit in Register 4.

The supply current to the output stage can be shut down until the part achieves lock. To enable this mode, the user will set the MTLD bit in Register 4. The MUTE pin can be used to mute all outputs and be used as a similar function.

Output Matching

The outputs of the 8V97051L are Open Drain Output and can be matched in different ways.

A simple broadband matching is to terminate the open drain RF_OUT output with a 50Ω to V_{DDA}, and with an AC coupling capacitor in series. An example of this termination scheme is shown on Figure 5, Broadband Matching Termination.

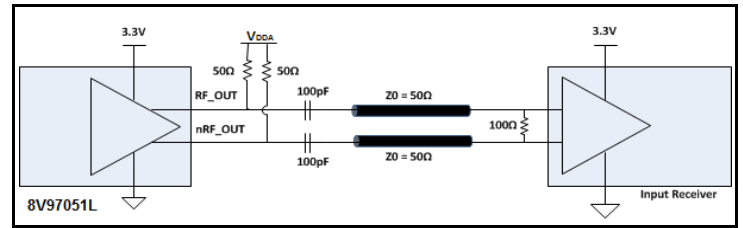


Figure 5. Broadband Matching Termination

This termination scheme allows to provide one of the selected output power on the differential pair when connected to a 50Ω load. (See the RF Output Power section for more information about the output power selection).

The 50Ω resistor connected to V_{DDA} can also be replaced by a choke, for better performance and optimal power transmission.

The pull up inductor value is frequency dependent. For impedance of 50Ω pull-up, the inductance value can be calculated as $L = 50 / (2 * 3.14 * F)$, where F is operating frequency. In this example, L = 3.9nH is for an operating frequency of approximately 2GHz.

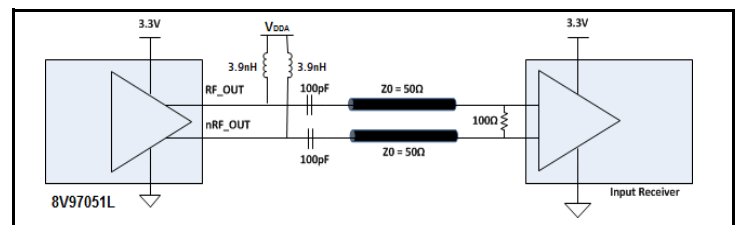


Figure 6. Optimal Matching Termination

See Applications Information section for more recommendations on the termination scheme.

Band Selection Disable

For a given frequency, the output phase can be adjusted when using the Band_Sel_Disable bit (Bit D28 in Register 1). When this bit is enabled (Bit D28 set to 1), the part does not do a VCO band selection or phase resync after an update to Register 0.

When the Band_Sel_Disable bit is set to 0, and when Register 0 is updated, the part proceeds to a VCO band selection, and to a phase resync if phase_resync is also enabled in Register 3 (Bits[D16:D15] set to D16 = 1 and D15 = 0).

The “Band_Sel_Disable” bit is useful when the user wants to make small changes in the output frequency (<1MHz from the nominal frequency) without recalibrating the VCO and minimizing the settling time.

Phase Adjust

The output phase is controlled by the 12-Bit phase value Bits[D26:D15] in Register 1. The output phase can vary over 360° with a 360°/MOD step. For dynamic adjustments of the phase after an initial phase setting, it is recommended to select the BAND_SEL_DISABLE function by setting the Band_Sel_Disable bit (D28 in Register 1) to 1.

The PHASE value can be extended to 16-bits when using the extended registers. In this 16 bit mode, both registers 1 and 7 define the PHASE value.

Phase Resync

The phase alignment function operates based on adjusting the “fractional” phase, so the phase can settle to any one of the MOD phase offsets, MOD being the modulus of the fractional feedback divider.

The phase adjustment can provide a 0-360° of phase adjust, assuming that the output divider ratio is set to 1.

The phase step is TVCO/MOD for the normal case of fundamental feedback. TVCO is the period of the VCO.

The feedback select bit (FbkSel bit, Bit D23 in Register 4) gives the choices of fundamental feedback or divided feedback. This bit controls the mux that sends the VCO signal or the output divider signal to the feedback loop. The user can get larger phase steps in the divided mode, but the phase noise may be degraded, especially in fractional mode. Should the user select this option, the phase adjustment step would be $\sim T_{OUT}/MOD$, where T_{OUT} is the output signal period.

When the part is in fractional mode, the device is dithering the feedback divider value. As an example, when using a 4GHz VCO frequency, the feedback divider value may dither between Div-by-20 and Div-by-21. Since the period is 250ps, there will be 250ps of jitter added to the phase detector. This jitter is filtered by the loop, but can still show up at the output if the loop bandwidth is high. When using a divider before the feedback divider, the effective VCO period is increased. If a Div-by-64 is used for example, the period becomes $64 \times 250ps = 16ns$. This means that there could be an additional 16ns of jitter at the PFD, rather than 250ps. It is more challenging for the loop to filter this larger amount of jitter and this will degrade the overall performance of the part, unless the user chooses to use a very low loop bandwidth. With normal loop bandwidth configurations (for optimal noise), the phase noise would be degraded when using a divided feedback mode.

The Phase Resync is controlled by setting Bits[D16:D15] in Register 3 to D16 = 1 and D15 = 0. When phase resync is used, an internal timer generates sync signals every T_{SYNC} where:

$$T_{SYNC} = ClkDiv \times MOD \times T_{PFD} \quad (5)$$

ClkDiv = the value (from 1 and 4095) programmed in the 12-bit clock counter in Bits[D14:D3] in Register 3. The 12-bit counter is used as a timer for Fast Lock and for the Phase Resync function.

MOD = the Modulus value (Bits[D14:D3] of Register 1)

T_{PFD} = the PFD period

In Equation 5, the minimum of either MOD value or 4095 is used for calculating T_{SYNC} when in 16-bit mode.

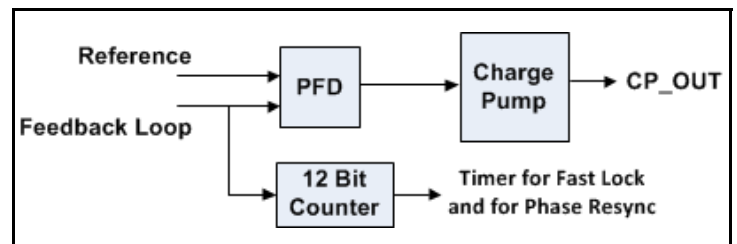


Figure 7. 12-bit Counter for Fast Lock and Phase Resync

After the user program a frequency, the second sync pulse coming from the 12-bit counter, after the nCS is asserted high, is used to resynchronize the output phase to the input phase. To ensure that the PLL is locked before to resynchronize the output phase, T_{SYNC} must be larger than the worst case lock time.

Fast Lock Function

The device uses a fast-lock mode to decrease lock time.

In order to allow the Fast Lock mode, the Fast Lock Switch (FLSW) is shorted to Ground and the charge pump current (ICP) is changed temporarily until the Fast Lock mode is disabled.

The loop bandwidth needs to be increased temporarily in order to allow a faster lock time. By doing this, the loop filter needs to be initially designed so that it addresses the risk of instability of having the zero and the poles too close to the actual bandwidth knee, when the user switches to a fast lock mode.

The loop bandwidth is proportional to:

$$RS \text{ and } ICP \text{ (} BW \sim RS * ICP \text{)}$$

Where:

BW = the loop bandwidth

RS = the damping resistor

ICP = the programmable charge pump current

In order to enable the fast lock mode, the charge pump current is increased to the maximum value in order to increase the loop bandwidth. In parallel, the FLSW filter is set to ON so that the RS value is $\frac{1}{4}$ of its initial value in order to maintain the loop stability. By doing so, the zero and the first pole are moved (by a factor of 4x in the example below), so that the zero and the pole are kept at a suitable distance around the loop bandwidth.

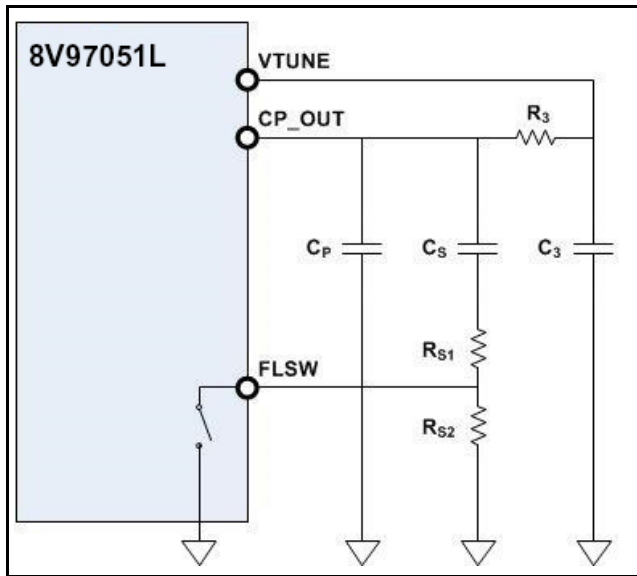


Figure 8. Example of Fast Lock Mode Loop Filter Topology

In the example of [Figure 8, Example of Fast Lock Mode Loop Filter Topology](#), the damping resistor RS is equal to: $RS1 + RS2$ in normal mode (FSLW switch OFF), with $RS2 = 3 * RS1$

When the FLSW switch is ON, the damping resistor value is reduced by $\frac{1}{4}$ of its initial value ($RS = RS1$).

The second pole defined by R3 and C3 need needs to be designed so that there is no risk of instability when widening the loop bandwidth.

RF Output Power

For RF_OUT_A and RF_OUT_B, the output power can be programmed from -4dBm to +7dBm.

Refer to [Table 9I, Page 26](#), [Table 9K, Table 11E, Page 30](#) and [Table 11F](#) in the [Register Map](#) section for more information.

MUX_OUT

MUX_OUT is a multipurpose output that can be programmed to provide the user with some internal status and values for test and debugging purpose. In addition, MUX_OUT can also be programmed to provide an additional Serial Data Out Pin for a 4-wire SPI interface when needed. The MUX_OUT function is described in the [Table 4C](#) and can be programmed in Bits[D28:D26] in Register 2.

Table 4C. MUX_OUT Pin Configuration

| MUX_OUT Register Value | MUX_OUT Function |
|------------------------|---------------------------|
| 000 | High-Impedance Output |
| 001 | V _{DDD} |
| 010 | GNDD |
| 011 | R Counter Output |
| 100 | N counter Output |
| 101 | Reserved |
| 110 | Lock Detect |
| 111 | MUX_OUT configured as SDO |

Power-Down Mode

When power-down is activated, the following events occur:

1. Counters are forced to their load state conditions
2. VCO is powered down
3. Charge pump is forced into three-state mode
4. Digital lock detect circuitry is reset
5. RF_OUT buffers are disabled
6. The input stage is powered down and set to High-Impedance
7. Input registers remain active and capable of loading and latching data

Default Power-Up Conditions

All the RF outputs are muted at power up until the loop is locked. Refer to the [Register Map](#) section for default values in registers.

Program Modes

[Table 4D](#) and the [Register Map](#) indicate how the program modes are set up in the 8V97051L.

Table 4D. Control Bits Configuration

| Control Bits (CB) | | | Register |
|-------------------|----|----|---------------------|
| C3 | C2 | C1 | |
| 0 | 0 | 0 | Register 0 |
| 0 | 0 | 1 | Register 1 |
| 0 | 1 | 0 | Register 2 |
| 0 | 1 | 1 | Register 3 |
| 1 | 0 | 0 | Register 4 |
| 1 | 0 | 1 | Register 5 |
| 1 | 1 | 0 | Extended Register 6 |
| 1 | 1 | 1 | Extended Register 7 |

Double Buffering

The following bits are Doubled Buffered:

1. **PHASE** (Bits[D26:D15] in Register 1)
2. **MOD** (Bits[D14:D3] in Register 1)
3. **REF DOUBLER** (Bit D25 in Register 2)
4. **REF DIV2** (Bit D24 in Register 2)
5. **R COUNTER** (Bits[D23:D14] in Register 2)
6. **ICP SETTING** (Bits[D12:D9] in Register 2)

The user must proceed to the following steps before any value written in these bits are used.

1. The new values are written in the double buffered bits
2. A new Write is performed on Register 0

The RF DIVIDER value in Register 4 (Bits[D22:D20]) is also double buffered, but only if the DOUBLE BUFFER bit (Bit D13 in Register 2) is set to 1.

Timing Characteristics

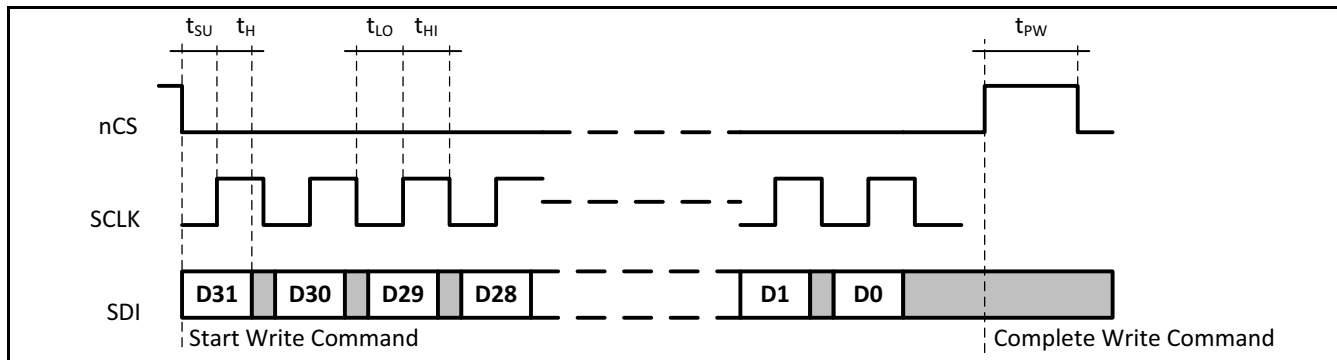


Figure 9. SPI Write Cycle Timing Diagram

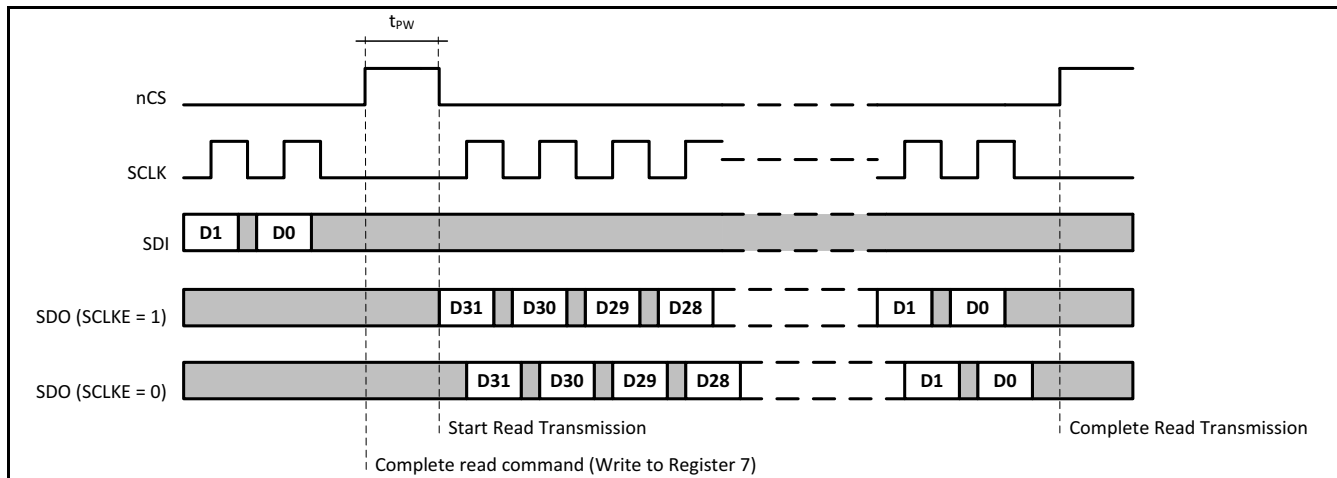


Figure 10. SPI Read Cycle Timing Diagram

Table 4E. SPI Read / Write Cycle Timing Parameters

| Symbol | Parameter | Minimum | Maximum | Unit |
|-----------|-----------------------------|---------|---------|------|
| f_{CLK} | SCLK Frequency | - | 20 | MHz |
| t_{SU} | nCS, SDI Setup Time to SCLK | 10 | - | ns |
| t_H | SCLK to nCS, SDI Hold Time | 10 | - | ns |
| t_{LO} | SCLK Low Pulse Width | 25 | - | ns |
| t_{HI} | SCLK High Pulse Width | 25 | - | ns |
| t_{PW} | nCS De-asserted Pulse Width | 20 | - | ns |

3- or 4-Wire SPI Interface Description

The 8V97051L has a serial control port capable of responding as a slave in an SPI compatible configuration to allow access to any of the internal registers (see [section, "Register Map" on page 17](#)) for device programming or examination of internal status. See the specific sections for each register for details on meanings and default conditions.

SPI mode slave operation requires that a device external to the 8V97051L has performed any necessary serial bus arbitration and/or address decoding at the level of the board or system. The 8V97051L begins a cycle by detecting an asserted (low) state on the nCS input at a rising edge of SCLK. This is also coincident with the first bit of data being shifted into the device. In SPI mode, the first bit is the Most Significant Bit (MSB) of the data word being written. Data must be written in 32-bit words, with nCS remaining asserted and one data bit being shifted in to the 8V97051L on every rising edge of SCLK. If nCS is de-asserted (high) at any time except after the complete 32nd SCLK cycle, this is treated as an error and the shift register contents are discarded. No data is written to any internal registers. If nCS is de-asserted (high) as expected at a time at least t_{SU} after the 32nd falling edge of SCLK, then this will result in the shift register contents being acted on according to the control bit in it.

It is recommended to write the registers in reverse sequential order, starting with the highest register number first and ending with Register 0.

The word format of the 32-bit quantity in the shift register is shown in [Table 4F](#). The register fields in the 8V97051L have been organized

so that the three LSBs in each 32-bit register row are not used for data transfer. These bits will represent the base address for the 32-bit register row.

To perform a register Read, the user needs set the MUX_OUT bits (Bits[28:D26]) in Register 2 to 111 to configure the MUX_OUT pin as SDO. Register 7 (Instruction register) needs to be set for Read operation. Bit D3 of Register 7 will set the Read or Write command, and Bits[D4:D6] determine the read back address.

If a read operation is requested, 32-bits of read data will be provided in the immediately subsequent access. nCS must be de-asserted (high) for at least t_{PW} , and then reasserted (low).

If SCLKE = 1 (default condition), one data bit will be transmitted on the SDO output at the falling edge of nCS and each falling edge of SCLK as long as nCS remains asserted (low), and the master device should capture data on the rising edge of SCLK. If SCLKE = 0, one data bit will be transmitted on the SDO output at each rising edge of SCLK as long as nCS remains asserted (low), and the master device should capture data on the falling edge of SCLK.

If nCS is de-asserted (high) before 32-bits of read data have been shifted out, the read cycle will be considered to be completed. If nCS remains asserted (low) longer than 32-bit times, then the data during those extra clock periods will be undefined. The MSB of the data will be presented first.

Table 4F. SPI Mode Serial Word Structure

| Bit # | MSB | | | | | | | LSB |
|---------|---------|-----|---|---|---|--------------|---|-----|
| | 31 | ... | 5 | 4 | 3 | 2 | 1 | 0 |
| Meaning | D[31:3] | | | | | Control Bits | | |
| Width | 29 | | | | | 3 | | |

Register Map

Register 0

Table 5A. Register 0 Bit Allocation

| BITS | D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|--------------------------------------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--|--------|--------|-------|-------|-------|--------------|-------|-------|-------|-------|-------|-----|-----|-----|
| NAME | RESERVED | NDiv16 | NDiv15 | NDiv14 | NDiv13 | NDiv12 | NDiv11 | NDiv10 | NDiv9 | NDiv8 | NDiv7 | NDiv6 | NDiv5 | NDiv4 | NDiv3 | NDiv2 | NDiv1 | FDiv12 | FDiv11 | FDiv10 | FDiv9 | FDiv8 | FDiv7 | FDiv6 | FDiv5 | FDiv4 | FDiv3 | FDiv2 | FDiv1 | CB3 | CB2 | CB1 |
| DESCRIPTION | RESERVED | FEEDBACK DIVIDER INTEGER VALUE (INT) | | | | | | | | | | | | | | | | FEEDBACK DIVIDER FRACTIONAL VALUE (FRAC) | | | | | | CONTROL BITS | | | | | | | | |

Table 5B. Register 0: 16-Bit Feedback Divider Integer Value (INT). Function Description

| Name | Description | Factory Default | Function |
|------------|--------------------------------------|------------------------------------|---|
| NDiv[16:1] | Feedback Divider Integer Value (INT) | 0000 0000 0110 0100 (INT = 100) | 0000 0000 0000 0000 = Not allowed 0000 0000 0000 0001 = Not allowed ... 0000 0000 0000 0111 = Not allowed 0000 0000 0000 1000 = 8 ... 0000 0000 0001 0111 = 23 0000 0000 0001 1000 = 24 ... 1111 1111 1111 1111 = 65,535 |

Table 5C. Register 0: 12-Bit Feedback Divider Fractional Value (FRAC). Function Description¹

| Name | Description | Factory Default | Function |
|------------|--|------------------------------|--|
| FDiv[12:1] | Feedback Divider Fractional Value (FRAC) | 0000 0000 0000 (FRAC = 0) | 0000 0000 0000 = 0 0000 0000 0001 = 1 ... 1111 1111 1111 = 4095 |

NOTE 1. This table is used when bit 16b_12b_sel is set to 0 (default). If the 16b_12b_sel is set to 1, refer to [Table 12I, Page 35](#).

Table 5D. Register 0: 3-Bit Control Bits. Function Description¹

| Name | Description | Function |
|---------|--------------|--------------------------------|
| CB[3:1] | Control Bits | 000 = Register 0 is programmed |

NOTE 1. The user has to set CB[3:1] to 000 in order to write to Register 0.

Register 1

Table 6A. Register 1 Bit Allocation

| BITS | D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|------------------|--------|---------------------|---------|---------|--------|--------|--------|--------|--------|--------|--------|--------|---------------------|-------|-------|-------|------|------|------|------|------|------|------|--------------|------|-----|-----|-----|
| NAME | Reserved | Reserved | Reserved | Band_Sel_Disable | Unused | Phase12 | Phase11 | Phase10 | Phase9 | Phase8 | Phase7 | Phase6 | Phase5 | Phase4 | Phase3 | Phase2 | Phase1 | Mod12 | Mod11 | Mod10 | Mod9 | Mod8 | Mod7 | Mod6 | Mod5 | Mod4 | Mod3 | Mod2 | Mod1 | CB3 | CB2 | CB1 |
| DESCRIPTION | RESERVED | | | BAND_SEL_DISABLE | UNUSED | PHASE VALUE (PHASE) | | | | | | | | | | | MODULUS VALUE (MOD) | | | | | | | | | | | CONTROL BITS | | | | |

Table 6B. Register 1: 1-Bit BAND_SEL_DISABLE. Function Description

| Name | Description | Factory Default | Function |
|------------------|------------------|-----------------|---|
| Band_Sel_Disable | BAND_SEL_DISABLE | 0 | 0 = VCO Band Selection occurs after a Write to Register 0 1 = VCO Band selection is not active and hold to previous VCO band selection |

Table 6C. Register 1: 12-Bit Phase Value (PHASE). Function Description

| Name | Description | 16b_12b_sel (Bit D20, Register7) | Factory Default | Function |
|--------------|-------------|-------------------------------------|-----------------|------------------------|
| Phase [12:1] | PHASE | 0 | 0000 0000 0001 | 0000 0000 0000 = 0 |
| | | | | 0000 0000 0001 = 1 |
| | | | | ... |
| | | | | 1111 1111 1111 = 4095 |
| | | 1 | 0000 0000 0001 | 0000 0000 0000 = 0 |
| | | | | 0000 0000 0001 = 16 |
| | | | | ... |
| | | | | 1111 1111 1111 = 65520 |

Table 6D. Register 1: 12-Bit Modulus Value (MOD). Function Description¹

| Name | Description | Factory Default | Function |
|-----------|-------------|-----------------|--|
| Mod[12:1] | MOD | 0000 0000 0010 | 0000 0000 0000 = Not Allowed 0000 0000 0001 = Not Allowed 0000 0000 0010 = 2 ... 1111 1111 1111 = 4095 |

NOTE 1. This table is used when bit D20 in Register 7 (16b_12B_sel) is set to 0 (default). If 16b_12b_sel is set to 1, refer to [Table 12H, Page 34](#).

Table 6E. Register 1: 3-Bit Control Bits. Function Description¹

| Name | Description | Function |
|---------|--------------|--------------------------------|
| CB[3:1] | Control Bits | 001 = Register 1 is programmed |

NOTE 1. The user has to set CB[3:1] to 001 in order to write to Register 1.

5HJLVWHU

7DEOH \$ 5HJLVWHU %LW \$OORFDWLRQ

| | | |
|---------------|------------|-----------|
| '(6&5,37,21 | 1 \$0(| % ,76 |
| 5(6(59(' | 5(6(59(' | - |
| 12,6(02'(' | ORGH1RLVH | ORGH1RLVH |
| 08;B287 | 08;B287 | - |
| 08;B287 | 08;B287 | - |
| 5() '28%/(5 | 5HI'RXE | - |
| 5() '9 | 5'LY | - |
| 5 & 2817(5 | 5 | - |
| | 5 | - |
| | 5 | - |
| | 5 | - |
| | 5 | - |
| | 5 | - |
| | 5 | - |
| | 5 | - |
| | 5 | - |
| '28%/(%8))(5 | 'RXE%XII | - |
| | &KUJ3PS | - |
| | &KUJ3PS | - |
| | &KUJ3PS | - |
| | &KUJ3PS | - |
| | (') | - |
| | '3 | - |
| 3' 32/\$5,7< | 3'BSRO | - |
| 32:(5 '2:1 | 3ZU'ZQ | - |
| &3 +, * += | &3B+, * += | - |
| 8186(' | 8QXVHG | - |
| & 21752/ | &% | - |
| % ,76 | &% | - |
| | &% | - |

7DEOH % 5HJLVWHU(02'(%LW)XQF2WLRQ 'HVFULSWLRQ

| | | | |
|------------|---------------|-----------------|--|
| 1DPH | 'HVFULSWLRQ |)DFWRU\ 'HIDXOW |)XQFWLRQ |
| ORGH1RLVH> | @ 12,6(02'(' | | /RZ 1RLVGH0 'LWKHU 2)) 5HVHUYHG 5HVHUYHG /RZ 6SXGH0RLWKHU (QDEOHG |

7DEOH & 5HJLVWHU(B287 %LW)XQFWLRQ 'HVFULSWLRQ

| | | | |
|----------|-------------|-----------------|--|
| 1DPH | 'HVFULSWLRQ |)DFWRU\ 'HIDXOW |)XQFWLRQ |
| 08;B287> | @ | 08;B287 | +LJK ,PSHGDQFH RXWS 9, *1'' 5 FRXQWHU RXWSXW 1 FRXQWHU RXWSXW 5HVHUYHG /RFN 'HWHFW 08;B287 FRQILJXUHG D |

7DEOH ' 5HJLVWHU('28%(%5W)XQFWLRQ 'HVFULSWLRQ

| | | | |
|---------|-------------|-----------------|---------------------|
| 1DPH | 'HVFULSWLRQ |)DFWRU\ 'HIDXOW |)XQFWLRQ |
| 5HI'RXE | 5() '28%/(5 | | 'LVDEOHG (QDEOHG |

Table 7E. Register 2: 1-Bit REF DIV2. Function Description

| Name | Description | Factory Default | Function |
|-------|-------------|-----------------|-----------------------------|
| RDIV2 | REF DIV2 | 0 | 0 = Disabled 1 = Enabled |

Table 7F. Register 2: 10-Bit R COUNTER (R). Function Description

| Name | Description | Factory Default | Function |
|---------|-------------|-----------------|--|
| R[10:1] | R | 00 0000 0001 | 00 0000 0000 = Not Allowed 00 0000 0001 = 1 00 0000 0010 = 2 ... 11 1111 1111 = 1023 |

Table 7G. Register 2: 1-Bit DOUBLE BUFFER. Function Description¹

| Name | Description | Factory Default | Function |
|-----------|---------------|-----------------|-----------------------------|
| DoubBuff1 | DOUBLE BUFFER | 0 | 0 = Disabled 1 = Enabled |

NOTE 1. Bit D13 enables or disables Double Buffering of Bits[D22:D20] in Register 4. Refer to [Program Modes](#) section.

Table 7H. Register 2: 4-Bit Charge Pump Setting (ICP SETTING). Function Description

| Name | Description | Factory Default | Function |
|--------------|-------------|-----------------|---|
| ChrgPmp[4:1] | ICP SETTING | 0000 | Icp (mA) assuming RCP = 5.1kΩ 0000 = 0.31 0001 = 0.63 0010 = 0.94 0011 = 1.25 0100 = 1.56 0101 = 1.88 0110 = 2.19 0111 = 2.50 1000 = 2.81 1001 = 3.13 1010 = 3.44 1011 = 3.75 1100 = 4.06 1101 = 4.38 1110 = 4.69 1111 = 5.00 |

Table 7I. Register 2: 1-Bit Lock Detect Function (LDF). Function Description¹

| Name | Description | Factory Default | Function |
|------|-------------|-----------------|--|
| LDF | LDF | 0 | 0 = 40 consecutive cycles (recommended for FRAC-N mode) 1 = 5 consecutive cycles (recommended for INT-N mode) |

NOTE 1. LDF controls the number of PFD cycles that needs to be considered by the Lock Detect function to decide if the part has achieved lock.

Table 7J. Register 2: 1-Bit Lock Detect Precision. Function Description

| Name | Description | Factory Default | Function |
|------|-------------|-----------------|---------------------|
| LDP | LDP | 0 | 0 = 10ns 1 = 6ns |

Table 7K. Register 2: 1-Bit Phase Detector Polarity. Function Description

| Name | Description | Factory Default | Function |
|--------|-------------|-----------------|------------------------------|
| PD_Pol | PD POLARITY | 1 | 0 = NEGATIVE 1 = POSITIVE |

Table 7L. Register 2: 1-Bit Power Down. Function Description

| Name | Description | Factory Default | Function |
|--------|-------------|-----------------|-----------------------------|
| PwrDwn | POWER DOWN | 0 | 0 = Disabled 1 = Enabled |

Table 7M. Register 2: 1-Bit Charge Pump High-Impedance. Function Description

| Name | Description | Factory Default | Function |
|----------|-------------|-----------------|-----------------------------|
| CP_HIGHZ | CP HIGHZ | 0 | 0 = Disabled 1 = Enabled |

Table 7N. Register 2: 3-Bit Control Bits. Function Description¹

| Name | Description | Function |
|---------|--------------|--------------------------------|
| CB[3:1] | Control Bits | 010 = Register 2 is programmed |

NOTE 1. The user has to set CB[3:1] to 010 in order to write to Register 2.

Register 3

Table 8A. Register 3 Bit Allocation

| | BITS | NAME | DESCRIPTION | |
|--|------|-------------|--------------|--------------|
| | D31 | RESERVED | RESERVED | |
| | D30 | RESERVED | | |
| | D29 | RESERVED | | |
| | D28 | RESERVED | | |
| | D27 | RESERVED | | |
| | D26 | RESERVED | | |
| | D25 | RESERVED | | |
| | D24 | RESERVED | | |
| | D23 | BandSelCM | | |
| | D22 | Unused | | |
| | D21 | Unused | UNUSED | |
| | D20 | RESERVED | | |
| | D19 | RESERVED | RESERVED | |
| | D18 | Unused | | |
| | D17 | RESERVED | UNUSED | |
| | D16 | ClkDivMode2 | | |
| | D15 | ClkDivMode1 | CLK DIV MODE | |
| | D14 | ClkDiv12 | | |
| | D13 | ClkDiv11 | | |
| | D12 | ClkDiv10 | | |
| | D11 | ClkDiv9 | | |
| | D10 | ClkDiv8 | | |
| | D9 | ClkDiv7 | | |
| | D8 | ClkDiv6 | | |
| | D7 | ClkDiv5 | | |
| | D6 | ClkDiv4 | | |
| | D5 | ClkDiv3 | | |
| | D4 | ClkDiv2 | | |
| | D3 | ClkDiv1 | | |
| | D2 | CB3 | | CONTROL BITS |
| | D1 | CB2 | | |
| | D0 | CB1 | | |

Table 8B. Register 3: 1-Bit Band Select Clock Mode. Function Description¹

| Name | Description | Factory Default | Function |
|-----------|--------------------------|-----------------|---|
| BandSelCM | BAND SELECT (CLOCK RATE) | 0 | 0 = LOW (125kHz) 1 = HIGH (up to 500kHz logic sequence for Faster Lock applications) |

NOTE 1. BAND SELECT (CLOCK RATE) selects the speed of the logic sequence for the band selection. BandSelCM = 1 sets the logic sequence rate faster, which is recommended for fast lock operation and when high PFD frequencies are used. BandSelCM = 0 is recommended when low PFD frequencies (125kHz) are used. When using BandSelCM = 1, the value of the BAND SELECT CLOCK COUNTER (BndSelDiv[8:1]) must be less than or equal to 254.

Table 8C. Register 3: 2-Bit Clock Divider Mode. Function Description

| Name | Description | Factory Default | Function |
|-----------------|--------------|-----------------|--|
| ClkDivMode[2:1] | CLK DIV MODE | 00 | 00 = Clock Divider OFF 01 = Fast Lock Enabled 10 = Resync Enabled 11 = Reserved |

Table 8D. Register 3: 12-Bit Clock Divider Value (CLKDIV). Function Description

| Name | Description | Factory Default | Function |
|--------------|-------------|-----------------|--|
| ClkDiv[12:1] | CLKDIV | 0000 0000 0001 | 0000 0000 0000 = Not allowed 0000 0000 0001 = 1 0000 0000 0010 = 2 ... 1111 1111 1111 = 4095 |

Table 8E. Register 3: 3-Bit Control Bits. Function Description¹

| Name | Description | Function |
|---------|--------------|--------------------------------|
| CB[3:1] | CONTROL BITS | 011 = Register 3 is programmed |

NOTE 1. The user has to set CB[3:1] to 011 in order to write to Register 3.

Register 4
Table 9A. Register 4 Bit Allocation

| BITS | NAME | DESCRIPTION | |
|------|-------------|----------------------|---------------------------|
| D31 | RESERVED | RESERVED | |
| D30 | RESERVED | | |
| D29 | RESERVED | | |
| D28 | RESERVED | | |
| D27 | RESERVED | | |
| D26 | RESERVED | | |
| D25 | RESERVED | | |
| D24 | RESERVED | | |
| D23 | FbkSel | | FEEDBACK SELECT |
| D22 | RFDiv3 | | RF DIVIDER |
| D21 | RFDiv2 | | |
| D20 | RFDiv1 | | |
| D19 | BndSelDiv8 | | BAND SELECT CLOCK COUNTER |
| D18 | BndSelDiv7 | | |
| D17 | BndSelDiv6 | | |
| D16 | BndSelDiv5 | | |
| D15 | BndSelDiv4 | | |
| D14 | BndSelDiv3 | | |
| D13 | BndSelDiv2 | | |
| D12 | BndSelDiv1 | | |
| D11 | VCOPwrDwn | VCO POWER DOWN | |
| D10 | MTLD | MTLD | |
| D9 | RF_OUTB_Sel | RF_OUTB SELECT | |
| D8 | RF_OUTB_En | RF_OUTB ENABLE | |
| D7 | RF_OUTB_Pwr | RF_OUTB OUTPUT POWER | |
| D6 | RF_OUTB_Pwr | | |
| D5 | RF_OutA_En | RF_OUTA ENABLE | |
| D4 | RF_OUTA_Pwr | RF_OUTA OUTPUT POWER | |
| D3 | RF_OUTA_Pwr | | |
| D2 | CB3 | CONTROL BITS | |
| D1 | CB2 | | |
| D0 | CB1 | | |

Table 9B. Register 4: 1-Bit Feedback Select. Function Description

| Name | Description | Factory Default | Function |
|--------|-----------------|-----------------|--------------------------------|
| FbkSel | FEEDBACK SELECT | 1 | 0 = Divided 1 = Fundamental |

Table 9C. Register 4: 3-Bit RF Output Divider (÷ MO) Select. Function Description

| Name | Description | Factory Default | Function |
|------------|-------------------|-----------------|---|
| RFDiv[3:1] | RF OUTPUT DIVIDER | 000 | 000 = Div by 1 001 = Div by 2 010 = Div by 4 011 = Div by 8 100 = Div by 16 101 = Div by 32 110 = Div by 64 111 = Reserved |

Table 9D. Register 4: 8-Bit Band Select Clock Counter. Function Description¹

| Name | Description | Factory Default | Function |
|----------------|---------------------------|-----------------|---|
| BndSelDiv[8:1] | BAND SELECT CLOCK COUNTER | 0000 0001 | 0000 0000 = Not Allowed 0000 0001 = 1 0000 0010 = 2 ... 1111 1111 = 255 |

NOTE 1. BAND SELECT CLOCK COUNTER sets the value of the divider for the band select logic clock input. By default, the output frequency of the R counter is used to clock the band select logic. If this frequency is larger than 125kHz, the Band Select Clock counter can be used to divide the R counter output to a smaller frequency suitable for the band selection logic.

Table 9E. Register 4: 1-Bit VCO Power Down. Function Description

| Name | Description | Factory Default | Function |
|-----------|----------------|-----------------|--|
| VCOPwrDwn | VCO POWER DOWN | 0 | 0 = VCO Powered Up 1 = VCO Powered Down |

Table 9F. Register 4: 1-Bit Mute Till Lock Detect. Function Description

| Name | Description | Factory Default | Function |
|------|-------------|-----------------|---------------------------------------|
| MTLD | MTLD | 0 | 0 = Mute Disabled 1 = Mute Enabled |

Table 9G. Register 4: 1-Bit RF_OUTB Select. Function Description

| Name | Description | Factory Default | Function |
|-------------|----------------|-----------------|---------------------------------------|
| RF_OUTB_Sel | RF_OUTB SELECT | 0 | 0 = Divided Output 1 = Fundamental |

Table 9H. Register 4: 1-Bit RF_OUTB Enable. Function Description

| Name | Description | Factory Default | Function |
|------------|----------------|-----------------|---|
| RF_OUTB_En | RF_OUTB ENABLE | 0 | 0 = Disabled (High-Impedance) 1 = Enabled ¹ |

NOTE 1. RF_OUT_A must also be enabled.

Table 9I. Register 4: 2-Bit RF_OUTB Output Power. Function Description¹

| Name | Description | Factory Default | Function |
|------------------|----------------------|-----------------|--|
| RF_OUTB_Pwr[2:1] | RF_OUTB OUTPUT POWER | 10 | 00 = -4dBm 01 = -1dBm 10 = +2dBm 11 = +5dBm |

NOTE 1. $f_{RF_OUT} = 34.375\text{MHz}$.

Table 9J. Register 4: 1-Bit RF_OUTA Enable. Function Description

| Name | Description | Factory Default | Function |
|------------|----------------|-----------------|---|
| RF_OUTA_En | RF_OUTA ENABLE | 0 | 0 = Disabled ¹ (High-Impedance) 1 = Enabled |

NOTE 1. RF_OUT_B will also disable.

Table 9K. Register 4: 2-Bit RF_OUTA Output Power. Function Description¹

| Name | Description | Factory Default | Function |
|------------------|----------------------|-----------------|--|
| RF_OUTA_Pwr[2:1] | RF_OUTA OUTPUT POWER | 10 | 00 = -4dBm 01 = -1dBm 10 = +2dBm 11 = +5dBm |

NOTE 1. $f_{RF_OUT} = 34.375\text{MHz}$.

Table 9L. Register 4: 3-Bit Control Bits. Function Description¹

| Name | Description | Function |
|---------|--------------|--------------------------------|
| CB[3:1] | CONTROL BITS | 100 = Register 4 is programmed |

NOTE 1. The user has to set CB[3:1] to 100 in order to write to Register 4.

Register 5
Table 10A. Register 5 Bit Allocation¹

| BITS | D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|----------|----------|----------|----------|-------------|------------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|--------------|----------|----------|----------|----------|----------|----------|
| NAME | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | LDPInMode2 | LDPInMode1 | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| DESCRIPTION | RESERVED | | | | | | | | LD PIN MODE | | RESERVED | | | | | | | | | | | | | | | CONTROL BITS | | | | | | |

NOTE 1. D19 and D20 must be set to 1.

Table 10B. Register 5: 2-Bit LD (Lock Detect) Pin Mode. Function Description

| Name | Description | Factory Default | Function |
|----------------|-------------|-----------------|---|
| LDPInMode[2:1] | LD PIN MODE | 01 | 00 = Low 01 = Digital Lock Detect 10 = Low 11 = High |

Table 10C. Register 5: 3-Bit Control Bits. Function Description¹

| Name | Description | Function |
|---------|--------------|--------------------------------|
| CB[3:1] | CONTROL BITS | 101 = Register 5 is programmed |

NOTE 1. The user has to set CB[3:1] to 101 in order to write to Register 5.

Extended Registers, (Registers 6 and 7)
Register 6
Table 11A. Register 6 Bit Allocation^{1 2 3}

| BITS | NAME | DESCRIPTION |
|------|------------------|-----------------------|
| D31 | DigLock | DIGITAL LOCK (RO) |
| D30 | Band_select_done | BAND_SELECT_DONE (RO) |
| D29 | Reserved | RESERVED (RO) |
| D28 | Reserved | RESERVED (RO) |
| D27 | LDP_Ext2 | LDP_EXT |
| D26 | LDP_Ext1 | |
| D25 | rfoutb_hi_pwr | RF_OUTB_HI_PWR |
| D24 | rfouta_hi_pwr | RF_OUTA_HI_PWR |
| D23 | SDMOrder2 | SDM_ORDER |
| D22 | SDMOrder1 | |
| D21 | DitherG | DITHER GAIN |
| D20 | ShapeDitherEn | SHAPE_DITHER_EN |
| D19 | SDMType1 | SDM_TYPE |
| D18 | SDMType0 | |
| D17 | band_select_acc2 | BAND_SELECT_ACC |
| D16 | band_select_acc1 | |
| D15 | Reserved | RESERVED (RO) |
| D14 | Reserved | |
| D13 | Reserved | |
| D12 | Reserved | |
| D11 | Reserved | |
| D10 | Reserved | |
| D9 | Reserved | |
| D8 | Reserved | RESERVED |
| D7 | Reserved | |
| D6 | ExtBndSelDiv4 | EXT_BND_SEL_DIV |
| D5 | ExtBndSelDiv3 | |
| D4 | ExtBndSelDiv2 | |
| D3 | ExtBndSelDiv1 | |
| D2 | CB3 | CONTROL BITS |
| D1 | CB2 | |
| D0 | CB1 | |

NOTE 1. It is recommended that the user writes to Register 0 after writing to Register 6.

NOTE 2. Bit D7 must be set to 0 for correct operation.

NOTE 3. RO Bits are Read Only Bits.

Table 11B. Register 6: 1-Bit Digital Lock Detect. Function Description

| Name | Description | Function |
|---------|--------------|--|
| DigLock | DIGITAL LOCK | 0 = PLL Not Locked 1 = PLL Locked (according LDF and LDP in Register 2) |

Table 11C. Register 6: 1-Bit Band Select Status (Read Only). Function Description

| Name | Description | Function |
|------------------|------------------|--|
| Band_select_done | BAND_SELECT_DONE | 0 = Band Selection Not Complete 1 = Band Selection Complete |

Table 11D. Register 6: 2-Bit Extra Lock Detect Precision. Function Description¹

| Name | Description | Factory Default | Function | | |
|--------------|--|-----------------|-----------|------------------------|-------|
| | | | Extra Bit | LDP Bits in Register 2 | Value |
| LDP_Ext[2:1] | LDP_EXT Extra Lock Detect Precision | 00 | 00 | 0 | 10ns |
| | | | | 1 | 6ns |
| | | | 01 | 0 | 3ns |
| | | | | 1 | 3ns |
| | | | 10 | 0 | 4ns |
| | | | | 1 | 4.5ns |
| 11 | 0 | 1.5ns | | | |
| | 1 | 1.5ns | | | |

NOTE 1. LDP_Ext[2:1] are Extra Lock Detect Precision bits. When these bits are set to 00, then the precision of the Lock Detect precision only relies on the LDP bit in Register 2, so that the lock detect window is 10ns or 6ns, depending on the LDP bit in Register 2. For high PFD frequencies, the 6ns window may be larger than the entire ref/FB period. The LDP_ext bits reduce the size of the lock detect window to the value described in [Table 11B, Page 29](#), allowing an accurate lock detection with higher PFD frequencies.

Table 11E. Register 6: 1-Bit Extra Bit of RF_OUTB Power. Function Description^{1 2}

| Name | Description | Factory Default | Function | | |
|----------------|----------------|-----------------|-----------|---|-------------|
| | | | Extra Bit | RF_OUTB OUTPUT POWER Bits in Register 4 | Value (dBm) |
| rf_outb_hi_pwr | RF_OUTB_HI_PWR | 0 | 0 | 00 | -4 |
| | | | | 01 | -1 |
| | | | | 10 | +2 |
| | | | | 11 | +5 |
| | | | 1 | 00 | +2 |
| | | | | 01 | +5 |
| | | | | 10 | +6 |
| | | | | 11 | +7 |

NOTE 1. RF_OUTB_HI_PWR is an Extra Bit of RF_OUTB Power that increases the output power to the RF_OUT_B output.

NOTE 2. $f_{RF_OUT} = 34.375\text{MHz}$.

Table 11F. Register 6: 1-Bit Extra Bit of RF_OUTA Power. Function Description^{1 2}

| Name | Description | Factory Default | Function | | |
|----------------|----------------|-----------------|-----------|---|-------------|
| | | | Extra Bit | RF_OUTA OUTPUT POWER Bits in Register 4 | Value (dBm) |
| rf_outa_hi_pwr | RF_OUTA_HI_PWR | 0 | 0 | 00 | -4 |
| | | | | 01 | -1 |
| | | | | 10 | +2 |
| | | | | 11 | +5 |
| | | | 1 | 00 | +2 |
| | | | | 01 | +5 |
| | | | | 10 | +6 |
| | | | | 11 | +7 |

NOTE 1. RF_OUTA_HI_PWR is an Extra Bit of RF_OUTA Power that increases the output power to the RF_OUT_A output.

NOTE 2. $f_{RF_OUT} = 34.375\text{MHz}$.

Table 11G. Register 6: 2-Bit Sigma Delta Modulator Order Configuration. Function Description

| Name | Description | Factory Default | Function |
|---------------|-------------|-----------------|---|
| SDMOrder[2:1] | SDM_ORDER | 11 | 00 = OFF. The device operates in integer mode and the fractional part is ignored. 01 = 1 st order 10 = 2 nd order 11 = 3 rd order |

Table 11H. Register 6: 2-Bit Dither Gain Configuration. Function Description

| Name | Description | Factory Default | Function |
|---------|-------------|-----------------|---|
| DitherG | DITHER_GAIN | 0 | 0 = LSB Dither (Recommended) 1 = LSB x4 Dither |

Table 11I. Register 6: 1-Bit Dither Noise Shaping Configuration. Function Description

| Name | Description | Factory Default | Function |
|---------------|-----------------|-----------------|---|
| ShapeDitheren | SHAPE_DITHER_EN | 1 | 0 = Dither Noise Shaping Disabled 1 = Dither Noise Shaping Enabled |

Table 11J. Register 6: 1-Bit Sigma Delta Modulator Type Configuration. Function Description

| Name | Description | Factory Default | Function |
|--------------|-------------|-----------------|---|
| SDMType[2:1] | SDM_TYPE | 01 | 00 = Reserved 01 = SSMF-II 10 = SSMF-I 11 = SSMF-B |

Table 11M. Register 6: 2-Bit VCO Band Selection Accuracy Configuration. Function Description

| Name | Description | Factory Default | Function |
|----------------------|-----------------|-----------------|--|
| band_select_acc[2:1] | BAND_SELECT_ACC | 00 | 00 = 1 cycle of the band select clock (output of the Band Select Divider) 01 = 2 cycles 10 = 4 cycles 11 = Reserved |

Table 11N. Register 6: 4-Bit Extra Most Significant Bits of Band Select Divider. Function Description^{1 2}

| Name | Description | Factory Default | Value | Function |
|-------------------|-----------------|-----------------|------------------------------------|------------------------|
| ExtBndSelDiv[4:1] | EXT_BND_SEL_DIV | 0000 | BSCC_R4 + [EXT_BND_SEL_DIV]x256 | 0000 = [BSCC_R4] |
| | | | | 0001 = [BSCC_R4]+256 |
| | | | | 0010 = [BSCC_R4] + 512 |
| | | | | |
| | | | | 1111 = [BSCC_R4]+3840 |

NOTE 1. EXT_BND_SEL_DIV are Extra 4 MSBs that extend the Band Select Clock Counter in Register 4. These additional bits are necessary for band selection to divide down to <500kHz when high PFD frequencies are used.

NOTE 2. BSCC_R4 is the BAND SELECT CLOCK COUNTER value in Register 4.

Table 11O. Register 6: 3-Bit Control Bits. Function Description¹

| Name | Description | Function |
|---------|--------------|--------------------------------|
| CB[3:1] | CONTROL BITS | 110 = Register 6 is programmed |

NOTE 1. The user has to set CB[3:1] to 110 in order to write to Register 6.

Register 7
Table 12A. Register 7 Bit Allocation^{1 2}

| BITS | NAME | DESCRIPTION |
|------|----------------|---------------------|
| D31 | Loss_Dig_Lock | LOSS_DIG_LOCK (SB) |
| D30 | Loss_Anlg_Lock | LOSS_ANLG_LOCK (SB) |
| D29 | Spi_error | SPI_ERROR (SB) |
| D28 | Reserved | RESERVED |
| D27 | Rev_ID3 | REV_ID (RO) |
| D26 | Rev_ID2 | |
| D25 | Rev_ID1 | |
| D24 | Dev_ID4 | DEV_ID (RO) |
| D23 | Dev_ID3 | |
| D22 | Dev_ID2 | |
| D21 | Dev_ID1 | |
| D20 | 16b_12b_sel | 16b_12b_SEL |
| D19 | RESERVED | RESERVED |
| D18 | RESERVED | RESERVED |
| D17 | RESERVED | RESERVED |
| D16 | RESERVED | RESERVED |
| D15 | ext_mod4 | EXT_MOD |
| D14 | ext_mod3 | |
| D13 | ext_mod2 | |
| D12 | ext_mod1 | |
| D11 | ext_fdiv4 | EXT_FRAC |
| D10 | ext_fdiv3 | |
| D9 | ext_fdiv2 | |
| D8 | ext_fdiv1 | |
| D7 | scike | SCLKE |
| D6 | Rd_Addr3 | READBACK_ADDR |
| D5 | Rd_Addr2 | |
| D4 | Rd_Addr1 | |
| D3 | SPI_R_WN | SPI_R_WN |
| D2 | CB3 | CONTROL BITS |
| D1 | CB2 | |
| D0 | CB1 | |

NOTE 1. SB Bits are Sticky Bits and need to be cleared.

NOTE 2. RO Bits are Read Only Bits.

Table 12B. Register 7: 1-Bit Loss of Digital Lock. Function Description¹

| Name | Description | Function |
|---------------|---------------|--|
| Loss_Dig_Lock | LOSS_DIG_LOCK | 0 = Locked since last time register was cleared 1 = Loss of Digital Lock since last time register was cleared |

NOTE 1. This bit is a sticky bit and needs to be cleared with a SPI write of 1 to detect further Loss of Digital Lock occurrences.

Table 12C. Register 7: 1-Bit Loss of Analog Lock. Function Description¹

| Name | Description | Function |
|----------------|----------------|---|
| Loss_Anlg_Lock | LOSS_ANLG_LOCK | 0 = Band Selection remained the same since last time register was cleared 1 = Band selection occurred since last time register was cleared |

NOTE 1. This bit is a sticky bit and needs to be cleared with a SPI write of 1 to detect further Band Selection occurrences.

Table 12D. Register 7: 1-Bit SPI Error. Function Description¹

| Name | Description | Function |
|-----------|-------------|---|
| Spi_error | SPI_ERROR | 0 = No SPI write error detection 1 = SPI Write error |

NOTE 1. Spi_error Bit goes high if the SPI interface detects a cycle with the incorrect number of SCLK cycles between nCS asserted Low and nCS asserted High. The SPI interface expects 32 clock cycles between nCS asserted Low and nCS asserted High. Any Read/Write via the SPI interface with more or less than 32 clock cycles will result in the Spi_error Bit switched to 1. This bit is a sticky bit and needs to be cleared with a SPI write of 1 in order to detect further possible SPI Write/Read errors.

Table 12E. Register 7: 3-Bit Revision ID. Function Description

| Name | Description | Factory Default |
|-------------|-------------|-----------------|
| Rev_ID[3:1] | REV_ID | 001 |

Table 12F. Register 7: 4-Bit Device ID. Function Description

| Name | Description | Factory Default |
|-------------|-------------|-----------------|
| Dev_ID[4:1] | DEV_ID | 0110 |

Table 12G. Register 7: 1-Bit Resolution Select. Function Description

| Name | Description | Factory Default | Function |
|-------------|-------------|-----------------|---|
| 16b_12b_sel | 16b_12b_SEL | 0 | 0 = FRAC, PHASE and MOD set to 12-Bit resolution, Bit[D19:D8] set to 0 and unused |
| | | | 1 = FRAC, PHASE and MOD set to 16-Bit resolution |

Table 12H. Register 7: 4-Bit Extra Bits of MOD Value. Function Description¹

| Name | Description | Factory Default | Function | | | | | |
|--------------|-------------|-----------------|----------------|---------|-------------|--|--|--|
| | | | MOD | EXT_MOD | Value | | | |
| ext_mod[4:1] | EXT_MOD | 0000 | 0000 0000 0000 | 0000 | Not Allowed | | | |
| | | | | 0001 | Not Allowed | | | |
| | | | | 0010 | 2 | | | |
| | | | | ... | ... | | | |
| | | | | 1111 | 15 | | | |
| | | | 0000 0000 0001 | 0000 | 16 | | | |
| | | | | ... | ... | | | |
| | | | | 1111 | 31 | | | |
| | | | ... | | | | | |
| | | | 1111 1111 1111 | 0000 | 65520 | | | |
| | | | | ... | ... | | | |
| | | | | 1111 | 65535 | | | |

NOTE 1. Bit D20 in Register 7 (16b_12b_SEL) is required to be set to 1 when using this table. If Bit D20 in Register 7 (16b_12b_SEL) is set to 0, refer to [Table 6D, Page 19](#).

Table 12I. Register 7: 4-Bit Extra Bits of FRAC Value. Function Description¹

| Name | Description | Factory Default | Function | | | | |
|---------------|-------------|-----------------|----------------|----------|-------|------|-------|
| | | | FRAC | EXT_FRAC | Value | | |
| ext_fdiv[4:1] | EXT_FRAC | 0000 | 0000 0000 0000 | 0000 | 0 | | |
| | | | | 0001 | 1 | | |
| | | | | ... | ... | | |
| | | | | 1111 | 15 | | |
| | | | 0000 0000 0001 | 0000 | 16 | | |
| | | | | ... | ... | | |
| | | | | 1111 | 31 | | |
| | | | ... | | | 0000 | 65520 |
| | | | ... | | | ... | ... |
| | | | 1111 1111 1111 | | | 1111 | 65535 |

NOTE 1. Bit D20 in Register 7 (16b_12b_SEL) is required to be set to 1 when using this table. If Bit D20 in Register 7 (16b_12b_SEL) is set to 0, refer to [Table 5C, Page 17](#).

Table 12J. Register 7: 1-Bit SCLKE. Function Description

| Name | Description | Factory Default | Function |
|-------|-------------|-----------------|---|
| Sclke | SCLKE | 1 | 0 = Output Data in a Read Cycle on a Rising Edge of SCLK 1 = Output Data in a Read Cycle on a Falling Edge of SCLK |

Table 12K. Register 7: 1-Bit READBACK_ADDR. Function Description¹

| Name | Description | Function |
|--------------|---------------|--|
| Rd_Addr[3:1] | READBACK_ADDR | 000 = Register 0 001 = Register 1 010 = Register 2 011 = Register 3 100 = Register 4 101 = Register 5 110 = Register 6 111 = Register 7 |

NOTE 1. In order to Read a register, the user must write to Register 7 first and set the SPI_R_WN Bit to 1 (READ) and indicate the address of the register to read in the READBACK_ADDR Bit (Bits[D6:D4]).

Table 12L. Register 7: 1-Bit SPI_R_WN. Function Description¹

| Name | Description | Factory Default | Function |
|----------|-------------|-----------------|-----------------------|
| SPI_R_WN | SPI_R_WN | 0 | 0 = WRITE 1 = READ |

NOTE 1. Writing this bit to a '1' will allow the user to read back the register selected in READBACK_ADDR on the next 32 SCLK cycle. This bit will revert back to '0' once it is written with '1' and will not retain the '1' value.

Table 12M. Register 7: 3-Bit Control Bits. Function Description¹

| Name | Description | Function |
|---------|--------------|--------------------------------|
| CB[3:1] | CONTROL BITS | 111 = Register 7 is programmed |

NOTE 1. The user has to set CB[3:1] to 111 in order to write to Register 7.

Absolute Maximum Ratings

Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the **DC Characteristics or AC Characteristics** is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 13. Absolute Maximum Ratings

| Item | Rating |
|--|--------------------------|
| Supply Voltage, V_{DDX} | 3.63V |
| Analog Supply Voltage, V_{DDA} | 3.63V |
| Input, V_I REF_IN Other Inputs (MUTE, SDI, FLSW, V_{TUNE}) | -0.5 to $V_{DDA} + 0.5V$ |
| Outputs, V_O RF_OUT _{A-B} , nRF_OUT _{A-B} | -0.5 to $V_{DDA} + 0.5V$ |
| Outputs, V_O (SCLK, LD, nCS, MUX_OUT) | -0.5 to $V_{DDA} + 0.5V$ |
| Outputs, I_O Continuous Current Surge Current | 40mA 65mA |
| Outputs, I_O (SCLK, LD, nCS, MUX_OUT) Continuous Current Surge Current | 8mA 13mA |
| Junction Temperature, T_J | 125°C |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: V_{DDX} denotes V_{DD} , V_{CP} , V_{DD_SD} , V_{VCO} .

DC Electrical Characteristics

Table 14A. Power Supply DC Characteristics, $V_{DDX} = V_{DDA} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ ^{1 2 3}

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|------------------------------------|--|---------|---------|---------|-------|
| V_{DDX} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DDX} | Power Supply Current ⁴ | | | 72 | 97 | mA |
| I_{DDA} | Analog Supply Current ⁵ | RF_OUT _A / nRF_OUT _A - Active RF_OUT _B / nRF_OUT _B - Muted | | 50 | 62 | mA |
| | | RF_OUT _A / nRF_OUT _A - Active RF_OUT _B / nRF_OUT _B - Active | | 74 | 94 | mA |
| | | RF_OUT _A / nRF_OUT _A - Muted RF_OUT _B / nRF_OUT _B - Muted | | 30 | 36 | mA |
| I_{VCO} | VCO Supply Current | | | 36 | 51 | mA |
| | Power Down Mode | | | 10 | 15 | mA |

NOTE 1. V_{DDX} denotes V_{DDD} , V_{CP} , V_{DD_SD} , V_{VCO} .

NOTE 2. RF Outputs Terminated $50\Omega \pm 1\%$ to V_{DDA} .

NOTE 3. Output Power set to +2dBm.

NOTE 4. I_{DDX} denotes $I_{DDD} + I_{CP} + I_{DD_SD} + I_{VCO}$.

NOTE 5. I_{DDA} is dependent on the value of the M0 output divider. The numbers indicated for I_{DDA} show the current consumption when using the output divider M0 = 64, for which I_{DDA} is higher than when using any other M0 divider value.

Table 14B. Output Divider Incremental Current¹

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------------------------|-----------------|---------|---------|---------|-------|
| Output Divider Supply Current | Divide by 2 | | 6.5 | | mA |
| | Divide by 4 | | 7 | | mA |
| | Divide by 8 | | 1 | | mA |
| | Divide by 16 | | 1.5 | | mA |
| | Divide by 32 | | 2 | | mA |
| | Divide by 64 | | 2 | | mA |

NOTE 1. RF Output divider (\div M0) has an incremental increase in current as the divider value increases. This specification is the incremental current change per output divider step. For example, current of divide-by-2 is 6.5mA more than divide-by-1, current of divide-by-4 is 7mA more than divide-by-2, and so on. The total increase from \div 1 to \div 64 is $6.5mA + 7mA + 1mA + 1.5mA + 2mA + 2mA = 20mA$.

Table 14C. Typical Current by Power Domain¹

| Pin Name | Pin Number | Typical Current | Unit |
|--------------------|------------|-----------------|------|
| V _{CP} | 6 | 21 | mA |
| V _{VCO} | 16, 17 | 30 | mA |
| V _{DDD} | 28 | 1 | mA |
| V _{DD_SD} | 32 | 5 | mA |
| V _{DDA} | 10 | 50 | mA |

NOTE 1. Operating conditions are:

REF_IN = 25MHz

INT = 100 (integer mode)

RF Divider = +1

 RF_OUT_A = RF_OUT_B = 2.5GHz

 RF_{POWER} = -1dBm

Charge Pump = 0.31mA

Table 14D. LVCMOS DC Characteristics, V_{DDX} = V_{DDA} = 3.3V ± 5%, T_A = -40°C to 85°C¹

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|---------------------|-----------------|---|------------------------|------------------|-------|
| V _{IH} | Input High Voltage | MUTE, CE | 1.8 | | V _{DDX} | V |
| | | SDI, SCLK, nCS | 1.5 | | V _{DDX} | V |
| V _{IL} | Input Low Voltage | | -0.3 | | 0.6 | V |
| I _{IH} | Input High Current | SDI, MUTE, CE | V _{DDX} = 3.465V, V _{IN} = 1.8V | | 5 | μA |
| | | SCLK, nCS | V _{DDX} = 3.465V, V _{IN} = 1.8V | | 150 | μA |
| I _{IL} | Input Low Current | SDI, MUTE, CE | V _{DDX} = 3.465V, V _{IN} = 0V | -150 | | μA |
| | | SCLK, nCS | V _{DDX} = 3.465V, V _{IN} = 0V | -5 | | μA |
| V _{OH} | Output High Voltage | MUX_OUT, LD | V _{DDX} = 3.465V; I _{OH} = -500μA | V _{DDX} - 0.4 | | V |
| V _{OL} | Output Low Voltage | MUX_OUT, LD | V _{DDX} = 3.465V; I _{OL} = 500μA | | 0.4 | V |

 NOTE 1. V_{DDX} denotes V_{DDD}, V_{CP}, V_{DD_SD}, V_{VCO}.

AC Electrical Characteristics

Table 15A. AC Characteristics, $V_{DDX} = V_{DDA} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$ ¹

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|--|---|---------|-----------|-----------|-------|
| REF_IN | Input Reference Frequency ² | Ref Doubler Disabled | 5 | | 310 | MHz |
| | | Ref Doubler Enabled | 5 | | 100 | MHz |
| V _{PP} | Input Sensitivity | REF_IN Biased at $V_{DDA}/2$ ³ | 0.7 | | V_{DDA} | V |
| f _{VCO} | VCO Frequency | Fundamental VCO Mode | 2200 | | 4400 | MHz |
| f _{RF_OUT} | Output Frequency | Divider Values: 1, 2, 4, 8, 16, 32, 64 | 34.375 | | 4400 | MHz |
| f _{PFD} | PFD Frequency | Fractional Mode | | | 125 | MHz |
| | | Integer Mode | | | 310 | MHz |
| K _{VCO} | VCO Sensitivity | | | 40 | | MHz/V |
| t _{LOCK} | PLL Lock Time | Time from Low to High nCS until Low to High LD | | 1 | | ms |
| - | Output Power Variation | | | ±1 | | dB |
| - | RF Output Power | Muted | | <-80 | | dBm |
| - | Min/Max VCO Tuning Voltage | | | 0.5 / 2.5 | | V |

NOTE 1. V_{DDX} denotes V_{DD} , V_{CP} , V_{DD_SD} , V_{VCO} .

NOTE 2. For REF_IN <10MHz, the slew rate must be >21V/μs.

NOTE 3. AC-coupling the reference signal ensures $V_{DDA}/2$ biasing.

Table 15B. RF_OUT_[A:B] Phase Noise and Jitter Characteristics, V_{DDX} = V_{DDA} = 3.3V ± 5%, T_A = -40°C to 85°C^{1 2}

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|---|---|---------|---------|---------|--------|
| tjit(Ø) | RMS Phase Jitter (Random) | f = 156.25MHz Integration Range: 12kHz - 20MHz | | 161 | | fs |
| | | f = 2.05GHz Integration Range: 12kHz - 20MHz | | 245 | | fs |
| | | f = 1.76GHz Integration Range: 12kHz - 20MHz | | 228 | | fs |
| φ _N (100k) | RF Output Phase Noise Performance @ 1.1GHz (Open Loop) | 100kHz Offset from Carrier | | -118.4 | | dBc/Hz |
| φ _N (800k) | | 800kHz Offset from Carrier | | -141 | | dBc/Hz |
| φ _N (1M) | | 1MHz Offset from Carrier | | -143 | | dBc/Hz |
| φ _N (5M) | | 5MHz Offset from Carrier | | -152.4 | | dBc/Hz |
| φ _N (10M) | | 10MHz Offset from Carrier | | -154 | | dBc/Hz |
| φ _N (∞) | | Noise Floor (≥30MHz from Carrier) | | -154.9 | | dBc/Hz |
| φ _N (100k) | RF Output Phase Noise Performance @ 1.65GHz (Open Loop) | 100kHz Offset from Carrier | | -117.7 | | dBc/Hz |
| φ _N (800k) | | 800kHz Offset from Carrier | | -143.1 | | dBc/Hz |
| φ _N (1M) | | 1MHz Offset from Carrier | | -145.5 | | dBc/Hz |
| φ _N (5M) | | 5MHz Offset from Carrier | | -157.9 | | dBc/Hz |
| φ _N (10M) | | 10MHz Offset from Carrier | | -159.6 | | dBc/Hz |
| φ _N (∞) | | Noise Floor (≥30MHz from Carrier) | | -160.6 | | dBc/Hz |
| φ _N (100k) | RF Output Phase Noise Performance @ 2.3GHz (Open Loop) | 100kHz Offset from Carrier | | -112.1 | | dBc/Hz |
| φ _N (800k) | | 800kHz Offset from Carrier | | -135.7 | | dBc/Hz |
| φ _N (1M) | | 1MHz Offset from Carrier | | -137.8 | | dBc/Hz |
| φ _N (5M) | | 5MHz Offset from Carrier | | -150.8 | | dBc/Hz |
| φ _N (10M) | | 10MHz Offset from Carrier | | -153.8 | | dBc/Hz |
| φ _N (∞) | | Noise Floor (≥30MHz from Carrier) | | -155.1 | | dBc/Hz |
| φ _N (100k) | RF Output Phase Noise Performance @ 3.8GHz (Open Loop) | 100kHz Offset from Carrier | | -106 | | dBc/Hz |
| φ _N (800k) | | 800kHz Offset from Carrier | | -130.9 | | dBc/Hz |
| φ _N (1M) | | 1MHz Offset from Carrier | | -133.2 | | dBc/Hz |
| φ _N (5M) | | 5MHz Offset from Carrier | | -148.1 | | dBc/Hz |
| φ _N (10M) | | 10MHz Offset from Carrier | | -152.2 | | dBc/Hz |
| φ _N (∞) | | Noise Floor (≥30MHz from Carrier) | | -154.7 | | dBc/Hz |
| φ _N (100k) | RF Output Phase Noise Performance @ 4.4GHz (Open Loop) | 100kHz Offset from Carrier | | -102 | | dBc/Hz |
| φ _N (800k) | | 800kHz Offset from Carrier | | -127 | | dBc/Hz |
| φ _N (1M) | | 1MHz Offset from Carrier | | -129.5 | | dBc/Hz |
| φ _N (5M) | | 5MHz Offset from Carrier | | -146 | | dBc/Hz |
| φ _N (10M) | | 10MHz Offset from Carrier | | -150.5 | | dBc/Hz |
| φ _N (∞) | | Noise Floor (≥30MHz from Carrier) | | -153 | | dBc/Hz |
| - | Spurious Signals Due to PFD Frequency | f _{PFD} = 50MHz; RF_OUT _A = 2.2GHz | | -78 | | dBc |
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |

Table 15B. RF_OUT_[A:B] Phase Noise and Jitter Characteristics, $V_{DDX} = V_{DDA} = 3.3V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$ ^{1 2}

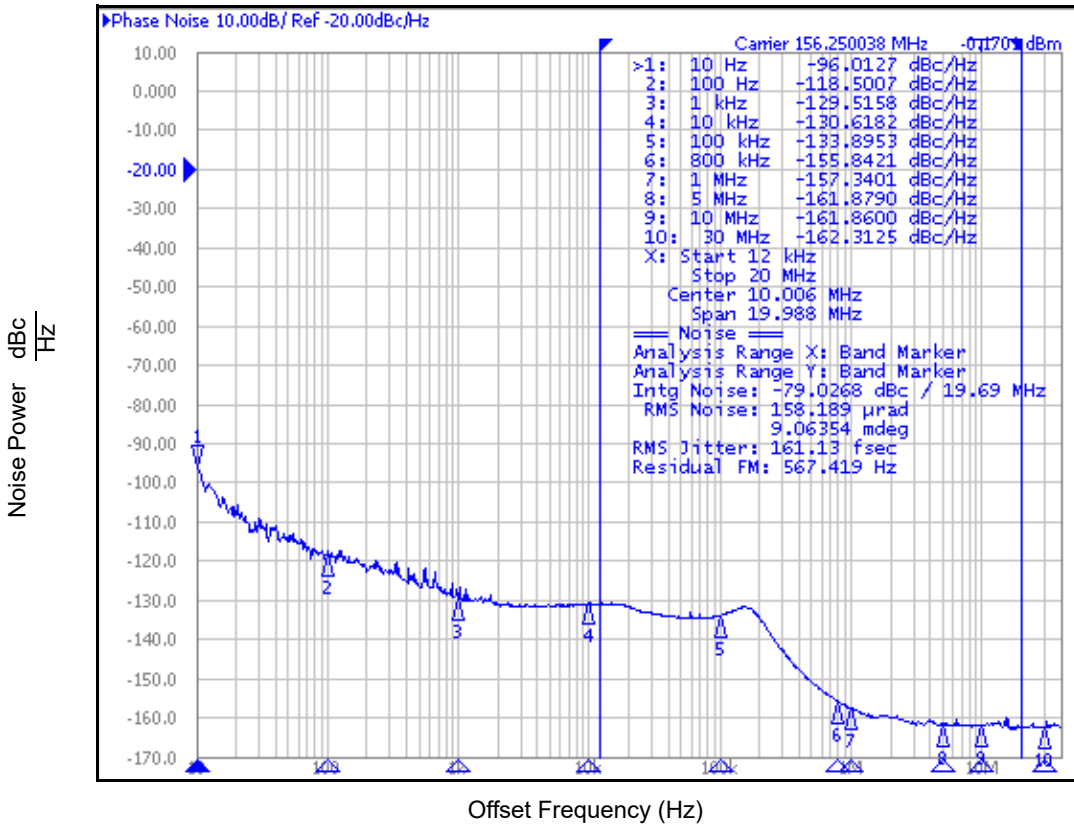
| | | | | | | |
|---------------------------|---|-----------------------------------|--|-----------|--|--------|
| - | In-Band Phase Noise | 3kHz from 2GHz Carrier | | -107 | | dBc/Hz |
| $\varphi_N(\text{SYNTH})$ | Normalized Phase Noise Floor | | | -231 | | dBc/Hz |
| $\varphi_N(1/f)$ | Normalized 1/f Noise ³ | 10kHz Offset; Normalized to 1GHz | | -122.8 | | dBc/Hz |
| Harmonics | $f_{RF_OUT} = f_{VCO}/1 = 2.2\text{GHz}$ | 2 nd / 3 rd | | -52/ -36 | | dB |
| | $f_{RF_OUT} = f_{VCO}/2 = 1.1\text{GHz}$ | 2 nd / 3 rd | | -32/ -18 | | dB |
| | $f_{RF_OUT} = f_{VCO}/32 = 100\text{MHz}$ | 2 nd / 3 rd | | -71/ -9.5 | | dB |
| | $f_{RF_OUT} = f_{VCO}/64 = 34.375\text{MHz}$ | 2 nd / 3 rd | | -69/ -9.4 | | dB |

NOTE 1. V_{DDX} denotes V_{DDD} , V_{CP} , V_{DD_SD} , V_{VCO} .

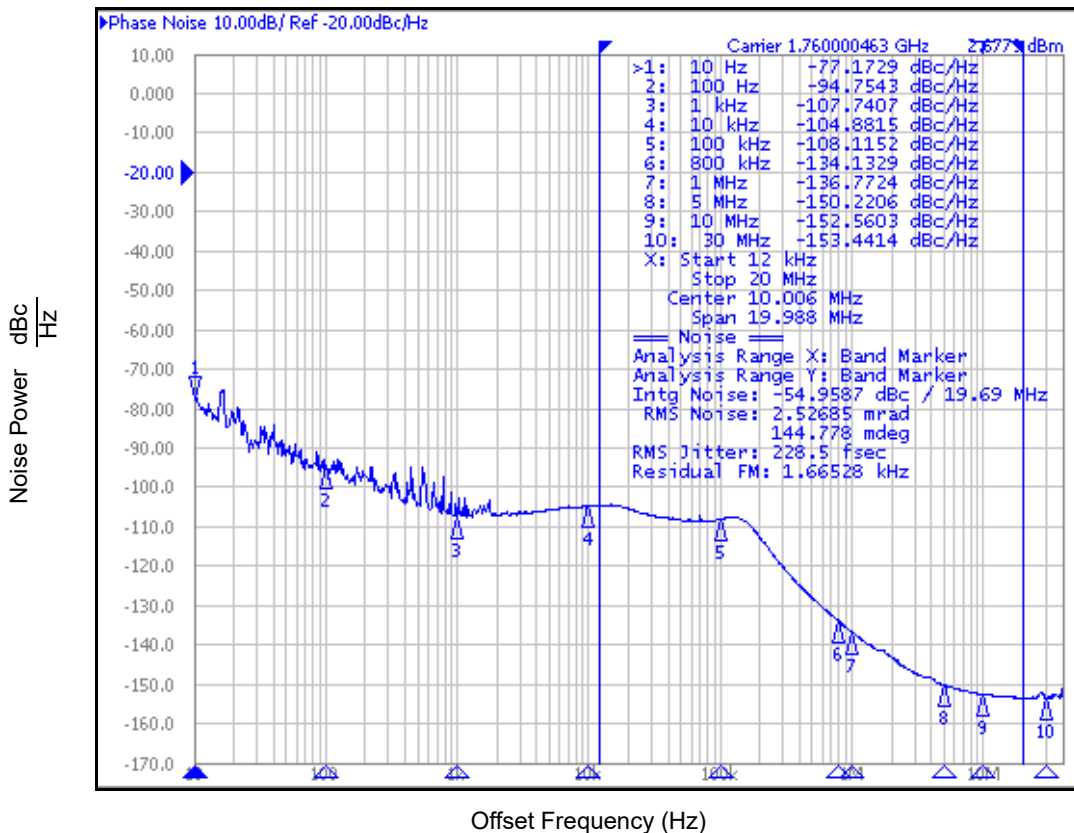
NOTE 2. RF_OUT_[A:B] output power setting = +2dBm.

NOTE 3. $\varphi_N(1/f) = \varphi_N(\text{RF_OUT}) - 10 \text{ Log}(10\text{kHz}/f) - 20 \text{ Log}(f_{RF_OUT}/1\text{GHz})$ where $\varphi_N(1/f)$ is the 1/f noise contribution at a RF_OUT frequency (f_{RF_OUT}) and at a frequency offset f .

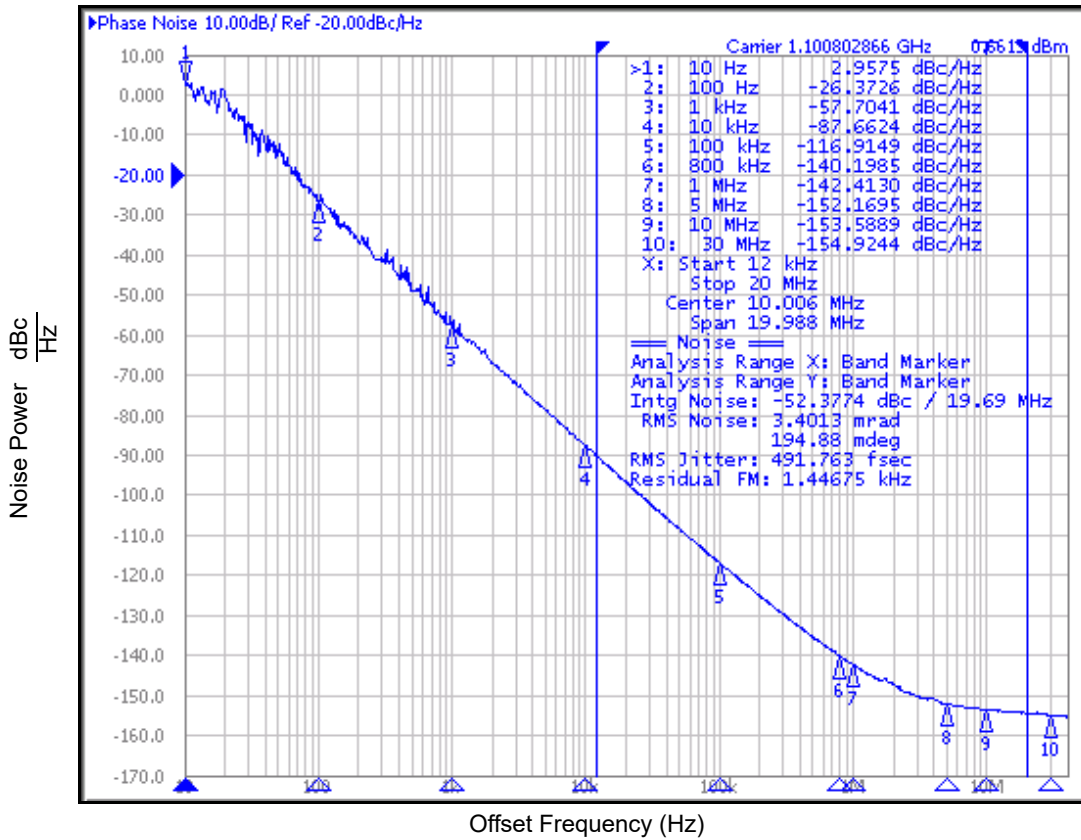
Phase Noise at 156.25MHz (3.3V)



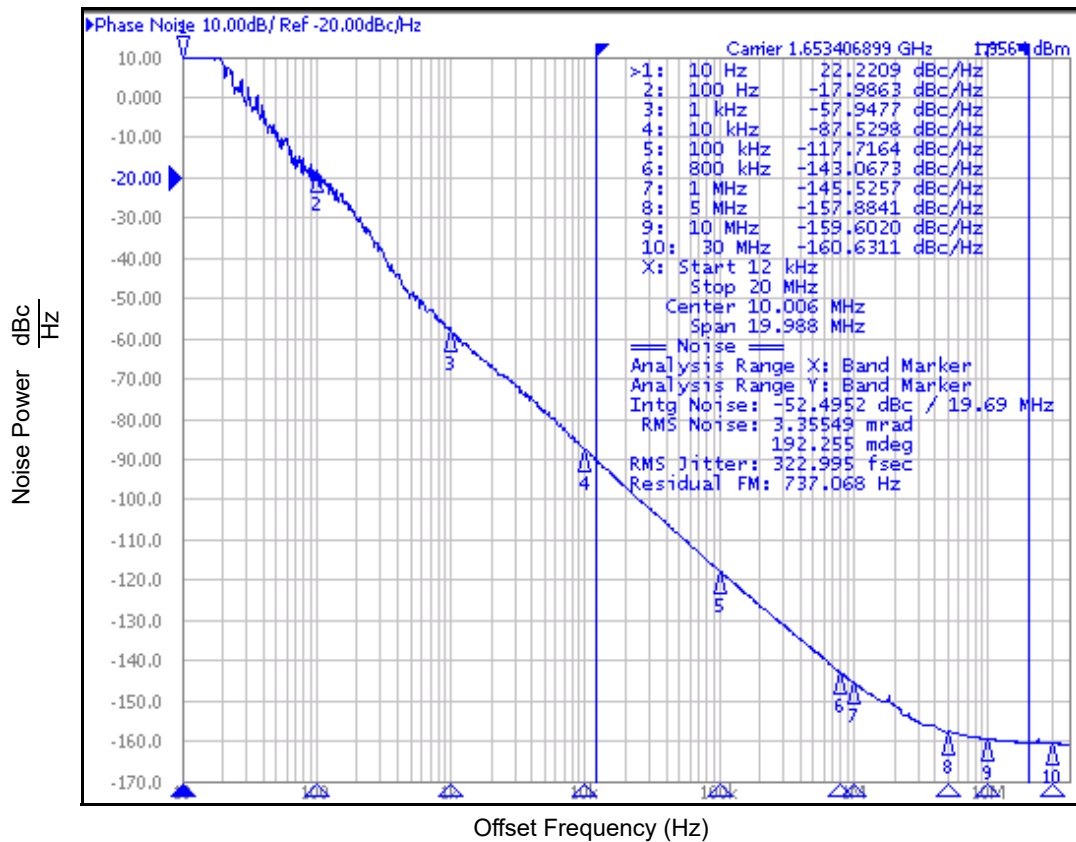
Phase Noise at 1.76GHz (3.3V)



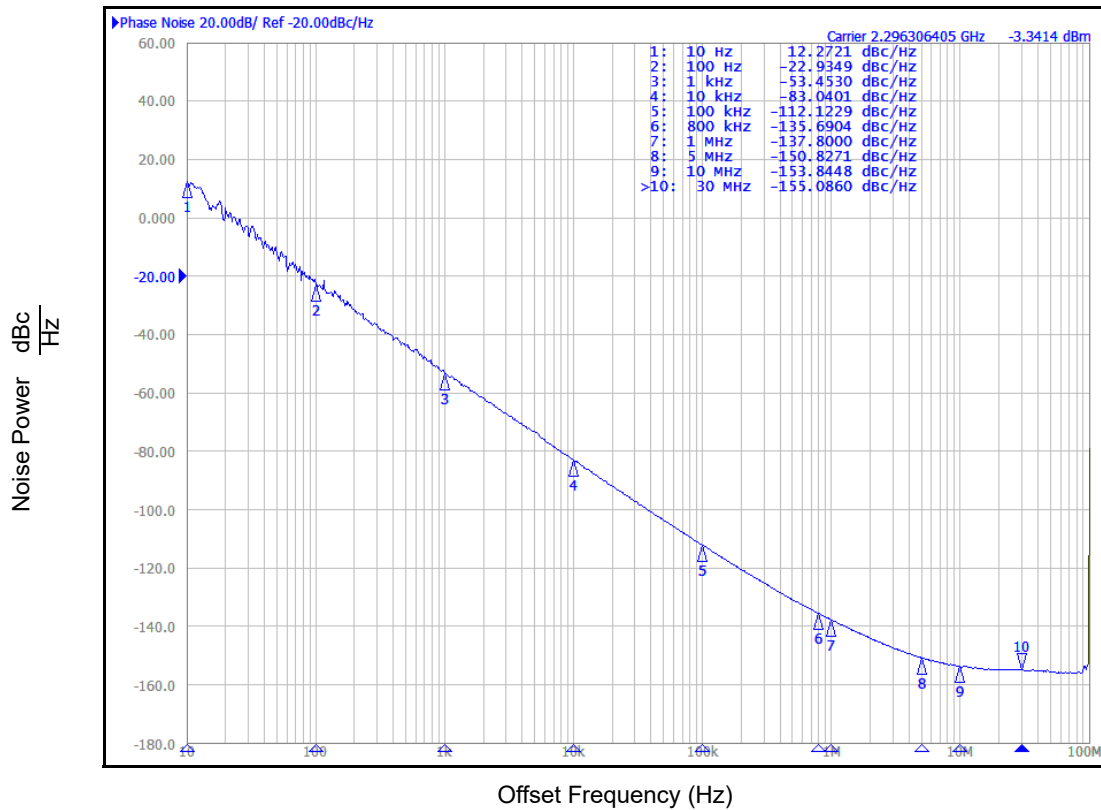
Phase Noise Performance (Open Loop) at 1.1GHz (3.3V)



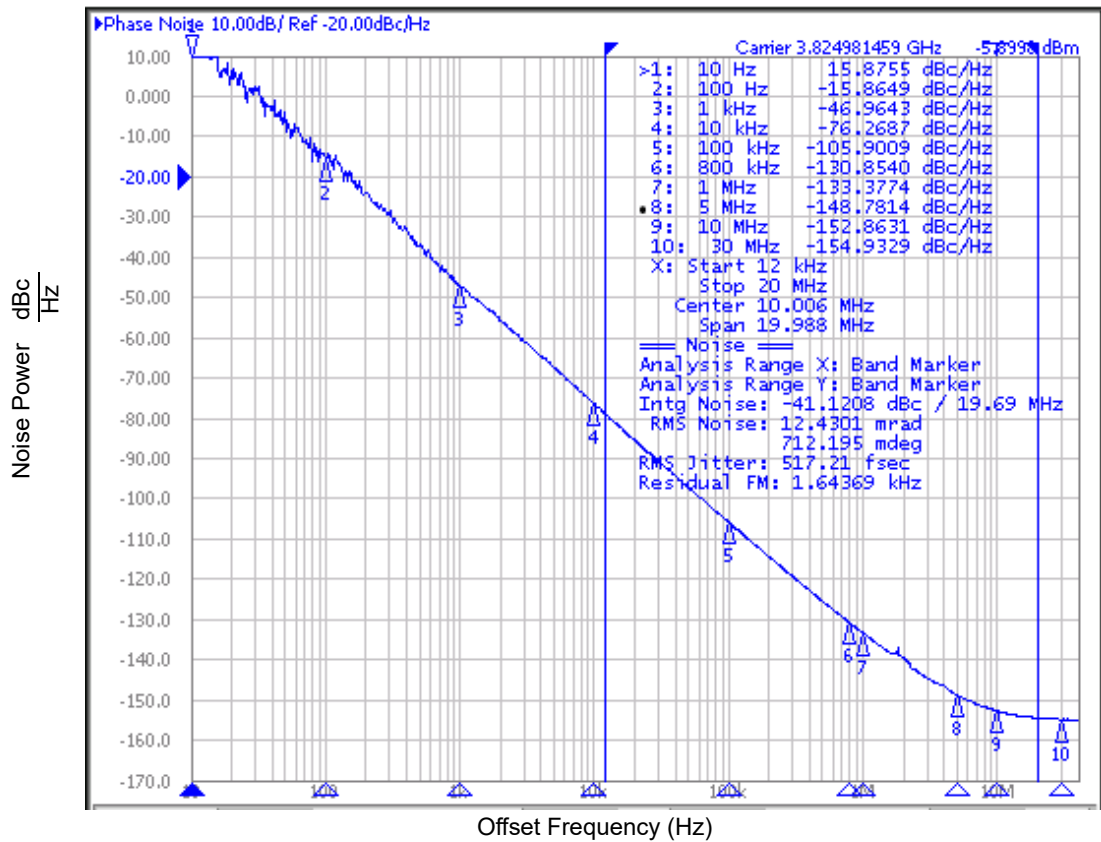
Phase Noise Performance (Open Loop) at 1.65GHz (3.3V)



Phase Noise Performance (Open Loop) at 2.3GHz (3.3V)



Phase Noise Performance (Open Loop) at 3.8GHz (3.3V)



Applications Information

Loop Filter Calculations

2nd Order Loop Filter

This section helps design a 2nd order loop filter for the 8V97051L. A general 2nd order loop filter is shown in [Figure 11, Typical 2nd Order Loop Filter](#). Step-by-step calculations to determine R_z, C_z and C_p values for a desired loop bandwidth are described below. Required parameters are provided. A spreadsheet for calculating the loop filter values is also available.

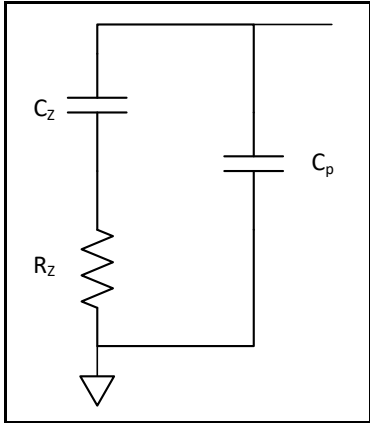


Figure 11. Typical 2nd Order Loop Filter

1. Determine desired loop bandwidth f_c .

2. Calculate R_z:

$$R_z = \frac{2 * \pi * f_c * N}{I_{cp} * K_{vco}}$$

Where,

I_{cp} is charge pump current. I_{cp} is programmable from 310μA to 5mA.

N is effective feedback divider. N must be programmed into the following value.

$$N = \frac{F_{vco}}{F_{pd}}$$

F_{vco} is VCO frequency.

VCO frequency range: 2200MHz to 4400MHz

F_{pd} is phase detector input frequency.

$$F_{pd} = \frac{F_{ref}}{P_v}$$

F_{ref} is reference clock (REF_IN) input frequency.

P_v is overall pre-divider setting.

K_{vco} is VCO gain. K_{vco} = 40MHz/V

3. Calculate C_z:

$$C_z = \frac{\alpha}{2 * \pi * f_c * R_z}$$

Where,

$\alpha = f_c / f_z$, user can determine an α number.

$\alpha > 6$ is recommended.

f_z is frequency at zero.

4. Calculate C_p:

$$C_p = \frac{C_z}{\alpha * \beta}$$

Where,

$\beta = f_p / f_c$, user can determine β number.

$\beta > 4$ is recommended.

f_p is frequency at pole.

5. Verify Phase Margin (PM)

$$PM = \arctan \left(\frac{b - 1}{2 * \sqrt{b}} \right)$$

Where,

$$b = 1 + \frac{C_z}{C_p}$$

The phase margin (PM) should be greater than 50°.

A spreadsheet for calculating the loop filter component values is available at www.IDT.com. To use the spreadsheet, the user simply enters the following parameters:

f_c , F_{ref}, P_v, I_{cp}, F_{VCO}, α and β .

The spreadsheet will provide the component values, R_z, C_z and C_p as the result. The spreadsheet also calculates the maximum phase margin for verification.

3rd Order Loop Filter

This section helps design a 3rd order loop filter for the 8V97051L. A general 3rd order loop filter is shown in [Figure 12, Typical 3rd Order Loop Filter](#).

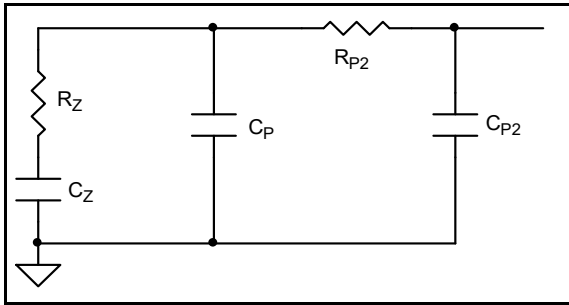


Figure 12. Typical 3rd Order Loop Filter

The R_Z , C_Z and C_P can be calculated as 2nd order loop filter. The following equation help determine the 3rd order loop filter R_{P2} and C_{P2} .

Pick an R_{P2} value. $R_{P2} \sim 1.5 \times R_Z$ is suggested.

$$C_{P2} = \frac{R_Z * C_P}{R_{P2} * \gamma}$$

Where,

γ is ratio between the 1st pole frequency and the 2nd pole frequency. $\gamma > 4$ is recommended.

Recommendations for Unused Input and Output Pins

Inputs:

LVC MOS Control Pins

All control pins have internal pullup and pulldown resistors; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

Outputs:

Output Pins

For any unused output, it can be left floating and disabled.

Schematic Example

Figure 13A and Figure 13B show general application schematic examples for the 8V97051L.

For power rails, bypass capacitors must be provided to all power supply pins. Suggest at least one bypass capacitor per power pin. Value can be ranged from 0.01uF or 0.1uF. Mix values of bypass capacitor can help filtering wider range of power supply noise.

The 8V97051L input is high impedance. The input termination depends on the driver type termination requirements. In these examples, the 8V97051L REF_IN input is terminated with a matched load termination. For transmission line with characteristic impedance $Z_0 = 50\Omega$, the termination resistor R8 is 50Ω . The input is self biased to proper DC offset after the AC coupling.

The loop filter values can be calculated to meet the loop bandwidth requirement. Please refer to the section, "Loop Filter Calculations" for detailed calculations. For fast lock mode, the loop filter can be configured as Fast Lock Loop Filter Option 1 or Fast Lock Loop Filter Option 2 shown in Figure 13A.

Fast Lock Loop Filter Option 1 is Parallel Resistor Configuration. For normal operating mode, only R5 is active and $R5 = R_s$, where R_s is the resistor value for normal operating mode loop bandwidth. In fast lock mode, the combination of R4 in parallel with R5 is active. For example, in normal operation mode, if the charge pump current is set at 0000 (ICP = 310uA), then, in fast lock mode, the loop bandwidth is set larger by increasing the charge pump current to ICP~5mA (ICP

setting = 1111 or 16 times the normal charge pump current). The combination of the R4 and R5 in parallel is $1/4 * R_s$.

Fast Lock Loop Filter Option 2 is Series Resistor Configuration. For normal operating mode, both R6 and R7 are active and $R6 + R7 = R_s$. For fast lock mode, only R6 is active. For example, in normal operation mode, if the charge pump current is set at 0000 (ICP = 310uA), then, in fast lock mode, the loop bandwidth is set larger by increasing the charge pump current to ICP~5mA (ICP setting = 1111 or 16 times the normal charge pump current). The sum of R6 and R7 equals to R_s , i.e. $R6 + R7 = R_s$. $R6 = 1/4 * R_s$ and $R7 = 3/4 * R_s$.

The 8V97051L output pull-up loading can be resistors or inductors. The pull up resistor value is typically 50Ω . Resistor pull up loading covers wide range of output frequencies. For inductor pull up loading, the inductor value is frequency dependent. One inductor value cannot cover all the output frequency range. This example shows the $L = 3.9nH$ that is suitable for approximately 2GHz operating frequency. The output can also drive single ended LO input. Figure 13B shows an example of the 8V97051L output driving single ended LO input of the mixer through an LC balun. The LC balun component values are frequency dependent. These values can be adjusted to optimize the performance. Single ended LO receiver input also can tap to one side of the differential driver using resistor loading or inductor loading. For single ended LO input, both sides of the differential driver still need to be loaded with pull up. The output power level can also be adjusted further through programming.

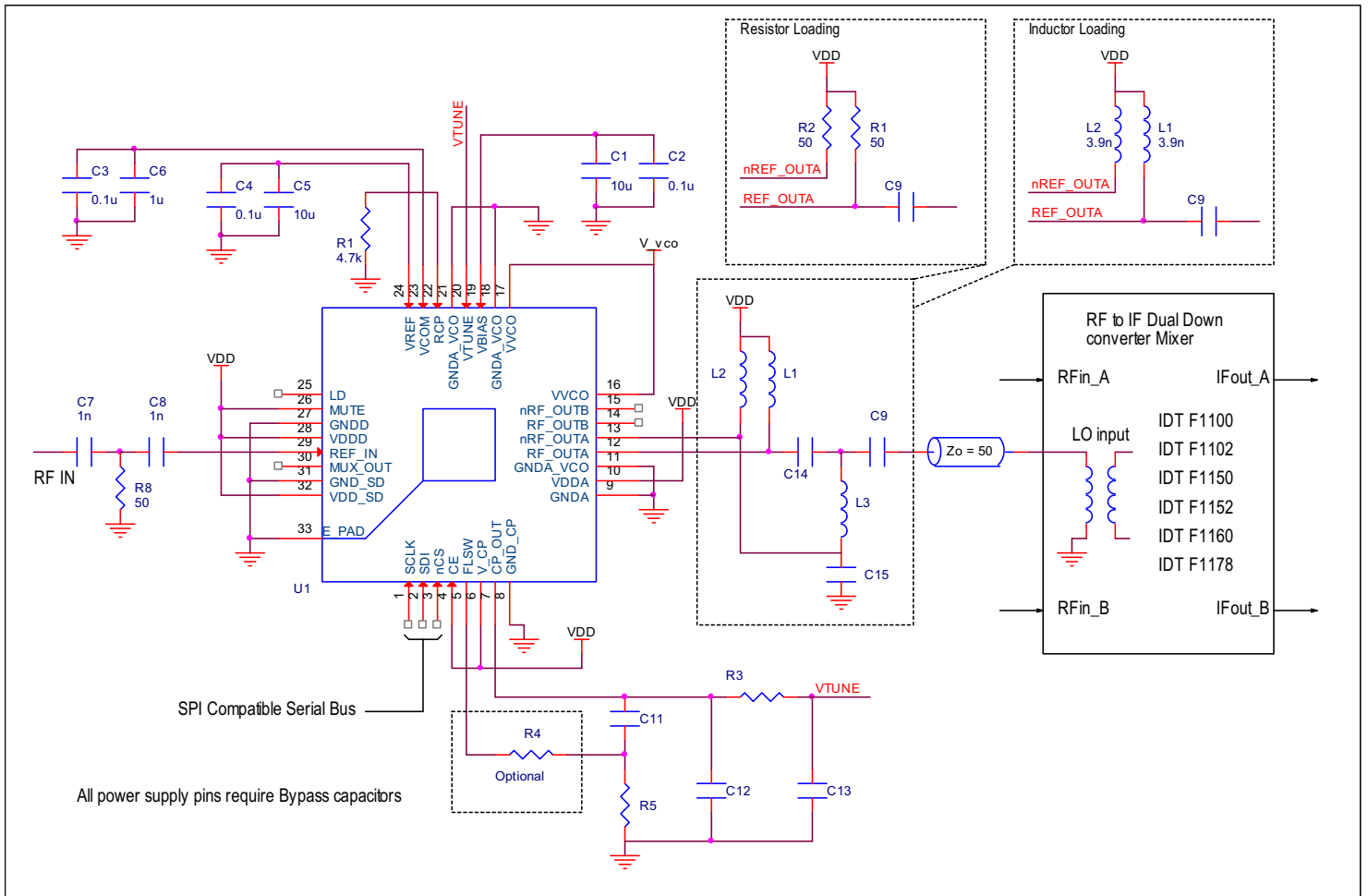


Figure 13B. Schematic Example for Driving Single Ended Mixer

Power Considerations

The 8V97051L device was designed and characterized to operate within the ambient industrial temperature range of -40°C to +85°C. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature. The power calculation example below was generated using a typical configuration. For many applications, the power consumption can vary depending on configuration. Please contact IDT technical support for any concerns on calculating the power dissipation for your own specific configuration.

1. Power Dissipation.

The total power dissipation for the 8V97051L is the sum of the core power plus the power dissipation in the output driver. The following is the power dissipation for $V_{DD} = 3.465V$, which gives worse case results.

- $$\text{Power (core)}_{MAX} = V_{DD_MAX} * (I_{DDA} + I_{VCO} + I_{CP} + I_{DD_SD} + I_{DDD})_{MAX} = V_{DD_MAX} * (I_{DDA} + I_{DDX})_{MAX}$$

$$= 3.465V * (94mA + 97mA) = \mathbf{661.8mW}$$

Total Power (with two outputs active at 2dBm output power level) = **661.8mW**

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 34.34°C/W per Table 16 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs active is:

$$85^\circ\text{C} + 0.662\text{W} * 34.34^\circ\text{C/W} = 107.7^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 16. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

| θ_{JA} by Velocity | | | |
|---|-----------|----------|-----------|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 34.34°C/W | 30.7°C/W | 29.12°C/W |

Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter Ψ_{JB} (Psi-JB) to calculate the junction temperature (T_J) and ensure it does not exceed the maximum allowed junction temperature in the Absolute Maximum Rating table.

The junction-to-board thermal characterization parameter, Ψ_{JB} , is calculated using the following equation:

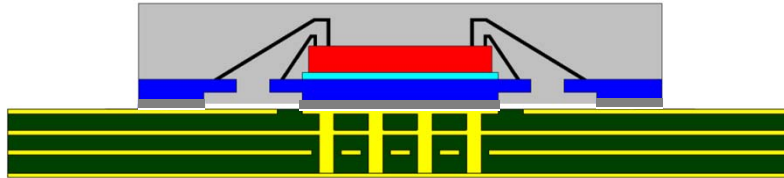
$$T_J = T_{CB} + \Psi_{JB} \times P_d, \text{ Where}$$

T_J = Junction temperature at steady state condition in ($^{\circ}\text{C}$).

T_{CB} = Case temperature (Bottom) at steady state condition in ($^{\circ}\text{C}$).

Ψ_{JB} = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.

P_d = power dissipation (W) in desired operating configuration.



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature (T_{CB}). A good connection ensures that temperature at the exposed pad (T_{CB}) and the board temperature (T_B) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example Calculation for Junction Temperature (T_J): $T_J = T_{CB} + \Psi_{JB} \times P_d$

| | |
|---------------|----------------------------------|
| Package type: | 32-Lead VFQFN |
| Body size: | 3mm x 3mm x 0.9mm |
| ePad size: | 3.15mm x 3.15mm |
| Thermal Via: | 4 x 4 matrix |
| Ψ_{JB} | 0.34 $^{\circ}\text{C}/\text{W}$ |
| T_{CB} | 105 $^{\circ}\text{C}$ |
| P_d | 0.6618 W |

For the variables above, the junction temperature is equal to 105.2 $^{\circ}\text{C}$. Since this is below the maximum junction temperature of 125 $^{\circ}\text{C}$, there are no long term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 107.7 $^{\circ}\text{C}$, this device can function without the degradation of the specified AC or DC parameters.

Reliability Information

Table 17A. θ_{JA} vs. Air Flow Table for a 32 lead VFQFN

| θ_{JA} vs. Air Flow | | | |
|---|-----------|----------|-----------|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 34.34°C/W | 30.7°C/W | 29.12°C/W |

Table 17B. θ_{JB} vs. Air Flow Table for a 32 lead VFQFN

| θ_{JB} vs. Air Flow | |
|---|-----------|
| Meters per Second | 0 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 0.472°C/W |

NOTE: θ_{JB} is independent of airflow.

Transistor Count

The 8V97051L transistor count is: 404,793

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/32-vfqfn-package-outline-drawing-50-x-50-x-090-mm-body-epad-315-x-315-mm-nlg32p1

Ordering Information

Table 18. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|-----------------|---|--------------------|----------------|
| 8V97051LNLGI | IDT8V97051LNLGI | 32-VFQFPN, Lead Free 5.0 × 5.0 × 0.90 mm | Tray | -40°C to +85°C |
| 8V97051LNLGI8 | IDT8V97051LNLGI | 32-VFQFPN, Lead Free Quadrant 1 (EIA-481-C) 5.0 × 5.0 × 0.90 mm | Tape & Reel | -40°C to +85°C |
| 8V97051LNLGI/W | IDT8V97051LNLGI | 32-VFQFPN, Lead Free Quadrant 2 (EIA-481-D) 5.0 × 5.0 × 0.90 mm | Tape & Reel | -40°C to +85°C |

Table 19. Pin 1 Orientation in Tape and Reel Packaging

| Part Number Suffix | Pin 1 Orientation | Illustration |
|--------------------|------------------------|---|
| NLGI8 | Quadrant 1 (EIA-481-C) | <p>Correct Pin 1 ORIENTATION</p> <p>CARRIER TAPE TOPSIDE (Round Sprocket Holes)</p> <p>USER DIRECTION OF FEED</p> |
| NLGI/W | Quadrant 2 (EIA-481-D) | <p>Correct Pin 1 ORIENTATION</p> <p>CARRIER TAPE TOPSIDE (Round Sprocket Holes)</p> <p>USER DIRECTION OF FEED</p> |

Revision History

| Revision Date | Description of Change |
|------------------|--|
| August 7, 2018 | <ul style="list-style-type: none"> * Changed incorrect measurement unit nF to nH in Output Matching and Schematic Example * Updated the Package Outline Drawings; however, no mechanical changes * Updated Note 3 in Table 15B * Completed other minor changes |
| January 31, 2017 | Initial release. |