

Description

The 8V49NS1412 is a clock generator with four output dividers: three integers, and one that is either integer or fractional. When used with an external crystal, the 8V49NS1412 generates high-performance timing for the communications and datacom markets, especially for applications that demand extremely low phase noise, such as 10GE, 40GE, 100G, and 400GE.

The 8V49NS1412 provides versatile frequency configurations and output formats, and is optimized to deliver excellent phase noise performance. The device delivers an optimum combination of high clock frequency and low phase noise performance, combined with high power supply noise rejection.

The 8V49NS1412 supports two types of output levels: LVPECL or LVDS on eleven of its outputs. In addition, the device has a single LVCMOS output that can provide a generated clock, or act as a reference bypass output.

The device can be configured to deliver specific configurations under pin control only, or additional configurations through an I²C serial interface by external processor, or an external I²C EEPROM to loading the configuration.

Typical Applications

- 10G/40G/100/400G Ethernet
- Fiber optics
- Gigabit Ethernet, Terabit IP switches/routers
- CPRI Interfaces

Features

- Eleven differential LVPECL and LVDS outputs with programmable voltage swings
- One LVCMOS output: Input reference can be passed to this output
- The clock input operates in full differential mode (LVDS, LVPECL) or single-ended LVCMOS mode
- Driven from a crystal or differential clock input
- 2.4–2.5 GHz PLL frequency range supports Ethernet, SONET, and CPRI frequency plans
- Four Integer output dividers with a range of output divide ratios (see [Table 5](#))
- One Fractional output divider can generate any desired output frequency
- Support of output power-down
- Excellent clock output phase noise:

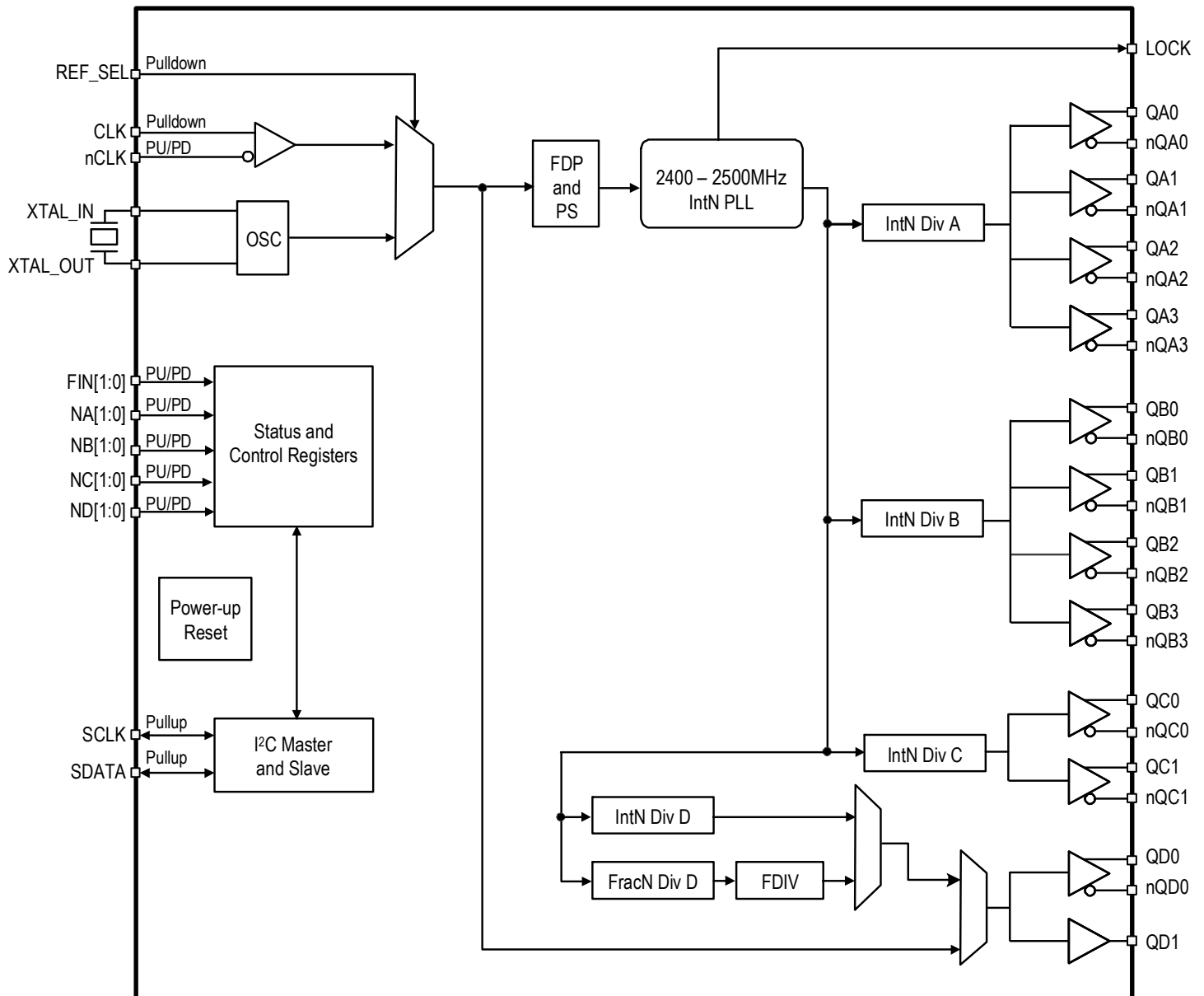
| Offset | Output Frequency | Single-side Band Phase Noise |
|--------|------------------|------------------------------|
| 100kHz | 156.25MHz | -143dBc/Hz |
- RMS phase noise, 12kHz to 20MHz integration range: 110fs (maximum) at 156.25MHz
- Selected configurations can be controlled via the control input pins without need for serial port access
- LVCMOS compatible I²C serial interface gives access to additional configuration by external processor or loading the configuration from an external I²C EEPROM, or in combination with the control input pins
- Single 3.3V supply voltage
- 64-VFQFPN 9 × 9 mm, lead-free (RoHS 6) package
- -40°C to +85°C ambient operating temperature

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Block Diagram

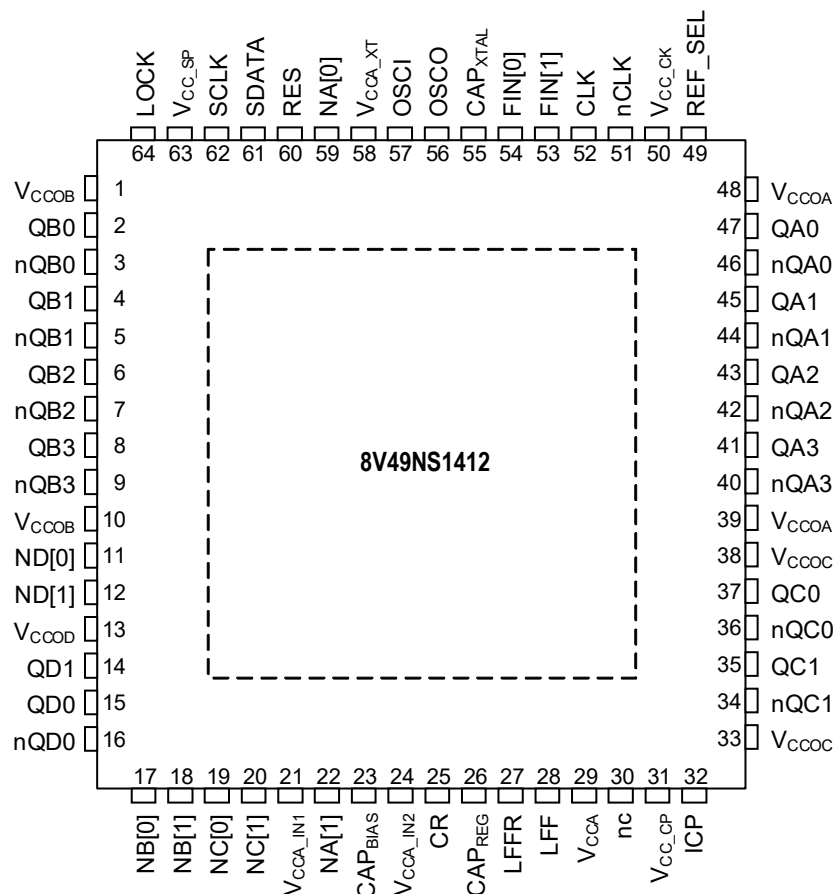
Figure 1. 8V49NS1412 Block Diagram



Transistor count: 132,756

Pin Assignments

Figure 2. Pin Assignments for 9 × 9 mm 64-Lead VFQFPN Package — Top View



Pin Descriptions

Table 1. Pin Descriptions

| Number | Name | Type | Description |
|--------|-------|---------------|---|
| 1 | VCCOB | Power | Power supply voltage for output Bank B (3.3V). |
| 2 | QB0 | Output | Differential clock output pair. LVPECL or LVDS with configurable amplitude. |
| 3 | nQB0 | Output | |
| 4 | QB1 | Output | Differential clock output pair. LVPECL or LVDS with configurable amplitude. |
| 5 | nQB1 | Output | |
| 6 | QB2 | Output | Differential clock output pair. LVPECL or LVDS with configurable amplitude. |
| 7 | nQB2 | Output | |
| 8 | QB3 | Output | Differential clock output pair. LVPECL or LVDS with configurable amplitude. |
| 9 | nQB3 | Output | |
| 10 | VCCOB | Power | Power supply voltage for output Bank B (3.3V). |
| 11 | ND[0] | Input [PU/PD] | Control input for output Bank D. 3-level signals (see Table 10). |
| 12 | ND[1] | Input [PU/PD] | Control input for output Bank D. 3-level signals (see Table 10). |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|--------|----------------------|---------------|--|
| 13 | V _{CCOD} | Power | Power supply voltage for output Bank D (3.3V). |
| 14 | QD1 | Output | Single-ended output clock. LVCMOS output levels. |
| 15 | QD0 | Output | Differential clock output pair. LVPECL or LVDS with configurable amplitude. |
| 16 | nQD0 | Output | |
| 17 | NB[0] | Input [PU/PD] | Control input for output Bank B. 3-level signals (see Table 8). |
| 18 | NB[1] | Input [PU/PD] | Control input for output Bank B. 3-level signals (see Table 8). |
| 19 | NC[0] | Input [PU/PD] | Control input for output Bank C. 3-level signals (see Table 9). |
| 20 | NC[1] | Input [PU/PD] | Control input for output Bank C. 3-level signals (see Table 9). |
| 21 | V _{CCA_IN1} | Power | Analog power supply voltage for PLL (3.3V). |
| 22 | NA[1] | Input [PU/PD] | Control input for output Bank A. 3-level signals (see Table 7). |
| 23 | CAP _{BIAS} | Analog | Internal VCO bias decoupling capacitor. Use a 4.7μF capacitor between the CAP _{BIAS} terminal and V _{EE} . |
| 24 | V _{CCA_IN2} | Power | Analog power supply voltage for VCO (3.3V). |
| 25 | CR | Analog | Internal VCO regulator decoupling capacitor. Use a 1μF capacitor between the CR and the V _{CCA} terminals. |
| 26 | CAP _{REG} | Analog | Internal VCO regulator decoupling capacitor. Use a 4.7μF capacitor between the CAP _{REG} terminal and V _{EE} . |
| 27 | LFFR | Analog | Ground return path pin for the PLL loop filter. |
| 28 | LFF | Output | Loop filter/charge pump output for the FemtoClock NG PLL. Connect to the external loop filter. |
| 29 | V _{CCA} | Power | Analog power supply voltage for VCO (3.3V). |
| 30 | nc | - | No connect. Do not use. |
| 31 | V _{CC_CP} | Power | Analog power supply voltage for PLL charge pump (3.3V). |
| 32 | ICP | Analog | Charge pump current input for PLL. Connect to LFF pin (28). |
| 33 | V _{CCOC} | Power | Power supply voltage for output Bank C (3.3V). |
| 34 | nQC1 | Output | Differential clock output pair. LVPECL or LVDS with configurable amplitude. |
| 35 | QC1 | Output | |
| 36 | nQC0 | Output | Differential clock output pair. LVPECL or LVDS with configurable amplitude. |
| 37 | QC0 | Output | |
| 38 | V _{CCOC} | Power | Power supply voltage for output Bank C (3.3V). |
| 39 | V _{CCOA} | Power | Power supply voltage for output Bank A (3.3V). |
| 40 | nQA3 | Output | Differential clock output pair. LVPECL or LVDS with configurable amplitude. |
| 41 | QA3 | Output | |
| 42 | nQA2 | Output | Differential clock output pair. LVPECL or LVDS with configurable amplitude. |
| 43 | QA2 | Output | |
| 44 | nQA1 | Output | Differential clock output pair. LVPECL or LVDS with configurable amplitude. |
| 45 | QA1 | Output | |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|--------|---------------------|---------------|---|
| 46 | nQA0 | Output | Differential clock output pair. LVPECL or LVDS with configurable amplitude. |
| 47 | QA0 | Output | |
| 48 | V _{CCOA} | Power | Power supply voltage for output Bank A (3.3V). |
| 49 | REF_SEL | Input [PD] | Selects input reference source. LVCMOS interface levels. 0 = Crystal input on pins OSCI, OSCO (default) 1 = Reference clock input on pins CLK, nCLK |
| 50 | V _{CC_CK} | Power | Power supply voltage for input CLK, nCLK (3.3V). |
| 51 | nCLK | Input [PU/PD] | Inverting differential clock input. Internal resistor bias to V _{CC_CK} /2. |
| 52 | CLK | Input [PD] | Non-inverting differential clock input. |
| 53 | FIN[1] | Input [PU/PD] | Control Inputs for input reference frequencies. 3-level signals (see Table 3). |
| 54 | FIN[0] | Input [PU/PD] | |
| 55 | CAP _{XTAL} | Analog | Crystal oscillator circuit decoupling capacitor. Use a 4.7μF capacitor between the CAP _{XTAL} and the V _{EE} terminals. |
| 56 | OSCO | Output | Crystal oscillator interface. |
| 57 | OSCI | Input | |
| 58 | V _{CCA_XT} | Power | Analog power supply voltage for the crystal oscillator (3.3V). |
| 59 | NA[0] | Input [PU/PD] | Control input for output Bank A. 3-level signals (see Table 7). |
| 60 | RES | Analog | Connect a 2.8kΩ (1%) resistor to V _{EE} for output current calibration. |
| 61 | SDATA | I/O [PU] | I ² C data input/output: LVCMOS interface levels. Open-drain pin. |
| 62 | SCLK | I/O [PU] | I ² C clock input/output. LVCMOS interface levels. Open-drain pin. |
| 63 | V _{CC_SP} | Power | Power supply voltage for the I ² C port (3.3V). |
| 64 | LOCK | Output | Lock status output. LVCMOS interface levels. Logic Low = PLL not locked Logic High = PLL locked |
| ePad | V _{EE} | Power | Negative supply. Exposed pad must be connected to ground. |

Principles of Operation

The 8V49NS1412 can be locked to either an input reference clock or a 10MHz to 50MHz fundamental-mode crystal, and generate a wide range of synchronized output clocks. Lock status can be monitored via the LOCK pin.

The 8V49NS1412 accepts a differential or single-ended input clock ranging from 5MHz to 1GHz. It generates up to twelve output clocks with up to four different output frequencies, ranging from 10.91MHz to 2.5GHz.

The device outputs are divided into four output banks. Each bank supports conversion of the input frequency to a different output frequency: one independent or integer related output frequency on Bank D (QD[0:1]) and three more integer related frequencies on Bank A (QA[0:3]), Bank B (QB[0:3]), and Bank C (QC[0:1]). All outputs within a bank will have the same frequency.

The device is programmable through an I²C serial interface by an external processor, or loaded through an external I²C EEPROM or control input pins.

Pin versus Register Control

The 8V49NS1412 can be configured via input control pins and/or over an I²C serial port. The pins/registers used to control each function are shown in Table 2. Each function is controlled at power-up via the control input pins. Access over the I²C serial port can change each function individually via register control. This allows for any mixture of register or pin control; however, any of the indicated functions can only be controlled by a register or by a pin at any given time, but not by both. Use of register control allows access to a wider range of configuration options, but values are lost on power-down. If the output bank or PLL is controlled by control input pins (at power-up or through Control Select bit), corresponding register values remain unchanged and have no impact on device functions.

Table 2. Control of Specific Functions

| Function | Control Select Bit | Control Input Pins | Register Fields Affected |
|------------------------------------|--------------------|--------------------|---|
| Prescaler and PLL Feedback Divider | FIN_CTL | FIN[1:0] | PS[5:0], FDP, M[8:0] |
| Bank A – Divider and Output Type | NA_CTL | NA[1:0] | NA_DIV, PD_A, PD_QAx, STY_QAx, AMP_QAx[1:0] |
| Bank B – Divider and Output Type | NB_CTL | NB[1:0] | NB_DIV, PD_B, PD_QBx, STY_QBx, AMP_QBx[1:0] |
| Bank C – Divider and Output Type | NC_CTL | NC[1:0] | NC_DIV, PD_C, PD_QCx, STY_QCx, AMP_QCx[1:0] |
| Bank D – Divider and Output Type | ND_CTL | ND[1:0] | ND[5:0], ND_FINT[3:0], ND_FRAC[23:0], ND_DIVF[1:0], ND_SRC, ND_DIV, PD_D, PD_QDx, STY_QD0, AMP_QD0[1:0] |

Changes to the control pins while the part is active are allowed, but limited, and cannot be guaranteed a glitch-free output transition. During the state transition of the control pins, the output phase alignment (synchronization) may be lost and Bank D outputs in Fractional Mode (FOD) may be unavailable. If I²C registers are accessible, then assertion of the INIT_CLK bit or powering down and then powering up the part will restore phase alignment and activate the Fractional output frequency.

Glitch-free operation can be performed by disabling the outputs using the I²C-accessible registers, then re-enabling once changes are completed.

Any change to the output dividers performed over the I²C interface must be followed by an assertion of the INIT_CLK register bit to force the loading of the new divider values, as well as to synchronize the output dividers.

Input Clock Selection (REF_SEL)

The 8V49NS1412 must be provided with an input reference frequency either from its crystal input pins (OSCI, OSCO), or its reference clock input pins (CLK, nCLK). The REF_SEL input pin controls which source is used.

The crystal input on the 8V49NS1412 can be driven by a parallel-resonant, fundamental mode crystal with a frequency of 10MHz to 50MHz. The crystal input also supports being driven by a single-ended crystal oscillator or reference clock, but only a frequency from 10MHz to 50MHz may be used on these pins.

The reference clock input accepts clocks with frequencies from 5MHz to 1GHz. The input can accept LVPECL, LVDS, LVHSTL, HCSL or LVCMOS inputs using 2.5V or 3.3V logic levels as shown in [Applications Information](#).

Prescaler and PLL Configuration

When the input frequency (f_{IN}), whether generated by a crystal or clock input is known, and the desired PLL operating frequency has been determined, several constraints need to be met:

- The Phase / Frequency Detector operating frequency (f_{PFD}) must be within the specified limits shown in [Table 31](#). This is controlled by selecting the doubler (FDP) or an appropriate prescaler (PS) value, but not both. If multiple values are possible, a higher f_{PFD} will provide better phase noise performance.
- The VCO operating frequency (f_{VCO}) must be within the specified limits shown in [Table 31](#). This is controlled by selecting an appropriate PLL feedback divider (M) value. Note, it may be necessary to select a different prescaler value if the limits cannot be met by the available values of M. It may also be necessary to select an appropriate input frequency value.

Several preset configurations can be selected directly from the FIN[1:0] control input pins. These configurations are based on a particular input frequency f_{IN} and a particular f_{VCO} (see [Table 3](#)). These selections apply whether the input frequency is provided from the crystal or reference clock inputs

Table 3. Input Selection Control

| FIN[1] | FIN[0] | f_{IN} (MHz) | f_{VCO} (MHz) |
|--------|-----------------------|----------------|-----------------|
| High | High | 38.88 | 2488.32 |
| High | Middle ^[a] | 38.4 | 2457.6 |
| High | Low | 31.25 | 2500 |
| Middle | High | 312.5 | 2500 |
| Middle | Middle | 125 | 2500 |
| Middle | Low | 156.25 | 2500 |
| Low | High | 100 | 2500 |
| Low | Middle | 25 | 2500 |
| Low | Low | 50 | 2500 |

[a] A "middle" voltage level is defined in [Table 24](#). Leaving the input pin open will also generate this level via a weak internal resistor network.

Alternatively the user can directly access the registers for M, FDP, and PS over the serial interface for a wider range of options (see [Table 4](#)).

Inputs do not support transmission of spread-spectrum clocking sources. Since this family of devices is intended for high-performance applications, it will assume input reference sources to have stabilities of +100ppm or greater.

Table 4. PLL Frequency Control Examples

| f_{IN} (MHz) | PS | FDP | f_{PFD} (MHz) | M | PLL Operating Frequency (MHz) |
|----------------|----|-----|-----------------|----|-------------------------------|
| 25 | 1 | 2 | 50 | 50 | 2500 |
| 39.0625 | 1 | 2 | 78.125 | 32 | 2500 |
| 50 | 1 | 2 | 100 | 25 | 2500 |
| 100 | 1 | 1 | 100 | 25 | 2500 |
| 125 | 1 | 1 | 125 | 20 | 2500 |
| 156.25 | 1 | 1 | 156.25 | 16 | 2500 |
| 200 | 2 | 1 | 100 | 25 | 2500 |
| 250 | 2 | 1 | 125 | 20 | 2500 |
| 312.5 | 2 | 1 | 156.25 | 16 | 2500 |
| 400 | 4 | 1 | 100 | 25 | 2500 |
| 500 | 4 | 1 | 125 | 20 | 2500 |
| 625 | 4 | 1 | 156.25 | 16 | 2500 |
| 19.44 | 1 | 2 | 38.88 | 64 | 2488.32 |
| 38.88 | 1 | 2 | 77.76 | 32 | 2488.32 |
| 38.4 | 1 | 2 | 76.8 | 32 | 2457.6 |

PLL Loop Bandwidth

The 8V49NS1412 PLL requires external loop components (resistor and capacitors) connecting in between the ICP and LFF pins. The PLL loop bandwidth generally depends on the loop components, charge pump current, PFD frequency, and VCO gain.

Output Divider Frequency Sources

Output dividers associated with Banks A, B, and C take their input frequency directly from the PLL. Bank D also has the option to bypass the input frequency (after mux) directly to the output.

Integer Output Dividers (Banks A, B, C, and D)

The 8V49NS1412 supports four integer output dividers: one per output bank. Each integer output divider block independently supports one of several divide ratios as shown in their respective register descriptions (Table 14, Table 15, Table 16 or Table 17). Selected divide ratios can be chosen directly from the control input pins for that particular output bank. The remaining ratios can only be selected via the serial interface. Bank D can choose whether to use the integer divider or a separate fractional divider to generate the output frequency.

Output frequency examples are shown in Table 5 for the minimum f_{VCO} (2400MHz), the maximum f_{VCO} (2500MHz), and two additional common VCO frequencies. With appropriate input frequencies and configuration selections, any f_{VCO} and f_{OUT} between the minimum and maximum can be generated.

Table 5. Integer Output Divider Control Examples

| Divide Ratio | f_{OUT} (MHz) | | | |
|--------------|----------------------------|------------------------------|-------------------------------|----------------------------|
| | $f_{VCO} = 2400\text{MHz}$ | $f_{VCO} = 2457.6\text{MHz}$ | $f_{VCO} = 2488.32\text{MHz}$ | $f_{VCO} = 2500\text{MHz}$ |
| 1 | 2400 | 2457.6 | 2488.32 | 2500 |
| 2 | 1200 | 1228.8 | 1244.16 | 1250 |
| 4 | 600 | 614.4 | 622.08 | 625 |
| 5 | 480 | 491.52 | 497.664 | 500 |
| 6 | 400 | 409.6 | 414.72 | 416.667 |
| 8 | 300 | 307.2 | 311.04 | 312.5 |
| 9 | 266.667 | 273.07 | 276.48 | 277.78 |
| 10 | 240 | 245.76 | 248.832 | 250 |
| 12 | 200 | 204.8 | 207.36 | 208.333 |
| 16 | 150 | 153.6 | 155.52 | 156.25 |
| 18 | 133.333 | 136.533 | 138.24 | 138.889 |
| 20 | 120 | 122.88 | 124.416 | 125 |
| 25 | 96 | 98.3 | 99.53 | 100 |
| 32 | 75 | 76.8 | 77.76 | 78.125 |
| 36 | 66.667 | 68.267 | 69.12 | 69.444 |
| 40 | 60 | 61.44 | 62.208 | 62.5 |
| 50 | 48 | 49.152 | 49.766 | 50 |
| 64 | 37.5 | 38.4 | 38.88 | 39.063 |
| 72 | 33.333 | 34.133 | 34.56 | 34.722 |
| 80 | 30 | 30.72 | 31.104 | 31.25 |
| 100 | 24 | 24.576 | 24.883 | 25 |
| 128 | 18.75 | 19.2 | 19.44 | 19.531 |
| 160 | 15 | 15.36 | 15.552 | 15.625 |
| 200 | 12 | 12.29 | 12.44 | 12.5 |
| 220 | 10.91 | 11.17 | 11.31 | 11.36 |

Fractional Output Divider (Bank D)

For the fractional output divider in Bank D, the output divide ratio is given by:

$$f_{OUT} = \frac{f_{VCO}}{2 \times \left(FINT + \frac{FRAC}{2^{24}} \right) \times (FDIV)}$$

Where,

- FINT = Integer Part: 5, 6, ..., $(2^4 - 1)$ – given by ND_FINT[3:0]
- FRAC = Fractional Part: 0, 1, 2, ..., $(2^{24} - 1)$ – given by ND_FRAC[23:0]
- FDIV = Post-divider: 1, 2 or 4 – given by ND_DIVF[1:0]

This provides a frequency range of 20 to 250MHz

Output Drivers

Each of the four output banks are provided with pin or register-controlled output drivers. Differential outputs can be individually selected as LVDS, LVPECL, or POWER-DOWN. When powered-down, both outputs of the differential output pair will drive a logic-high level, and the single-ended QD1 output will be in a High-Impedance state.

The differential outputs can individually choose one of several different output voltage swings: 350mV, 500mV, or 750mV – measured single-ended.

Note, under pin-control, all differential outputs within an output bank will assume the same configuration. Pin-control does not allow configuration of individual outputs within a bank.

Pin Control of the Output Frequencies and Protocols

For pin-control settings, see Table 6 to Table 10. All of the output frequencies assume $f_{VCO} = 2500\text{MHz}$. With different f_{VCO} configurations, the pins can still be used to select the indicated divide ratios for each bank, but the f_{OUT} will be different.

The control pins do not affect the internal register values, but act directly on the output structures. Register values will not change to match the control input pin selections.

Each output bank can be powered-up/down and enabled/disabled by register bits. In the disabled state, an output will drive a logic low level. The default state is all outputs enabled. Pin-control does not require register access to enable the outputs. Additionally, individual outputs within a bank can be powered up/down by register bits only.

Table 6. Definition of Output Disabled / Power-Down^[a]

| Output Conditions | $Q_{MN}^{[b]}$ | $nQ_{MN}^{[c]}$ | QD1 |
|--|----------------|-----------------|----------------|
| DISABLED (register-control only) | LOW | HIGH | LOW |
| POWER-DOWN (pin-control or register-control) | HIGH | HIGH | High-Impedance |

[a] Do not terminate the differential outputs when DISABLED or POWER-DOWN.

[b] Q_{MN} refers to output pins QA[0:3], QB[0:3], QC[0:1], and QD0.

[c] nQ_{MN} refers to output pins nQA[0:3], nQB[0:3], nQC[0:1], and nQD0.

Table 7. Bank A Divider/Driver Pin-Control (3-level Control Signals)

| NA[1] | NA[0] | Output Type | Divide Ratio | f _{OUT} (MHz) |
|--------|--------|--|--------------|------------------------|
| Low | Low | LVPECL ^[a] | 16 | 156.25 |
| Low | Middle | LVPECL | 20 | 125 |
| Low | High | LVPECL | 25 | 100 |
| Middle | Low | LVPECL | 100 | 25 |
| Middle | Middle | POWER-DOWN ^[b] | - | - |
| Middle | High | LVDS ^[c] | 16 | 156.25 |
| High | Low | LVDS | 20 | 125 |
| High | Middle | LVPECL | 8 | 312.5 |
| High | High | Loading the configuration from EEPROM ^[d] | | |

[a] Under pin control, all outputs of the bank are LVPECL using 750mV output swing.

[b] No active receivers should be connected to QA outputs.

[c] Under pin control, all outputs of the bank are LVDS using 350mV output swing.

[d] When the configuration is loading from an external EEPROM (NA[1] and NA[0] pins are HIGH), pins NB[1] and NB[0] act as address pins for EEPROM (for more information, see [I²C Master Mode Operation and Device Start-up Behavior](#)).

Table 8. Bank B Divider/Driver Pin-Control (3-level Control Signals)^[a]

| NB[1] | NB[0] | Output Type | Divide Ratio | f _{OUT} (MHz) |
|--------|--------|---------------------------|--------------|------------------------|
| Low | Low | LVPECL ^[b] | 16 | 156.25 |
| Low | Middle | LVPECL | 20 | 125 |
| Low | High | LVPECL | 25 | 100 |
| Middle | Low | LVPECL | 100 | 25 |
| Middle | Middle | POWER-DOWN ^[c] | - | - |
| Middle | High | LVDS ^[d] | 16 | 156.25 |
| High | Low | LVDS | 20 | 125 |
| High | Middle | LVPECL | 8 | 312.5 |
| High | High | LVPECL | 50 | 50 |

[a] When the configuration is loading from an external EEPROM (NA[1] and NA[0] pins are HIGH), pins NB[1] and NB[0] act as address pins for EEPROM (for more information, see [I²C Master Mode Operation and Device Start-up Behavior](#)).

[b] Under pin control, all outputs of the bank are LVPECL using 750mV output swing.

[c] No active receivers should be connected to QB outputs.

[d] Under pin control, all outputs of the bank are LVDS using 350mV output swing.

Table 9. Bank C Divider/Driver Pin-Control (3-level Control Signals)

| NC[1] | NC[0] | Output Type | Divide Ratio | f _{OUT} (MHz) |
|--------|--------|---------------------------|--------------|------------------------|
| Low | Low | LVPECL ^[a] | 8 | 312.5 |
| Low | Middle | LVPECL | 16 | 156.25 |
| Low | High | LVPECL | 20 | 125 |
| Middle | Low | LVPECL | 100 | 25 |
| Middle | Middle | POWER-DOWN ^[b] | | - |
| Middle | High | LVDS ^[c] | 20 | 125 |
| High | Low | LVDS | 25 | 100 |
| High | Middle | LVPECL | 50 | 50 |
| High | High | LVDS | 16 | 156.25 |

[a] Under pin control, all outputs of the bank are LVPECL using 750mV output swing.

[b] No active receivers should be connected to QC outputs.

[c] Under pin control, all outputs of the bank are LVDS using 350mV output swing.

Table 10. Bank D Divider/Driver Pin-Control (3-level Control Signals)

| ND[1] | ND[0] | QD0 Output Type | QD1 Output Type | Divide Ratio | f _{OUT} (MHz) |
|--------|--------|---------------------------|-----------------|----------------------|--------------------------------|
| Low | Low | LVPECL ^[a] | LVC MOS | 18.75 ^[b] | 133.333 |
| Low | Middle | LVPECL | LVC MOS | 37.5 ^[b] | 66.667 |
| Low | High | LVPECL | High-Impedance | 11.76 ^[b] | 212.5 |
| Middle | Low | Reserved | Reserved | Reserved | Reserved |
| Middle | Middle | POWER-DOWN ^[c] | High-Impedance | - | - |
| Middle | High | LVPECL | LVC MOS | 25 | 100 |
| High | Low | LVPECL | LVC MOS | 100 | 25 |
| High | Middle | LVPECL | LVC MOS | 20 | 125 |
| High | High | LVPECL | LVC MOS | 1 | f _{IN} ^[d] |

[a] Under pin control, all outputs of the bank are LVPECL using 750mV output swing.

[b] Generated from a fractional divider.

[c] No active receivers should be connected to QD0 outputs.

[d] Bypasses the input frequency directly to the output.

Device Start-up and Reset Behavior

The 8V49NS1412 has an internal power-on reset (POR) circuit. The POR circuit will remain active for a maximum of 175msec after device power-up when recommended CR (pin 25) value (1.0uF) used. For faster power-up to Lock Time, a minimum CR value of 0.1uF can be used.

While in the reset state (POR active), the device will operate as follows:

1. All registers will return to and be held in their default states as indicated in the applicable register description.
2. All internal state machines will be in their reset conditions.
3. The serial interface will not respond to read or write cycles.
4. Lock status will be cleared.

Upon the internal POR circuit expiring, the device will exit reset and begin self-configuration.

Self-configuration initiates the loading of appropriate values indicated by the control input pins, and the default values into the registers indicated in the register descriptions.

When the NA[1] and NA[0] pins are set up to HIGH, the device will load the configuration from an external I²C EEPROM at a defined address (for more information, see [I²C Master Mode Operation and Device Start-up Behavior](#)). Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock the PLL to the input frequency, if available. Once the PLL is locked, all of the outputs will be synchronized.

Serial Control Port Description

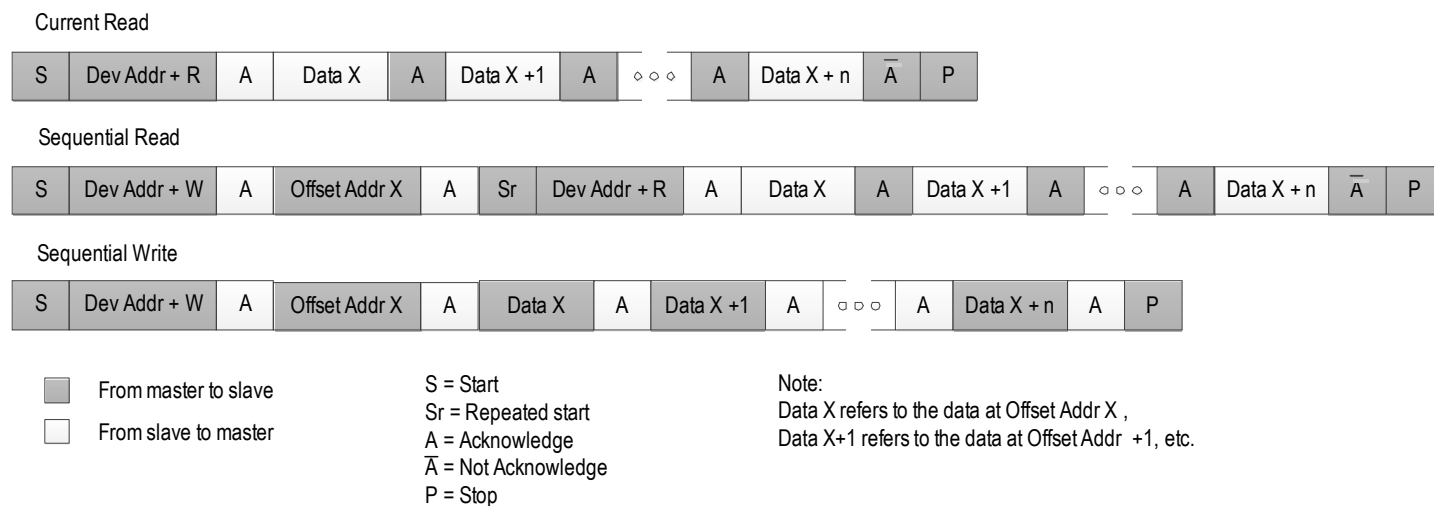
Serial Control Port Configuration Description

The 8V49NS1412 has a serial control port that can respond as a slave in an I²C compatible configuration at a base address of 1101100b, to allow access to any of the internal registers for device programming or examination of internal status. In addition, the device can become a master only in order to read the initial register configuration from a serial EEPROM on the I²C bus.

I²C Mode Operation

The I²C interface is designed to fully support v1.2 of the *I2C Specification* for Fast mode operation. The 8V49NS1412 acts as a slave device on the I²C bus at 400kHz using a fixed base address of 1101100b. The interface accepts byte-oriented block write and block read operations. One address byte specifies the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

Figure 3. I²C Slave Read and Write Cycle Sequencing


I²C Master Mode Operation and Device Start-up Behavior

The 8V49NS1412 can load the device configuration from an external EEPROM. During start-up if the configuration pins NA[1] and NA[0] are set to HIGH, or if after start-up they transition to HIGH, the 8V49NS1412 acts as a master on the I²C bus and initiates reading its configuration from an external I²C EEPROM device. Only a block read cycle is supported.

The expected external EEPROM address is pin configurable and depends on the setting of the NB[1] and NB[0] pins. All the address pins of the external EEPROM device must be configured to match the expected EEPROM Address of the 8V49NS1412. The EEPROM address configuration of the 8V49NS1412 is displayed in [Table 11](#).

Table 11. Expected EEPROM Address Settings

| NB[1] | NB[0] | Expected EEPROM Address |
|--------|--------|-------------------------|
| LOW | LOW | 0x50 |
| LOW | MIDDLE | |
| MIDDLE | LOW | |
| MIDDLE | MIDDLE | |
| LOW | HIGH | 0x52 |
| MIDDLE | HIGH | |
| HIGH | LOW | 0x54 |
| HIGH | MIDDLE | |
| HIGH | HIGH | 0x56 |

The 8V49NS1412 loads 82 bytes of data from the external EEPROM device. The first 81 bytes of data contain the device configuration. The last byte (address 0x51) is the location of the CRC checksum. If the CRC is incorrect, the data still loads into the registers but a checksum error is flagged in bit 0 of the 'd59 status register.

The speed of the Master I²C clock is from 200 to 400kHz. Renesas recommends the use of an external EEPROM device with an appropriate speed to match the speed of the 8V49NS1412.

Bit 4 of the 'd59 status register is set to 1 if an EEPROM read is triggered based on the pin configuration until the end of this EEPROM read (then it will go back to 0). Bit 2 of the 'd59 status register is set to 1 after an EEPROM read based on the pin configuration has been completed. These two bits remain 0 for other pin configurations when an EEPROM read is never requested.

As an I²C bus master, the 8V49NS1412 supports the following functions:

- 7-bit addressing mode
- Validation of the read block via CCITT-8 CRC check against the value stored in the last byte (0x51) of the EEPROM
- Support for 400kHz operation without speed negotiation
- Support for 1-byte addressing mode
- Fixed-period cycle response timer to prevent permanently hanging the I²C bus
- Read will abort with a status error (bit 1 = 1 in the 'd59 register) if one of the following conditions occurs:
 - Slave NACK
 - Arbitration fail
 - Collision during address phase
 - Slave response timeout

The 8V49NS1412 does not support the following functions:

- I²C general call
- Slave clock stretching
- I²C start byte protocol
- EEPROM chaining
- CBUS compatibility
- Responding to its own slave address when acting as a master

Register Descriptions

Table 12. Register Blocks

| Register Ranges Offset (Hex) | Register Block Description |
|------------------------------|-------------------------------------|
| 00–08 | Prescaler and PLL Control Registers |
| 09–0F | Reserved ^[a] |
| 10–17 | Bank A Control Registers |
| 18–1F | Bank B Control Registers |
| 20–27 | Bank C Control Registers |
| 28–31 | Bank D Control Registers |
| 32–37 | Reserved |
| 38–3A | Reserved |
| 3B | EEPROM Reading Status Register |
| 3C | Reserved |
| 3D–40 | Device Control Registers |
| 41–4B | Reserved |
| 4C–4F | Reserved |
| 50–FF | Reserved |

[a] Reserved registers should not be written to and have indeterminate read values.

Table 13. Prescaler and PLL Control Register Bit Field Locations and Descriptions

| Prescaler and PLL Control Register Block Field Locations | | | | | | | | |
|--|--------|------|---------|---------|----|----|---------|---------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00 | Rsvd | Rsvd | PS[5:0] | | | | | |
| 01 | Rsvd | | | | | | | FDP |
| 02 | Rsvd | | | | | | FIN_CTL | OSC_LOW |
| 03 | Rsvd | | | | | | | |
| 04 | Rsvd | | | | | | | M[8] |
| 05 | M[7:0] | | | | | | | |
| 06 | Rsvd | | | | | | | |
| 07 | Rsvd | | | | | | | |
| 08 | Rsvd | | | CP[4:0] | | | | |

| Prescaler and PLL Control Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| PS[5:0] | R/W | 000000b | Prescaler – scales input frequency by the value: 00h = Reserved 01h–3Fh = Divide by the value used (e.g. 04 = divide-by-4) Note: When FDP = 1, Prescaler values are ignored and have no impact on device functions. |
| FDP | R/W | 1b | Input frequency doubler: 0 = Disabled 1 = Enabled |
| FIN_CTL | R/W | 0b | Prescaler and PLL configuration control: 0 = PS, FDP, and M settings determined by FIN[1:0] control pins 1 = PS, FDP, and M settings determined by register settings over I ² C |
| OSC_LOW | R/W | 0b | Crystal oscillator gain control selection: 0 = Normal gain for crystal frequencies of 25MHz and up 1 = Low gain for crystal frequencies less than 25MHz |
| M[8:0] | R/W | 019h | PLL Feedback divider ratio: 000h–003h = Reserved (do not use) 004h–1FFh = Divide the value used (e.g. 04 = divide-by-4) |
| CP[4:0] | R/W | 11001b | PLL Charge Pump Current control: $I_{CP} = 200\mu A \times (CP[4:0] + 1)$ Maximum charge pump current is 6.4mA. Default setting is 5.2mA: $((25 + 1) \times 200\mu A)$. |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 14. Bank A Control Register Bit Field Locations and Descriptions

| Bank A Control Register Block Field Locations | | | | | | | | |
|---|--------|------|---------|----|----|---------|--------------|--------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 10 | Rsvd | | NA[5:0] | | | | | |
| 11 | Rsvd | | | | | | | |
| 12 | PD_A | Rsvd | | | | | | NA_CTL |
| 13 | Rsvd | | | | | | | |
| 14 | PD_QA0 | Rsvd | | | | STY_QA0 | AMP_QA0[1:0] | |
| 15 | PD_QA1 | Rsvd | | | | STY_QA1 | AMP_QA1[1:0] | |
| 16 | PD_QA2 | Rsvd | | | | STY_QA2 | AMP_QA2[1:0] | |
| 17 | PD_QA3 | Rsvd | | | | STY_QA3 | AMP_QA3[1:0] | |

| Bank A Control Register Block Field Descriptions | | | |
|--|------------|---------------|--|
| Bit Field Name ^[a] | Field Type | Default Value | Description |
| NA[5:0] | R/W | 0Dh | Divider ratio for Bank A: Any changes to this register do not take effect until the INIT_CLK register bit is toggled. |
| | | | 00 0000b = Reserved |
| | | | 00 0001b = ÷1 |
| | | | 00 0010b = ÷2 |
| | | | 00 0011b = ÷3 |
| | | | 00 0100b = ÷4 |
| | | | 00 0101b = ÷5 |
| | | | 00 0110b = ÷6 |
| | | | 00 0111b = ÷8 |
| | | | 00 1000b = ÷9 |
| | | | 00 1001b = ÷10 |
| | | | 00 1010b = ÷12 |
| | | | 00 1011b = ÷14 |
| | | | 00 1100b = ÷15 |
| | | | 00 1101b = ÷16 |
| | | | 00 1110b = ÷18 |
| | | | 00 1111b = ÷20 |
| | | | 01 0000b = ÷21 |
| | | | 01 0001b = ÷22 |
| | | | 01 0010b = ÷24 |
| | | | 01 0011b = ÷25 |
| | | | 01 0100b = ÷27 |
| | | | 01 0101b = ÷28 |
| | | | 01 0110b = ÷30 |
| | | | 01 0111b = ÷32 |
| | | | 01 1000b = ÷33 |
| | | | 01 1001b = ÷35 |
| | | | 01 1010b = ÷36 |
| | | | 01 1011b = ÷40 |
| | | | 01 1100b = ÷42 |
| | | | 01 1101b = ÷44 |
| | | | 01 1110b = ÷45 |
| | | | 01 1111b = ÷48 |
| | | | 10 0000b = ÷50 |
| | | | 10 0001b = ÷54 |
| | | | 10 0010b = ÷55 |
| | | | 10 0011b = ÷56 |
| | | | 10 0100b = ÷60 |
| | | | 10 0101b = ÷64 |
| | | | 10 0110b = ÷66 |
| | | | 10 0111b = ÷70 |
| | | | 10 1000b = ÷72 |
| | | | 10 1001b = ÷80 |
| | | | 10 1010b = ÷84 |
| | | | 10 1011b = ÷88 |
| | | | 10 1100b = ÷90 |
| | | | 10 1101b = ÷96 |
| | | | 10 1110b = ÷100 |
| | | | 10 1111b = ÷108 |
| | | | 11 0000b = ÷110 |
| | | | 11 0001b = ÷112 |
| | | | 11 0010b = ÷120 |
| | | | 11 0011b = ÷128 |
| | | | 11 0100b = ÷132 |
| | | | 11 0101b = ÷140 |
| | | | 11 0110b = ÷144 |
| | | | 11 0111b = ÷160 |
| | | | 11 1000b = ÷176 |
| | | | 11 1001b = ÷180 |
| | | | 11 1010b = ÷200 |
| | | | 11 1011b = ÷220 |
| | | | 11 1100b = Reserved |
| | | | 11 1101b = Reserved |
| | | | 11 1110b = Reserved |
| | | | 11 1111b = Reserved |

| Bank A Control Register Block Field Descriptions | | | |
|--|------------|---------------|---|
| Bit Field Name ^[a] | Field Type | Default Value | Description |
| PD_A | R/W | 0b | Power-down Bank A: 0 = Bank A and all QA outputs powered and operate normally 1 = Bank A and all QA outputs powered down – no active receivers should be connected to QA outputs. When powering down the output bank, it is recommended to also write a 1 to the PD_QAx fields. |
| NA_CTL | R/W | 0b | Bank A configuration control: 0 = NA[5:0], PD_A, STY_Ax, and AMP_Ax[1:0] settings determined by NA[1:0] control pins 1 = NA[5:0], PD_A, STY_Ax, and AMP_Ax[1:0] settings determined by register settings over I ² C |
| PD_QAx | R/W | 0b | Power-down output QAx: 0 = QAx output powered and operates normally 1 = QAx output powered-down - no active receivers should be connected to the QAx output. |
| STY_QAx | R/W | 0b | Output style for output QAx: 0 = QAx is LVDS 1 = QAx is LVPECL |
| AMP_QAx[1:0] | R/W | 00b | Output amplitude for output QAx (measured single-ended): 00 = 350mV 01 = 500mV 10 = 750mV 11 = Reserved |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

[a] Where x = 0, 1, 2, or 3.

Table 15. Bank B Control Register Bit Field Locations and Descriptions

| Bank B Control Register Block Field Locations | | | | | | | | |
|---|--------|------|---------|----|----|---------|--------------|--------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 18 | Rsvd | | NB[5:0] | | | | | |
| 19 | Rsvd | | | | | | | |
| 1A | PD_B | Rsvd | | | | | | NB_CTL |
| 1B | Rsvd | | | | | | | |
| 1C | PD_QB0 | Rsvd | | | | STY_QB0 | AMP_QB0[1:0] | |
| 1D | PD_QB1 | Rsvd | | | | STY_QB1 | AMP_QB1[1:0] | |
| 1E | PD_QB2 | Rsvd | | | | STY_QB2 | AMP_QB2[1:0] | |
| 1F | PD_QB3 | Rsvd | | | | STY_QB3 | AMP_QB3[1:0] | |

| Bank B Control Register Block Field Descriptions | | | |
|--|------------|---------------|--|
| Bit Field Name ^[a] | Field Type | Default Value | Description |
| NB[5:0] | R/W | 0Dh | Divider ratio for Bank B: Any changes to this register do not take effect until the INIT_CLK register bit is toggled. |
| | | | 00 0000b = Reserved |
| | | | 00 0001b = ÷1 |
| | | | 00 0010b = ÷2 |
| | | | 00 0011b = ÷3 |
| | | | 00 0100b = ÷4 |
| | | | 00 0101b = ÷5 |
| | | | 00 0110b = ÷6 |
| | | | 00 0111b = ÷8 |
| | | | 00 1000b = ÷9 |
| | | | 00 1001b = ÷10 |
| | | | 00 1010b = ÷12 |
| | | | 00 1011b = ÷14 |
| | | | 00 1100b = ÷15 |
| | | | 00 1101b = ÷16 |
| | | | 00 1110b = ÷18 |
| | | | 00 1111b = ÷20 |
| | | | 01 0000b = ÷21 |
| | | | 01 0001b = ÷22 |
| | | | 01 0010b = ÷24 |
| | | | 01 0011b = ÷25 |
| | | | 01 0100b = ÷27 |
| | | | 01 0101b = ÷28 |
| | | | 01 0110b = ÷30 |
| | | | 01 0111b = ÷32 |
| | | | 01 1000b = ÷33 |
| | | | 01 1001b = ÷35 |
| | | | 01 1010b = ÷36 |
| | | | 01 1011b = ÷40 |
| | | | 01 1100b = ÷42 |
| | | | 01 1101b = ÷44 |
| | | | 01 1110b = ÷45 |
| | | | 01 1111b = ÷48 |
| | | | 10 0000b = ÷50 |
| | | | 10 0001b = ÷54 |
| | | | 10 0010b = ÷55 |
| | | | 10 0011b = ÷56 |
| | | | 10 0100b = ÷60 |
| | | | 10 0101b = ÷64 |
| | | | 10 0110b = ÷66 |
| | | | 10 0111b = ÷70 |
| | | | 10 1000b = ÷72 |
| | | | 10 1001b = ÷80 |
| | | | 10 1010b = ÷84 |
| | | | 10 1011b = ÷88 |
| | | | 10 1100b = ÷90 |
| | | | 10 1101b = ÷96 |
| | | | 10 1110b = ÷100 |
| | | | 10 1111b = ÷108 |
| | | | 11 0000b = ÷110 |
| | | | 11 0001b = ÷112 |
| | | | 11 0010b = ÷120 |
| | | | 11 0011b = ÷128 |
| | | | 11 0100b = ÷132 |
| | | | 11 0101b = ÷140 |
| | | | 11 0110b = ÷144 |
| | | | 11 0111b = ÷160 |
| | | | 11 1000b = ÷176 |
| | | | 11 1001b = ÷180 |
| | | | 11 1010b = ÷200 |
| | | | 11 1011b = ÷220 |
| | | | 11 1100b = Reserved |
| | | | 11 1101b = Reserved |
| | | | 11 1110b = Reserved |
| | | | 11 1111b = Reserved |

| Bank B Control Register Block Field Descriptions | | | |
|--|------------|---------------|---|
| Bit Field Name ^[a] | Field Type | Default Value | Description |
| PD_B | R/W | 0b | Power-down Bank B: 0 = Bank B and all QB outputs powered and operate normally 1 = Bank B and all QB outputs powered down – no active receivers should be connected to QB outputs. When powering down the output bank, it is recommended to also write a 1 to the PD_QBx fields. |
| NB_CTL | R/W | 0b | Bank B configuration control: 0 = NB[5:0], PD_B, STY_Bx, and AMP_Bx[1:0] settings determined by NB[1:0] control pins 1 = NB[5:0], PD_B, STY_Bx, and AMP_Bx[1:0] settings determined by register settings over I ² C |
| PD_QBx | R/W | 0b | Power-down output QBx: 0 = QBx output powered and operates normally. 1 = QBx output powered down – no active receivers should be connected to the QBx output. |
| STY_QBx | R/W | 0b | Output style for output QBx: 0 = QBx is LVDS 1 = QBx is LVPECL |
| AMP_QBx[1:0] | R/W | 00b | Output amplitude for output QBx (measured single-ended): 00 = 350mV 01 = 500mV 10 = 750mV 11 = Reserved |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

[a] Where x = 0, 1, 2, or 3.

Table 16. Bank C Control Register Bit Field Locations and Descriptions

| Bank C Control Register Block Field Locations | | | | | | | | |
|---|--------|------|---------|----|----|---------|--------------|--------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 20 | Rsvd | | NC[5:0] | | | | | |
| 21 | Rsvd | | | | | | | |
| 22 | PD_C | Rsvd | | | | | | NC_CTL |
| 23 | Rsvd | | | | | | | |
| 24 | PD_QC0 | Rsvd | | | | STY_QC0 | AMP_QC0[1:0] | |
| 25 | PD_QC1 | Rsvd | | | | STY_QC1 | AMP_QC1[1:0] | |

| Bank C Control Register Block Field Descriptions | | | |
|--|------------|---------------|--|
| Bit Field Name ^[a] | Field Type | Default Value | Description |
| NC[5:0] | R/W | 0Dh | <p>Divider ratio for Bank C:</p> <p>Any changes to this register do not take effect until the INIT_CLK register bit is toggled.</p> |
| | | | <p>00 0000b = Reserved</p> <p>00 0001b = ÷1</p> <p>00 0010b = ÷2</p> <p>00 0011b = ÷3</p> <p>00 0100b = ÷4</p> <p>00 0101b = ÷5</p> <p>00 0110b = ÷6</p> <p>00 0111b = ÷8</p> <p>00 1000b = ÷9</p> <p>00 1001b = ÷10</p> <p>00 1010b = ÷12</p> <p>00 1011b = ÷14</p> <p>00 1100b = ÷15</p> <p>00 1101b = ÷16</p> <p>00 1110b = ÷18</p> <p>00 1111b = ÷20</p> <p>01 0000b = ÷21</p> <p>01 0001b = ÷22</p> <p>01 0010b = ÷24</p> <p>01 0011b = ÷25</p> <p>01 0100b = ÷27</p> <p>01 0101b = ÷28</p> |
| | | | 01 0110b = ÷30 |
| | | | 01 0111b = ÷32 |
| | | | 01 1000b = ÷33 |
| | | | 01 1001b = ÷35 |
| | | | 01 1010b = ÷36 |
| | | | 01 1011b = ÷40 |
| | | | 01 1100b = ÷42 |
| | | | 01 1101b = ÷44 |
| | | | 01 1110b = ÷45 |
| | | | 01 1111b = ÷48 |
| | | | 10 0000b = ÷50 |
| | | | 10 0001b = ÷54 |
| | | | 10 0010b = ÷55 |
| | | | 10 0011b = ÷56 |
| | | | 10 0100b = ÷60 |
| | | | 10 0101b = ÷64 |
| | | | 10 0110b = ÷66 |
| | | | 10 0111b = ÷70 |
| | | | 10 1000b = ÷72 |
| | | | 10 1001b = ÷80 |
| | | | 10 1010b = ÷84 |
| | | | 10 1011b = ÷88 |
| | | | 10 1100b = ÷90 |
| | | | 10 1101b = ÷96 |
| | | | 10 1110b = ÷100 |
| | | | 10 1111b = ÷108 |
| | | | 11 0000b = ÷110 |
| | | | 11 0001b = ÷112 |
| | | | 11 0010b = ÷120 |
| | | | 11 0011b = ÷128 |
| | | | 11 0100b = ÷132 |
| | | | 11 0101b = ÷140 |
| | | | 11 0110b = ÷144 |
| | | | 11 0111b = ÷160 |
| | | | 11 1000b = ÷176 |
| | | | 11 1001b = ÷180 |
| | | | 11 1010b = ÷200 |
| | | | 11 1011b = ÷220 |
| | | | 11 1100b = Reserved |
| | | | 11 1101b = Reserved |
| | | | 11 1110b = Reserved |
| | | | 11 1111b = Reserved |
| PD_C | R/W | 0b | <p>Power-down Bank C:</p> <p>0 = Bank C and all QC outputs powered and operate normally</p> <p>1 = Bank C and all QC outputs powered down – no active receivers should be connected to QC outputs. When powering down the output bank, it is recommended to also write a 1 to the PD_QCx fields.</p> |

| Bank C Control Register Block Field Descriptions | | | |
|--|------------|---------------|--|
| Bit Field Name ^[a] | Field Type | Default Value | Description |
| NC_CTL | R/W | 0b | Bank C configuration control: 0 = NC[5:0], PD_C, STY_Cx, and AMP_Cx[1:0] settings determined by NC[1:0] control pins 1 = NC[5:0], PD_C, STY_Cx, and AMP_Cx[1:0] settings determined by register settings over I ² C |
| PD_QCx | R/W | 0b | Power-down output QCx: 0 = QCx output powered and operates normally. 1 = QCx output powered down – no active receivers should be connected to the QCx output. |
| STY_QCx | R/W | 0b | Output style for output QCx: 0 = QCx is LVDS 1 = QCx is LVPECL |
| AMP_QCx[1:0] | R/W | 00b | Output amplitude for output QCx (measured single-ended): 00 = 350mV 01 = 500mV 10 = 750mV 11 = Reserved |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

[a] Where x = 0 or 1.

Table 17. Bank D Control Register Bit Field Locations and Descriptions

| Bank D Control Register Block Field Locations | | | | | | | | |
|---|----------------|------|---------|----|--------------|---------|--------------|--------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 28 | ND_FRAC[7:0] | | | | | | | |
| 29 | ND_FRAC[15:8] | | | | | | | |
| 2A | ND_FRAC[23:16] | | | | | | | |
| 2B | Rsvd | | | | ND_FINT[3:0] | | | |
| 2C | Rsvd | | ND[5:0] | | | | | |
| 2D | Rsvd | | | | ND_DIVF[1:0] | | ND_DIV | ND_SRC |
| 2E | PD_D | Rsvd | | | | | | ND_CTL |
| 2F | Rsvd | | | | | | | |
| 30 | PD_QD0 | Rsvd | | | | STY_QD0 | AMP_QD0[1:0] | |
| 31 | PD_QD1 | Rsvd | | | | | | |

| Bank D Control Register Block Field Descriptions | | | |
|--|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| ND_FRAC[23:0] | R/W | 600000h | Fractional portion of divider ratio for fractional divider Bank D: Fraction used in divide ratio = $ND_FRAC[23:0] / 2^{24}$ |
| ND_FINT[3:0] | R/W | 1001b | Integer portion of divider ratio for fractional divider Bank D: 0h–4h = Reserved 5h–Fh = Divide by the value used (e.g. 5 = divide-by-5) |

| Bank D Control Register Block Field Descriptions | | | |
|--|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| ND[5:0] | R/W | 0Dh | <p>Divider ratio for Bank D:</p> <p>Any changes to this register do not take effect until the INIT_CLK register bit is toggled.</p> |
| | | | <p>00 0000b = Reserved</p> <p>00 0001b = ÷1</p> <p>00 0010b = ÷2</p> <p>00 0011b = ÷3</p> <p>00 0100b = ÷4</p> <p>00 0101b = ÷5</p> <p>00 0110b = ÷6</p> <p>00 0111b = ÷8</p> <p>00 1000b = ÷9</p> <p>00 1001b = ÷10</p> <p>00 1010b = ÷12</p> <p>00 1011b = ÷14</p> <p>00 1100b = ÷15</p> <p>00 1101b = ÷16</p> <p>00 1110b = ÷18</p> <p>00 1111b = ÷20</p> <p>01 0000b = ÷21</p> <p>01 0001b = ÷22</p> <p>01 0010b = ÷24</p> <p>01 0011b = ÷25</p> <p>01 0100b = ÷27</p> <p>01 0101b = ÷28</p> |
| | | | <p>01 0110b = ÷30</p> <p>01 0111b = ÷32</p> <p>01 1000b = ÷33</p> <p>01 1001b = ÷35</p> <p>01 1010b = ÷36</p> <p>01 1011b = ÷40</p> <p>01 1100b = ÷42</p> <p>01 1101b = ÷44</p> <p>01 1110b = ÷45</p> <p>01 1111b = ÷48</p> <p>10 0000b = ÷50</p> <p>10 0001b = ÷54</p> <p>10 0010b = ÷55</p> <p>10 0011b = ÷56</p> <p>10 0100b = ÷60</p> <p>10 0101b = ÷64</p> <p>10 0110b = ÷66</p> <p>10 0111b = ÷70</p> <p>10 1000b = ÷72</p> <p>10 1001b = ÷80</p> <p>10 1010b = ÷84</p> |
| | | | <p>10 1011b = ÷88</p> <p>10 1100b = ÷90</p> <p>10 1101b = ÷96</p> <p>10 1110b = ÷100</p> <p>10 1111b = ÷108</p> <p>11 0000b = ÷110</p> <p>11 0001b = ÷112</p> <p>11 0010b = ÷120</p> <p>11 0011b = ÷128</p> <p>11 0100b = ÷132</p> <p>11 0101b = ÷140</p> <p>11 0110b = ÷144</p> <p>11 0111b = ÷160</p> <p>11 1000b = ÷176</p> <p>11 1001b = ÷180</p> <p>11 1010b = ÷200</p> <p>11 1011b = ÷220</p> <p>11 1100b = Reserved</p> <p>11 1101b = Reserved</p> <p>11 1110b = Reserved</p> <p>11 1111b = Reserved</p> |
| | | | Note: QD1 CMOS output should be powered down for output frequencies greater than the maximum listed for it in Table 31 . |
| ND_DIVF[1:0] | R/W | 00b | <p>Post-divider ratio for fractional divider for Bank D:</p> <p>00 = ÷1</p> <p>01 = ÷2</p> <p>10 = ÷4</p> <p>11 = Reserved</p> |
| ND_DIV | R/W | 0b | <p>Control which divider is used to provide output frequency for Bank D:</p> <p>0 = Integer divider D (ND configures this)</p> <p>1 = Fractional mode (ND_FINT, ND_FRAC, and ND_DIVF configure this)</p> |
| ND_SRC | R/W | 0b | <p>Output source selection for Bank D:</p> <p>0 = Bank D is driven from the integer or fractional divider as selected by ND_DIV</p> <p>1 = Bank D is driven from the input reference (after the mux)</p> |

| Bank D Control Register Block Field Descriptions | | | |
|--|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| PD_D | R/W | 0b | Power-down Bank D: 0 = Bank D and all QD outputs powered and operate normally 1 = Bank D and all QD outputs powered down – no active receivers should be connected to QD0 output. QD1 output is in High-Impedance. When powering down the output bank, it is recommended to also write a 1 to the PD_QDx fields. |
| ND_CTL | R/W | 0b | Bank D configuration control: 0 = ND[5:0], ND_FRAC[23:0], ND_FINT[3:0], ND_DIVF[1:0], ND_DIV, ND_SRC, PD_D, PD_QD1, STY_D0, and AMP_D0[1:0] settings determined by ND[1:0] control pins 1 = ND[5:0], ND_FRAC[23:0], ND_FINT[3:0], ND_DIVF[1:0], ND_DIV, ND_SRC, PD_D, PD_QD1, STY_D0, and AMP_D0[1:0] settings determined by register settings over I ² C |
| PD_QDx | R/W | 0b | Power-down output QDx: 0 = QD[0:1] outputs powered and operate normally. 1 = QD0 output powered down – no active receivers should be connected to the QD0 output, QD1 output is in High-Impedance. |
| STY_QD0 | R/W | 0b | Output style for output QD0: 0 = QD0 is LVDS 1 = QD0 is LVPECL |
| AMP_QD0[1:0] | R/W | 00b | Output amplitude for output QD0 (measured single-ended): 00 = 350mV 01 = 500mV 10 = 750mV 11 = Reserved |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 18. EEPROM Reading Status Register Bit Field Locations and Descriptions

| Device Control Register Block Field Locations | | | | | | | | |
|---|------|----|----|--------|------|---------|----------|--------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 3B | Rsvd | | | EE_ACT | Rsvd | EE_DONE | EE_ABORT | EE_CHK |

| EEPROM Reading Status Register Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| EE_ACT | R | - | 0 = EEPROM reading completed or has not started / been requested yet 1 = EEPROM reading is active |
| EE_DONE | R | - | 0 = EEPROM reading was never requested / did not complete 1 = EEPROM reading completed |
| EE_ABORT | R | - | 0 = EEPROM reading did not abort 1 = EEPROM reading aborted |
| EE_CHK | R | - | 0 = No checksum error was detected 1 = Checksum error was detected |
| Rsvd | R | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 19. Device Control Register Bit Field Locations and Descriptions

| Device Control Register Block Field Locations | | | | | | | | |
|---|----------|------|----|----|------|------|------|------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 3D | INIT_CLK | Rsvd | | | | | | |
| 3E | RELOCK | Rsvd | | | | | | |
| 3F | PB_CAL | Rsvd | | | | | | |
| 40 | Rsvd | | | | EN_A | EN_B | EN_C | EN_D |

| Device Control Register Block Field Descriptions | | | |
|--|--------------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| INIT_CLK | W/O ^[a] | 0b | Writing a 1 to this bit location will cause output dividers to be synchronized. This must be done every time a divider value is changed. This bit will auto-clear. |
| RELOCK | W/O ^[a] | 0b | Writing a 1 to this bit location will cause the PLL to re-lock. This bit will auto-clear. |
| PB_CAL | W/O ^[a] | 0b | Precision Bias Calibration: Setting this bit to 1 will start the calibration of an internal precision bias current source. The bias current is used as reference for outputs configured as LVDS and for as reference for the charge pump currents. This bit will auto-clear. |
| EN_A | R/W | 1b | Output Enable control for Bank A: 0 = Bank A outputs QA[0:3] disabled to logic-low state (QA _x = 0, nQA _x = 1) 1 = Bank A outputs QA[0:3] enabled |
| EN_B | R/W | 1b | Output Enable control for Bank B: 0 = Bank B outputs QB[0:3] disabled to logic-low state (QB _x = 0, nQB _x = 1) 1 = Bank B outputs QB[0:3] enabled |
| EN_C | R/W | 1b | Output Enable control for Bank C: 0 = Bank C outputs QC[0:1] disabled to logic-low state (QC _x = 0, nQC _x = 1) 1 = Bank C outputs QC[0:1] enabled |
| EN_D | R/W | 1b | Output Enable control for Bank D: 0 = Bank D outputs QD[0:1] disabled to logic-low state (QD ₀ = 0, nQD ₀ = 1, QD ₁ = 0) 1 = Bank D outputs QD[0:1] enabled Note: If Bank D is powered down via the PD_D bit or the QD1 output is powered down by the PD_QD1 bit, then QD1 will be in High-Impedance regardless of the state of this bit. |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

[a] These bits are read as 0. When a 1 is written to them, it will have the indicated effect and then self-clear back to 0.

Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the [DC Electrical Characteristics](#) or [AC Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 20. Absolute Maximum Ratings

| Item | Rating |
|--|--------------------------------|
| Supply Voltage, V_{CC} | 3.6V |
| Inputs, V_I OSCI Other Inputs | -0.5V to 3.6V -0.5V to 3.6V |
| Outputs, V_O (LVCMOS) | -0.5V to 3.6V |
| Outputs, I_O (LVPECL) Continuous Current Surge Current | 50mA 100mA |
| Outputs, I_O (LVDS) Continuous Current Surge Current | 50mA 100mA |
| Maximum Junction Temperature, t_{JMAX} | 125°C |
| Storage Temperature, T_{STG} | -65°C to 150°C |

Table 21. Input Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|----------------|----------------------------------|-----------------|---------|---------|---------|------|
| C_{IN} | Input Capacitance ^[a] | | | 3.5 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |
| R_{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |

[a] This specification does not apply to OSCI and OSCO pins.

Table 22. Output Characteristics

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Unit |
|-----------|------------------|------|-----------------------|---------|---------|---------|------|
| R_{OUT} | Output Impedance | LOCK | $V_{CC}^{[a]} = 3.3V$ | | 20 | | W |
| | | QD1 | | | 30 | | W |

[a] V_{CC} denotes V_{CC_SP} , V_{CCOD} .

DC Electrical Characteristics

Table 23. Power Supply DC Characteristics, $V_{CC_X}^{[a]} = V_{CCOX}^{[b]} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Unit |
|--------------------|------------------------------|----------------|--|---------|---------|---------|------|
| V_{CC_X} | Core Supply Voltage | | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA_X}^{[c]}$ | Analog Supply Voltage | | | 3.135 | 3.3 | 3.465 | V |
| V_{CCOX} | Output Supply Voltage | | | 3.135 | 3.3 | 3.465 | V |
| $I_{CC_X}^{[d]}$ | Core Supply Current | | | | 83 | 100 | mA |
| $I_{CCA_X}^{[e]}$ | Analog Supply Current | | | | 138 | 165 | mA |
| $I_{CCOA}^{[f]}$ | Bank A Output Supply Current | LVPECL | 350mV, all outputs enabled and terminated ^[g] | | 130 | 160 | mA |
| | | | 500mV, all outputs enabled and terminated ^[h] | | 143 | 175 | mA |
| | | | 750mV, all outputs enabled and terminated ^[i] | | 165 | 200 | mA |
| | | LVDS | 350mV, all outputs enabled and terminated ^[j] | | 83 | 96 | mA |
| | | | 500mV, all outputs enabled and terminated ^[j] | | 100 | 120 | mA |
| | | | 750mV, all outputs enabled and terminated ^[j] | | 129 | 152 | mA |
| | | LVPECL or LVDS | 350mV, divider and buffers disabled and unterminated | | 1 | 2 | mA |
| | | | 500mV, divider and buffers disabled and unterminated | | 1 | 2 | mA |
| | | | 750mV, divider and buffers disabled and unterminated | | 1 | 2 | mA |
| $I_{CCOB}^{[f]}$ | Bank B Output Supply Current | LVPECL | 350mV, all outputs enabled and terminated ^[g] | | 130 | 160 | mA |
| | | | 500mV, all outputs enabled and terminated ^[h] | | 143 | 175 | mA |
| | | | 750mV, all outputs enabled and terminated ^[i] | | 165 | 200 | mA |
| | | LVDS | 350mV, all outputs enabled and terminated ^[j] | | 83 | 96 | mA |
| | | | 500mV, all outputs enabled and terminated ^[j] | | 100 | 120 | mA |
| | | | 750mV, all outputs enabled and terminated ^[j] | | 129 | 152 | mA |
| | | LVPECL or LVDS | 350mV, divider and buffers disabled and unterminated | | 1 | 2 | mA |
| | | | 500mV, divider and buffers disabled and unterminated | | 1 | 2 | mA |
| | | | 750mV, divider and buffers disabled and unterminated | | 1 | 2 | mA |

Table 23. Power Supply DC Characteristics, $V_{CC_X}^{[a]} = V_{CCOX}^{[b]} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Unit |
|------------------|-----------------------------------|----------------|--|---------|---------|---------|------|
| $I_{CCOC}^{[f]}$ | Bank C Output Supply Current | LVPECL | 350mV, all outputs enabled and terminated ^[g] | | 80 | 98 | mA |
| | | | 500mV, all outputs enabled and terminated ^[h] | | 87 | 105 | mA |
| | | | 750mV, all outputs enabled and terminated ^[i] | | 98 | 120 | mA |
| | | LVDS | 350mV, all outputs enabled and terminated ^[j] | | 53 | 65 | mA |
| | | | 500mV, all outputs enabled and terminated ^[j] | | 64 | 75 | mA |
| | | | 750mV, all outputs enabled and terminated ^[j] | | 76 | 92 | mA |
| | | LVPECL or LVDS | 350mV, divider and buffers disabled and unterminated | | 1 | 2 | mA |
| | | | 500mV, divider and buffers disabled and unterminated | | 1 | 2 | mA |
| | | | 750mV, divider and buffers disabled and unterminated | | 1 | 2 | mA |
| $I_{CCOD}^{[f]}$ | Bank D Output Supply Current | LVPECL | 350mV, all outputs enabled and terminated ^[g] | | 82 | 100 | mA |
| | | | 500mV, all outputs enabled and terminated ^[h] | | 84 | 105 | mA |
| | | | 750mV, all outputs enabled and terminated ^[i] | | 90 | 112 | mA |
| | | LVDS | 350mV, all outputs enabled and terminated ^[j] | | 72 | 86 | mA |
| | | | 500mV, all outputs enabled and terminated ^[j] | | 76 | 92 | mA |
| | | | 750mV, all outputs enabled and terminated ^[j] | | 84 | 100 | mA |
| | | LVPECL or LVDS | 350mV, divider and buffers disabled and unterminated | | 3 | 4 | mA |
| | | | 500mV, divider and buffers disabled and unterminated | | 3 | 4 | mA |
| | | | 750mV, divider and buffers disabled and unterminated | | 3 | 4 | mA |
| $I_{EE}^{[f]}$ | Power Supply Current for V_{EE} | LVPECL | 350mV, outputs enabled and terminated ^[g] | | 422 | 495 | mA |
| | | | 500mV, outputs enabled and terminated ^[h] | | 430 | 506 | mA |
| | | | 750mV, outputs enabled and terminated ^[i] | | 446 | 523 | mA |
| | | LVPECL | 350mV, divider and buffers disabled and unterminated | | 220 | 262 | mA |
| | | | 500mV, divider and buffers disabled and unterminated | | 220 | 262 | mA |
| | | | 750mV, divider and buffers disabled and unterminated | | 220 | 262 | mA |

[a] V_{CC_X} denotes V_{CC_CP} , V_{CC_CK} , V_{CC_SP} .

[b] V_{CCOX} denotes V_{CCOA} , V_{CCOB} , V_{CCOC} , V_{CCOD} .

[c] V_{CCA_X} denotes V_{CCA_IN1} , V_{CCA_IN2} , V_{CCA} , V_{CCA_XT} .

[d] I_{CC_X} denotes I_{CC_CP} , I_{CC_CK} , I_{CC_SP} .

[e] I_{CCA_X} denotes I_{CCA_IN1} , I_{CCA_IN2} , I_{CCA} , I_{CCA_XT} .

[f] Internal maximum dynamic switching current is included.

- [g] Differential outputs terminated with 50Ω to $V_{CCOX} - 1.6V$. QD1 output terminated with 50Ω to $V_{CCOD}/2$.
[h] Differential outputs terminated with 50Ω to $V_{CCOX} - 1.75V$. QD1 output terminated with 50Ω to $V_{CCOD}/2$.
[i] Differential outputs terminated with 50Ω to $V_{CCOX} - 2V$. QD1 output terminated with 50Ω to $V_{CCOD}/2$.
[j] Differential outputs terminated with 100Ω across Q and nQ. QD1 output terminated with 50Ω to $V_{CCOD}/2$.

Table 24. LVCMOS DC Characteristics for 3-level Pins, $V_{CC_X}^{[a]} = V_{CCOX}^{[b]} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Unit |
|----------|----------------------|--|--------------------------------------|---------------------------|---------|---------------------------|---------|
| V_{IH} | Input High Voltage | FIN[1:0], NA[1:0], NB[1:0], NC[1:0], ND[1:0] | | $0.7 \times V_{CC}^{[c]}$ | | 3.465 | V |
| V_{IM} | Input Middle Voltage | | | $0.4 \times V_{CC}^{[c]}$ | | $0.6 \times V_{CC}^{[c]}$ | V |
| V_{IL} | Input Low Voltage | | | -0.3 | | $0.3 \times V_{CC}^{[c]}$ | V |
| I_{IH} | Input High Current | | $V_{CC}^{[c]} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IM} | Input Middle Current | | $V_{IN} = V_{CC}^{[c]}/2$ | | ± 1 | | μA |
| I_{IL} | Input Low Current | | $V_{CC}^{[c]} = 3.465V, V_{IN} = 0V$ | -150 | | | μA |

[a] V_{CC_X} denotes V_{CC_CP} , V_{CC_CK} , V_{CC_SP} .

[b] V_{CCOX} denotes V_{CCOA} , V_{CCOB} , V_{CCOC} , V_{CCOD} .

[c] V_{CC} denotes V_{CCA_IN1} , V_{CC_CK} .

Table 25. LVCMOS DC Characteristics for 2-level Pins, $V_{CC_X}^{[a]} = V_{CCOX}^{[b]} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Unit |
|----------|---------------------|-------------------|--------------------------------------|---------------------------|---------|----------------------------|---------|
| V_{IH} | Input High Voltage | | | $0.7 \times V_{CC}^{[c]}$ | | 3.465 | V |
| V_{IL} | Input Low Voltage | REF_SEL | | -0.3 | | $0.3 \times V_{CC}^{[c]}$ | V |
| | | SDATA, SCLK | | -0.3 | | $0.15 \times V_{CC}^{[c]}$ | V |
| I_{IH} | Input High Current | SCLK, SDATA | $V_{CC}^{[c]} = V_{IN} = 3.465V$ | | | 5 | μA |
| | | REF_SEL | $V_{CC}^{[c]} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | SCLK, SDATA | $V_{CC}^{[c]} = 3.465V, V_{IN} = 0V$ | -150 | | | μA |
| | | REF_SEL | $V_{CC}^{[c]} = 3.465V, V_{IN} = 0V$ | -5 | | | μA |
| V_{OH} | Output High Voltage | LOCK | $I_{OH} = -4mA$ | 2.2 | | | V |
| V_{OL} | Output Low Voltage | SDATA, SCLK, LOCK | $I_{OL} = 4mA$ | | | 0.45 | V |

[a] V_{CC_X} denotes V_{CC_CP} , V_{CC_CK} , V_{CC_SP} .

[b] V_{CCOX} denotes V_{CCOA} , V_{CCOB} , V_{CCOC} , V_{CCOD} .

[c] V_{CC} denotes V_{CC_SP} , V_{CC_CK} .

Table 26. Differential Input DC Characteristics, $V_{CC_X}^{[a]} = V_{CCOX}^{[b]} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Unit |
|-----------|--|--------------------|---|----------------|---------|----------------------|---------|
| I_{IH} | Input High Current | CLK_IN, nCLK_IN | $V_{CC}^{[c]} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | CLK_IN | $V_{CC}^{[c]} = 3.465V$, $V_{IN} = 0V$ | -5 | | | μA |
| | | nCLK_IN | $V_{CC}^{[c]} = 3.465V$, $V_{IN} = 0V$ | -150 | | | μA |
| V_{PP} | Peak-to-Peak Voltage ^{[d], [e]} | CLK_IN, nCLK_IN | | 0.2 | | 1.4 | V |
| V_{CMR} | Common Mode Input Voltage ^{[d] [e]} | CLK_IN, nCLK_IN | | $V_{EE} + 1.1$ | | $V_{CC}^{[c]} - 0.3$ | V |

[a] V_{CC_X} denotes V_{CC_CP} , V_{CC_CK} , V_{CC_SP} .

[b] V_{CCOX} denotes V_{CCOA} , V_{CCOB} , V_{CCOC} , V_{CCOD} .

[c] V_{CC} denotes V_{CC_CK} .

[d] Common mode voltage is defined as the cross point.

[e] Input voltage cannot be less than $V_{EE} - 300mV$ or more than V_{CC} .

Table 27. LVPECL Output DC Characteristics ($Q_{mn}^{[a]}$), $V_{CC_X}^{[b]} = V_{CCOX}^{[c]} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|-------------|--|-------------------------|------------------|---------|------------------|------|
| V_{OH} | Output High Voltage ^[d] | 350mV Amplitude setting | $V_{CCOX} - 1.1$ | | $V_{CCOX} - 0.8$ | V |
| | | 500mV Amplitude setting | $V_{CCOX} - 1.1$ | | $V_{CCOX} - 0.8$ | |
| | | 750mV Amplitude setting | $V_{CCOX} - 1.1$ | | $V_{CCOX} - 0.8$ | |
| V_{OL} | Output Low Voltage ^[d] | 350mV Amplitude setting | $V_{CCOX} - 1.5$ | | $V_{CCOX} - 1.1$ | V |
| | | 500mV Amplitude setting | $V_{CCOX} - 1.6$ | | $V_{CCOX} - 1.3$ | |
| | | 750mV Amplitude setting | $V_{CCOX} - 1.8$ | | $V_{CCOX} - 1.5$ | |
| V_{SWING} | Single-ended Peak-to-Peak Output Voltage Swing | 350mV Amplitude setting | 280 | 350 | 420 | mV |
| | | 500mV Amplitude setting | 430 | 500 | 570 | |
| | | 750mV Amplitude setting | 630 | 700 | 770 | |

[a] Q_{mn} denotes the differential outputs QA[0:3], QB[0:3], QC[0:1], and QD0.

[b] V_{CC_X} denotes V_{CC_CP} , V_{CC_CK} , V_{CC_SP} .

[c] V_{CCOX} denotes V_{CCOA} , V_{CCOB} , V_{CCOC} , V_{CCOD} .

[d] Outputs terminated with 50Ω to $V_{CCOX} - 2V$ for 750mV amplitude setting, $V_{CCOX} - 1.75V$ for 500mV amplitude setting, and $V_{CCOX} - 1.6V$ for 350mV amplitude setting.

Table 28. LVDS Output DC Characteristics (Qmn^[a]), V_{CC_X}^[b] = V_{CCOX}^[c] = 3.3V ±5%, T_A = -40°C to +85°C, V_{EE} = 0V

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|------------------|---|-------------------------|---------|---------|---------|------|
| V _{OD} | Differential Output Voltage | 350mV Amplitude setting | 0.27 | 0.32 | 0.37 | V |
| | | 500mV Amplitude setting | 0.39 | 0.46 | 0.53 | |
| | | 750mV Amplitude setting | 0.62 | 0.69 | 0.76 | |
| ΔV _{OD} | V _{OD} Magnitude Change | | | | 50 | mV |
| V _{OS} | Offset Voltage ^{[d],[e],[f],[g]} | 350mV Amplitude setting | 1.9 | 2.3 | 2.7 | V |
| | | 500mV Amplitude setting | 1.8 | 2.2 | 2.6 | |
| | | 750mV Amplitude setting | 1.7 | 2.1 | 2.5 | |
| ΔV _{OS} | V _{OS} Magnitude Change | | | | 50 | mV |

[a] Qmn denotes the differential outputs QA[0:3], QB[0:3], QC[0:1], and QD0.

[b] V_{CC_X} denotes V_{CC_CP}, V_{CC_CK}, V_{CC_SP}.

[c] V_{CCOX} denotes V_{CCOA}, V_{CCOB}, V_{CCOC}, V_{CCOD}.

[d] No external DC pulldown resistor.

[e] Loading condition is with 100Ω across the differential output.

[f] Offset voltage (V_{OS}) changes with amplitude setting.

[g] It does not conform to standard LVDS V_{OS} values.

Table 29. LVCMOS DC Characteristics for QD1 Output, V_{CC_X}^[a] = V_{CCOD} = 3.3V ±5%

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|-----------------|---------------------|-----------------------------|---------|---------|---------|------|
| V _{OH} | Output High Voltage | QD1, I _{OH} = -8mA | 2.6 | | | V |
| V _{OL} | Output Low Voltage | QD1, I _{OL} = 8mA | | | 0.5 | V |

[a] V_{CC_X} denotes V_{CC_CP}, V_{CC_CK}, V_{CC_SP}.

Table 30. Crystal Characteristics

| Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|------------------------------------|-----------------|-------------|---------|---------|------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 10 | | 50 | MHz |
| Equivalent Series Resistance (ESR) | > 32 MHz | | | 30 | Ω |
| | ≤ 32 MHz | | | 50 | |
| Load Capacitance (C _L) | 50MHz Crystal | | 8 | < 12 | pF |
| | 25MHz Crystal | | 12 | < 22 | |
| Shunt Capacitance | > 32 MHz | | | 3 | pF |
| | ≤ 32 MHz | | | 7 | pF |
| Maximum Crystal Drive Level | | | 200 | | μW |
| Frequency Stability (total) | | -100 | | 100 | ppm |

AC Electrical Characteristics

Table 31. AC Characteristics,^[a] $V_{CC_X}^{[b]} = V_{CCOX}^{[c]} = 3.3V + 5\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, $V_{EE} = 0V$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Unit |
|---------------------------------|--------------------------------------|---|--------------------------------|---------|---------|---------|------|
| f _{VCO} | VCO Frequency | | | 2400 | | 2500 | MHz |
| f _{PFD} | Phase / Frequency Detector Frequency | | | 5 | | 200 | MHz |
| f _{OUT} | Output Frequency | QA[0:3], nQA[0:3] QB[0:3], nQB[0:3] QC[0:1], nQC[0:1] | | 10.91 | | 2500 | MHz |
| | | QD0, nQD0 | Integer divider selected | 10.91 | | 2500 | MHz |
| | | | Fractional divider selected | 20 | | 250 | MHz |
| | | QD1 | Integer divider selected | 10.91 | | 250 | MHz |
| | | | Fractional divider selected | 20 | | 250 | MHz |
| t _{sk(b)} | Bank Skew ^{[d], [e], [f]} | Bank A | Same frequency and output type | | | 45 | ps |
| | | Bank B | | | | 45 | |
| | | Bank C | | | | 20 | |
| t _R / t _F | Output Rise/Fall Time | QA[0:3],nQA[0:3] QB[0:3], nQB[0:3] QC[0:1], nQC[0:1] QD0, nQD0 | 20% to 80% | | 100 | 200 | ps |
| | | QD1 | 20% to 80% | | 700 | 1100 | |
| odc | Output Duty Cycle ^[g] | QA[0:3], nQA[0:3] QB[0:3], nQB[0:3] QC[0:1], nQC[0:1], QD0, nQD0 | F _{OUT} ≤ 1250MHz | 45 | 50 | 55 | % |
| | | | F _{OUT} > 1250MHz | 40 | 50 | 60 | % |
| | | QD1 | F _{OUT} < 156.25MHz | 45 | 50 | 55 | % |
| | | | F _{OUT} ≥ 156.25MHz | 40 | 50 | 60 | % |
| t _{LOCK} | PLL Lock Time ^[h] | | | | 10 | | ms |

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] V_{CC_X} denotes V_{CC_CP} , V_{CC_CK} , V_{CC_SP} .

[c] V_{CCOX} denotes V_{CCOA} , V_{CCOB} , V_{CCOC} , V_{CCOD} .

[d] Defined as skew among outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.

[e] This parameter is defined in accordance with JEDEC Standard 65.

[f] This parameter is guaranteed by characterization. Not tested in production.

[g] Duty cycle of PLL bypassed signals (input reference clock or crystal input) is not adjusted by the device.

[h] PLL Lock Time is defined as time from input clock availability to frequency locked output. The following loop filter component values may be used: $R_Z = 150\Omega$, $C_Z = 0.1\mu F$, $C_P = 30pF$. See [Applications Information](#).

Table 32. Qmn^[a] and QD1 Phase Noise and Jitter Characteristics, V_{CC_X}^[b] = V_{CCOX}^[c] = 3.3V + 5%, T_A = -40°C to +85°C^{[d][e][f][g][h][i]}

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Unit |
|-----------------------|---|--|----------------------------------|---------|---------|---------|--------|
| f _{jit} (Ø) | RMS Phase Jitter Random | Qmn = 156.25MHz | Integration range: 12kHz – 20MHz | | 80 | 110 | fs |
| | RMS Phase Jitter Random | Qmn = 125MHz | Integration range: 12kHz – 20MHz | | 85 | | fs |
| | RMS Phase Jitter Random | Qmn = 100MHz | Integration range: 12kHz – 20MHz | | 92 | | fs |
| | RMS Phase Jitter Random | Qmn = 25MHz | Integration range: 12kHz – 5MHz | | 115 | | fs |
| | RMS Phase Jitter Random | QD0 = 212.5MHz (fractional) ^[j] | Integration range: 12kHz – 20MHz | | 132 | | fs |
| | RMS Phase Jitter Random | QD1 = 125MHz | Integration range: 12kHz – 20MHz | | 170 | | fs |
| | RMS Phase Jitter Random ^[k] | QAn = 156.25MHz | Integration range: 12kHz – 20MHz | | 95 | | fs |
| | | QBn = 100MHz | Integration range: 12kHz – 20MHz | | 140 | | fs |
| | | QCn = 25MHz | Integration range: 12kHz – 5MHz | | 115 | | fs |
| | | QD0 = 212.5MHz (fractional) | Integration range: 12kHz – 20MHz | | 133 | | fs |
| Φ _N (10) | Single-Side Band Noise Power, 10Hz from Carrier | | Qmn = 156.25MHz | | -71 | | dBc/Hz |
| Φ _N (100) | Single-Side Band Noise Power, 100Hz from Carrier | | Qmn = 156.25MHz | | -113 | | dBc/Hz |
| Φ _N (1k) | Single-Side Band Noise Power, 1kHz from Carrier | | Qmn = 156.25MHz | | -136 | | dBc/Hz |
| Φ _N (10k) | Single-Side Band Noise Power, 10kHz from Carrier | | Qmn = 156.25MHz | | -137.6 | | dBc/Hz |
| Φ _N (100k) | Single-Side Band Noise Power, 100kHz from Carrier | | Qmn = 156.25MHz | | -143.4 | | dBc/Hz |
| Φ _N (1M) | Single-Side Band Noise Power, 1MHz from Carrier | | Qmn = 156.25MHz | | -156 | | dBc/Hz |
| Φ _N (10M) | Single-Side Band Noise Power, 10MHz from Carrier | | Qmn = 156.25MHz | | -162 | | dBc/Hz |
| Φ _N (∞) | Noise Floor (≥30MHz from Carrier) | | Qmn = 156.25MHz | | -162 | | dBc/Hz |

[a] Qmn denotes the differential outputs QA[0:3], QB[0:3], QC[0:1] or QD0.

[b] V_{CC_X} denotes V_{CC_CP}, V_{CC_CK}, V_{CC_SP}.

[c] V_{CCOX} denotes V_{CCOA}, V_{CCOB}, V_{CCOC}, V_{CCOD}.

[d] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[e] All outputs enabled and configured for the same output frequency unless otherwise noted.

[f] Characterized using a 50MHz Crystal unless otherwise noted.

- [g] V_{CCA} requires a voltage regulator. Voltage supplied to V_{CCA} should be derived from a regulator with a typical power supply rejection ratio of 80dB at 1kHz and ultra-low noise generation with a typical value of 3nV/ $\sqrt{\text{Hz}}$ at 10kHz and 7nV/ $\sqrt{\text{Hz}}$ at 1kHz.
- [h] Characterized with 750mV output voltage swing configuration for all differential outputs.
- [i] The following loop filter component values were used: $R_Z = 150\Omega$, $C_Z = 0.1\mu\text{F}$, $CP = 200\text{pF}$. PLL Charge Pump Current Control set at 5.2mA.
- [j] $QAx = 156.25\text{MHz}$, $QBx = 156.25\text{MHz}$, $QCx = 156.25\text{MHz}$, $QD1 = \text{OFF}$.
- [k] $QAx = 156.25\text{MHz}$, $QBx = 100\text{MHz}$, $QCx = 25\text{MHz}$, $QD0 = 212.5\text{MHz}$ (fractional), $QD1 = \text{OFF}$.

Phase Noise Plots

Figure 4. Typical Phase Noise at 312.5MHz (QB1)

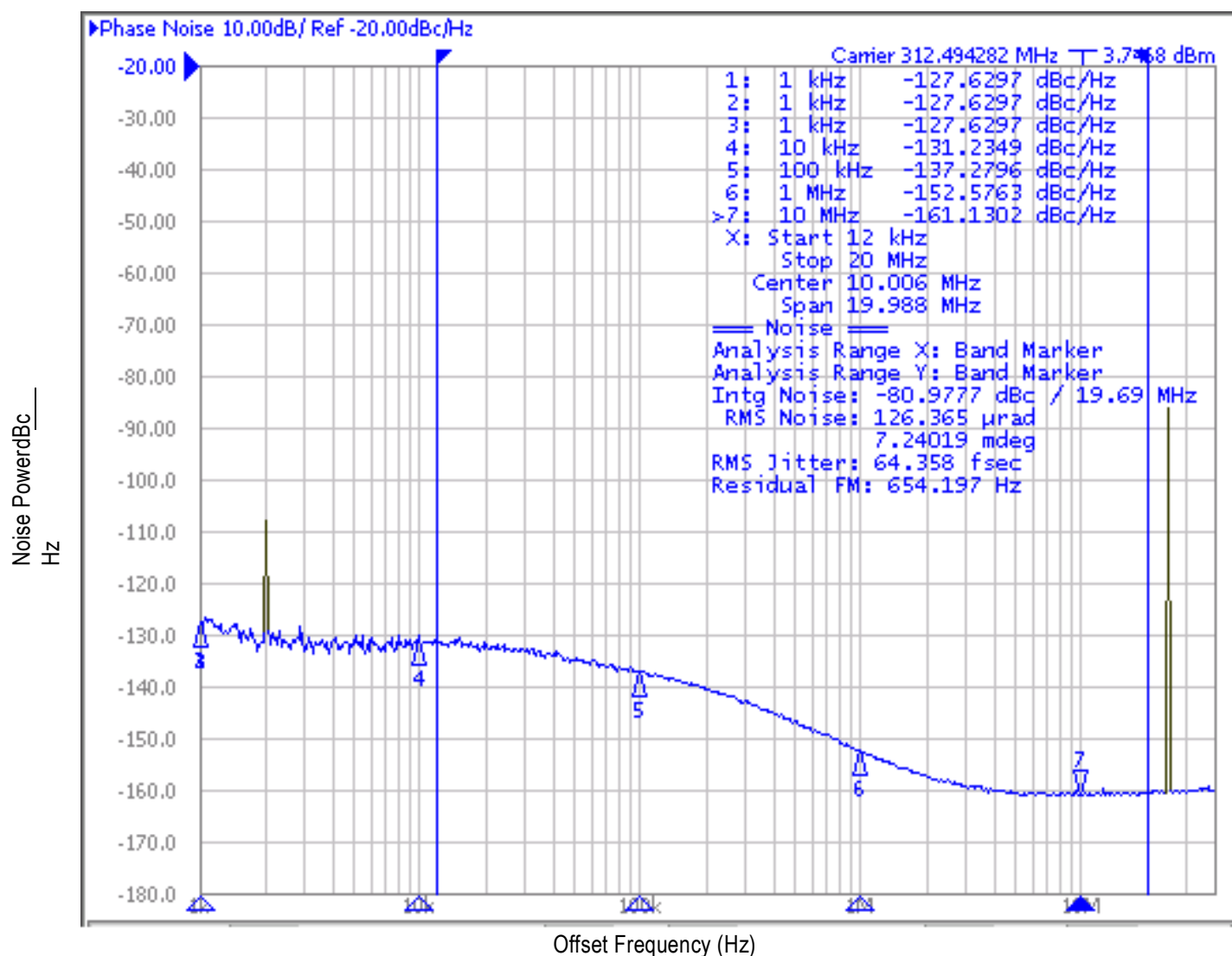


Figure 5. Typical Phase Noise at 156.25MHz (QB1)

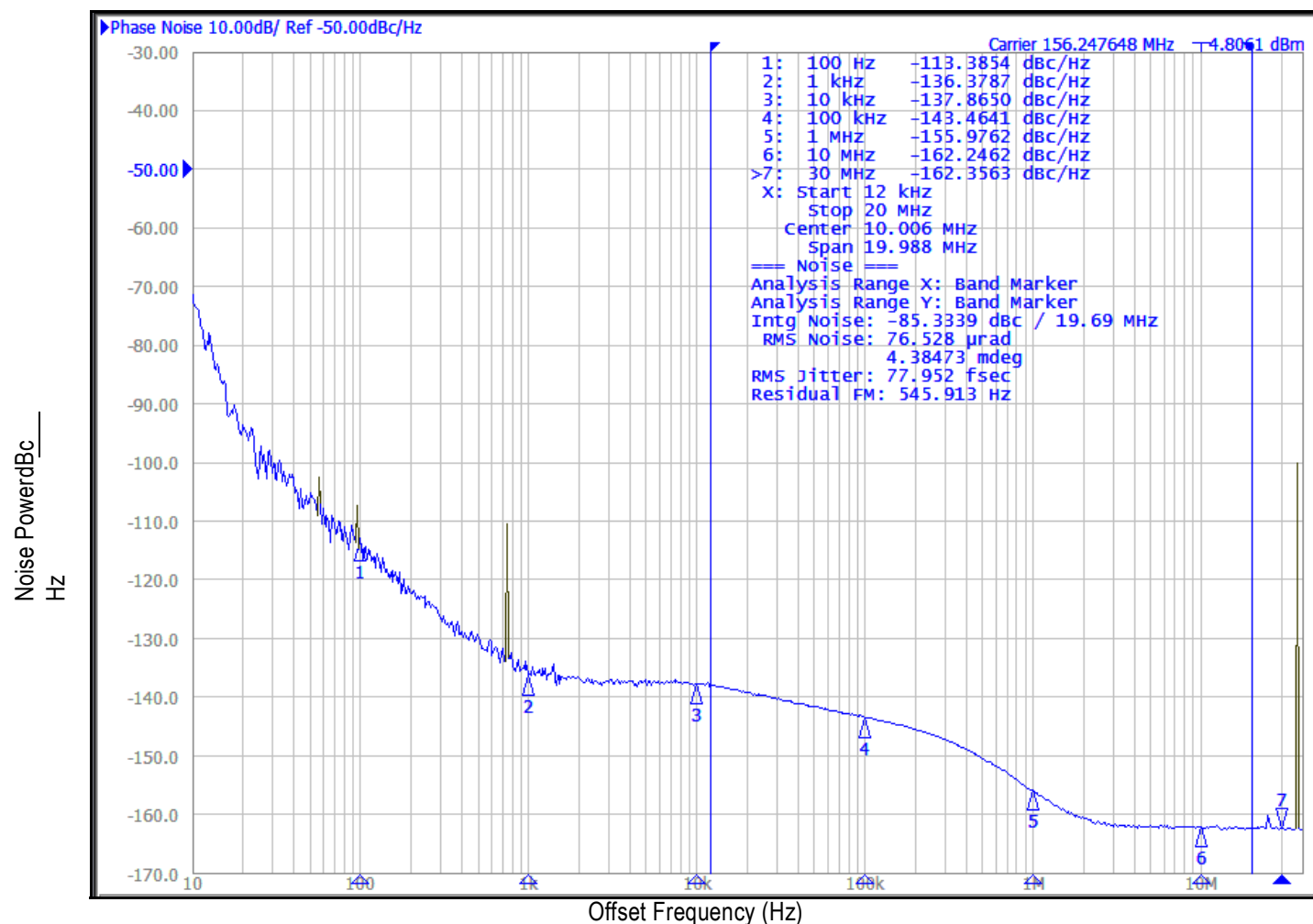
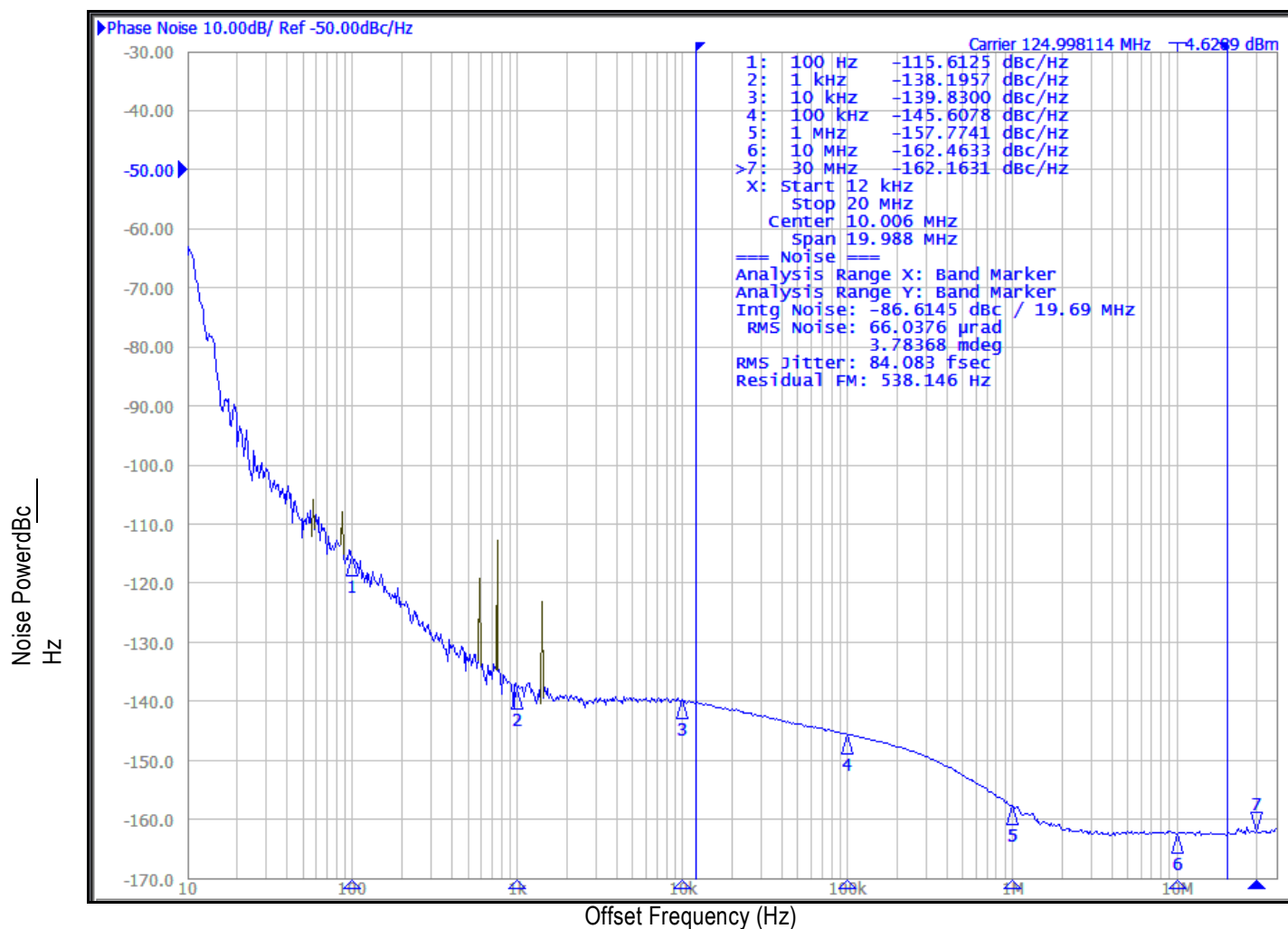


Figure 6. Typical Phase Noise at 125MHz (QB1)^[1]



[1] Measured using a 50MHz, 12pF crystal as input reference.

Applications Information

Recommendations for Unused Input and Output Pins

Inputs

LVC MOS Control Pins

All control pins have internal pull-up and/or pull-down resistors; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

Outputs

LVPECL Outputs

All unused LVPECL outputs must be left floating. Renesas recommends that there is no trace attached.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 Ω across. If left floating, there should be no trace attached.

LVC MOS Outputs

QD1 output can be left floating if unused. There should be no trace attached.

Overdriving the XTAL Interface

The OSC I input can be overdriven by an LVC MOS driver or by one side of a differential driver through an AC coupling capacitor. The OSC O pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVC MOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 7 shows an example of the interface diagram for a high-speed 3.3V LVC MOS driver. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50 Ω applications, R_1 and R_2 can be 100 Ω . This can also be accomplished by removing R_1 and changing R_2 to 50 Ω . The values of the resistors can be increased to reduce the loading for a slower and weaker LVC MOS driver.

Figure 7. General Diagram for LVC MOS Driver to XTAL Input Interface

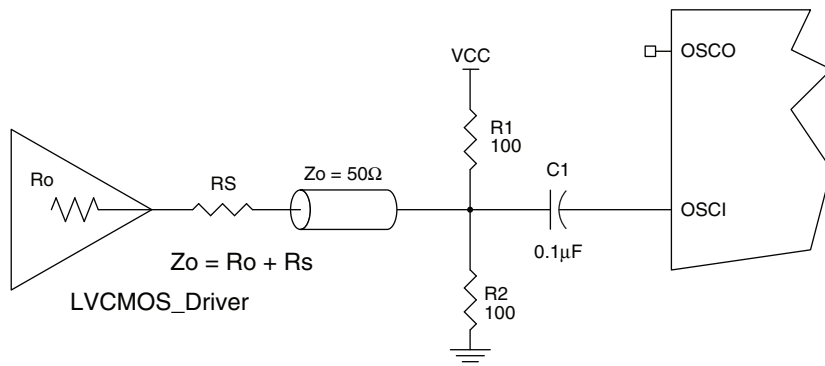
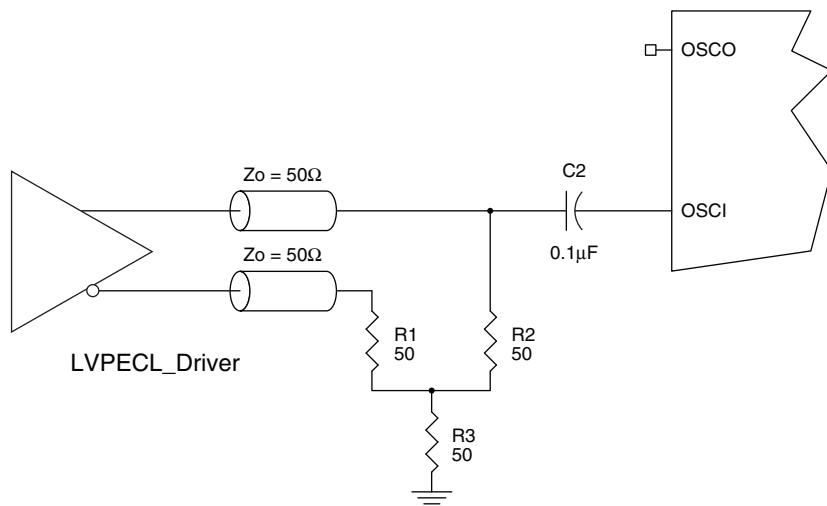


Figure 8 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the OSC I input. It is recommended that all components in the schematics be placed in the layout. Though some components may not be used, they can be used for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

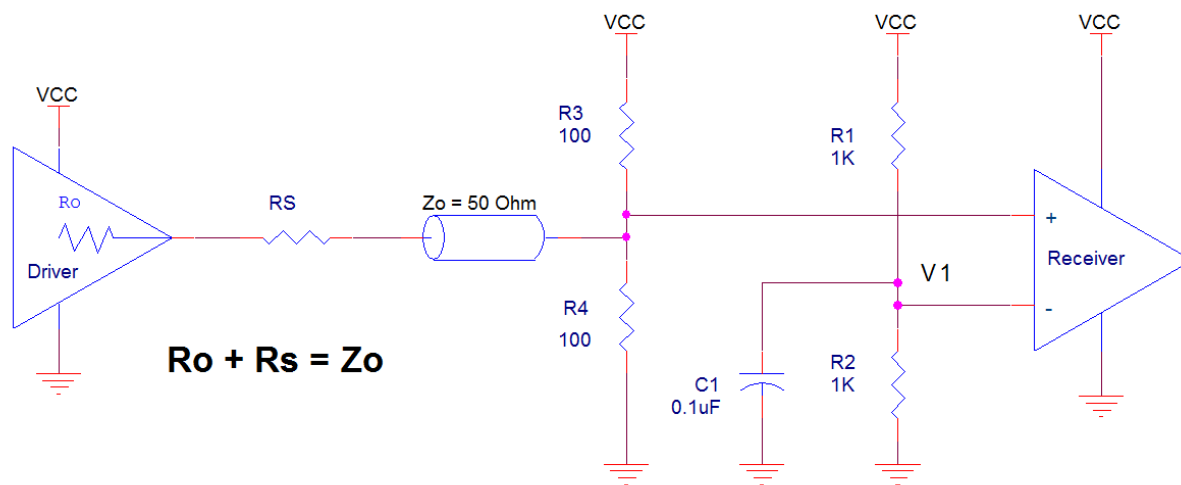
Figure 8. General Diagram for LVPECL Driver to XTAL Input Interface



Wiring the Differential Input to Accept Single-Ended Levels

Figure 9 shows how a differential input can be wired to accept single-ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors, R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 may need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock is driven from a single-ended 2.5V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25V, then adjust the R1 and R2 values to set V_1 at 1.25V. The values below are when both the single-ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance.

Figure 9. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω . The resistor values can be increased to reduce the loading for a slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits for differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended to reduce the amplitude while maintaining an edge rate faster than 1V/ns . The datasheet specifies a lower differential amplitude, however, this only applies to differential signals. For single-ended applications, the swing can be larger, however, V_{IL} cannot be less than -0.3V , and V_{IH} cannot be more than $V_{CC} + 0.3\text{V}$. Though some of the recommended components may not be used, the pads should be placed in the layout. They can be used for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

3.3V Differential Clock Input Interface

CLK, nCLK accepts LVDS, LVPECL and other differential signals. Both V_{SWING} and V_{OX} must meet the V_{PP} and V_{CMR} input requirements. Figure 10 to Figure 12 show interface examples for the CLK, nCLK input driven by the most common driver types. The input interfaces suggested here are some examples of direct-coupled termination.

Figure 10. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

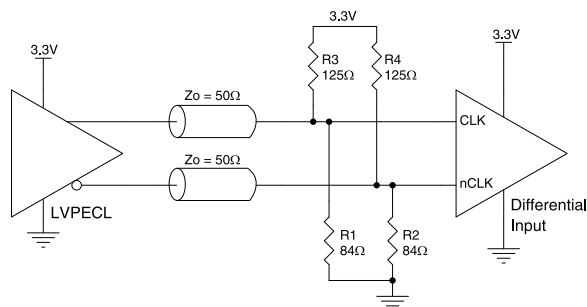


Figure 11. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

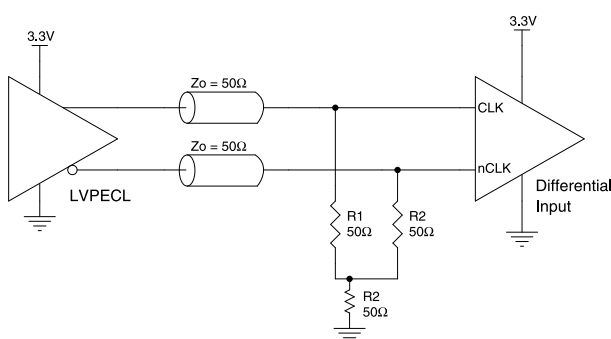
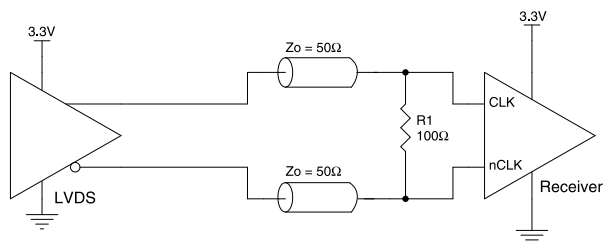


Figure 12. CLK/nCLK Input Driven by a 3.3V LVDS Driver



LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. Renesas offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source.

The standard termination schematic as shown in Figure 13 can be used with either type of output structure. Figure 14, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact Renesas and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 13. Standard LVDS Termination

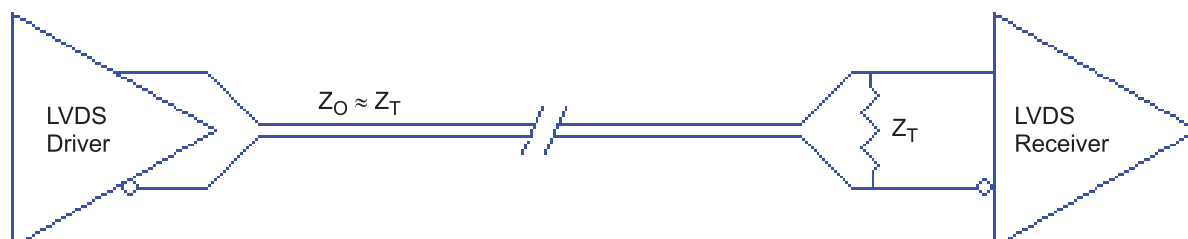
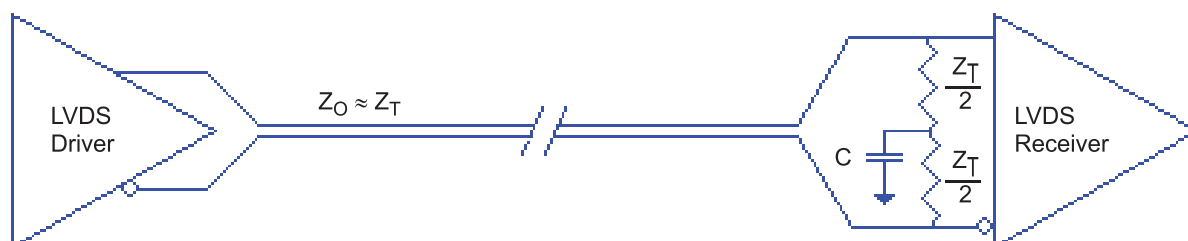


Figure 14. Optional LVDS Termination



For more information on the recommended termination schemes, see Figure 15 to Figure 17.

Figure 15. DC Termination for LVDS Outputs

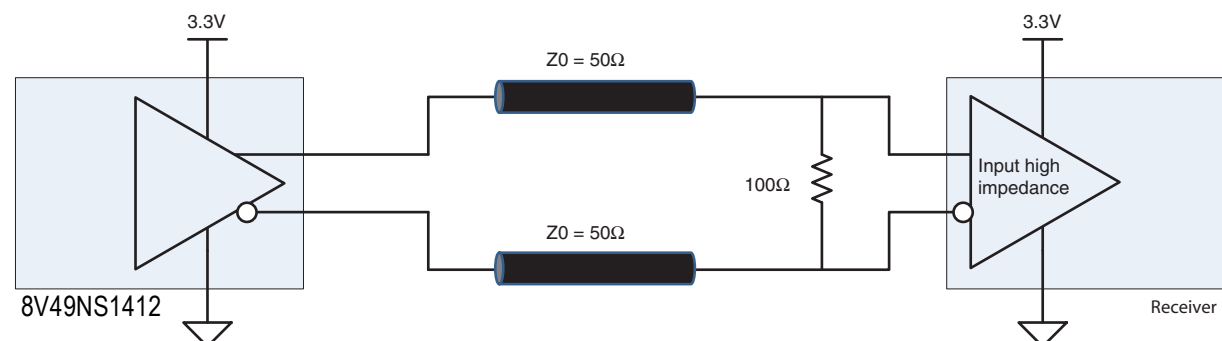


Figure 16. AC Termination for LVDS Outputs

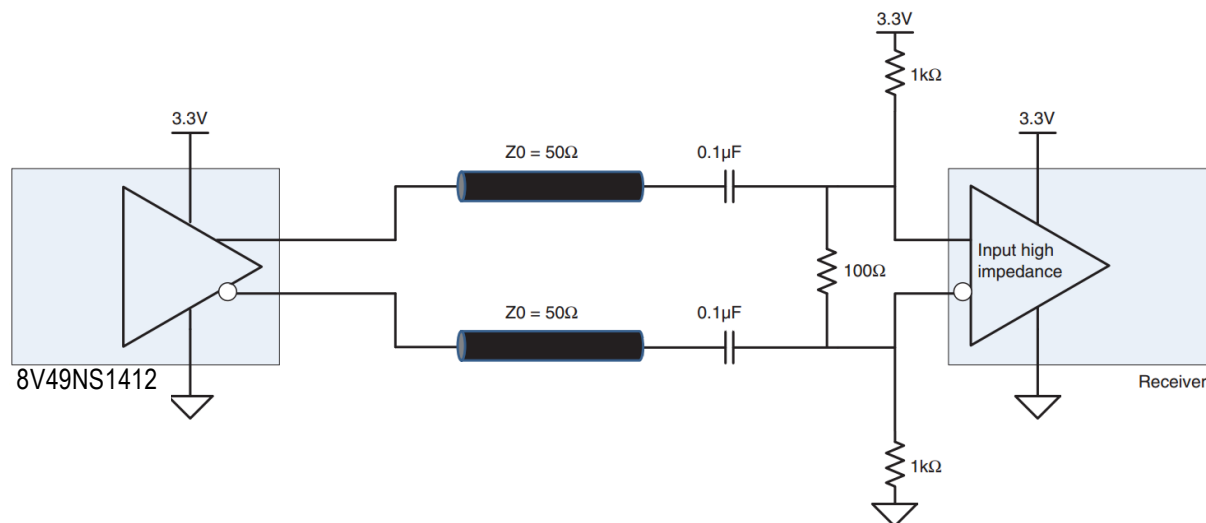
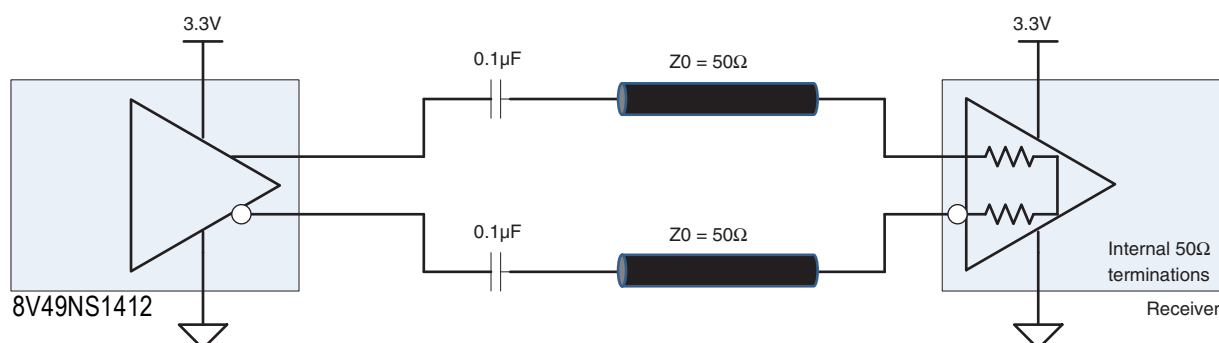


Figure 17. AC Termination for LVDS Outputs Used with an Input Clock Receiver with Internal 50Ω Terminations and DC Bias



Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts are recommended only as guidelines. The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figure 18 and Figure 19 show two different termination schemes that are recommended only as guidelines. Other suitable clock termination schemes may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

Figure 18. 3.3V LVPECL Output Termination

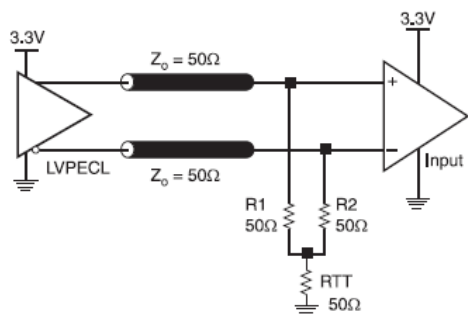


Figure 19. 3.3V LVPECL Output Termination

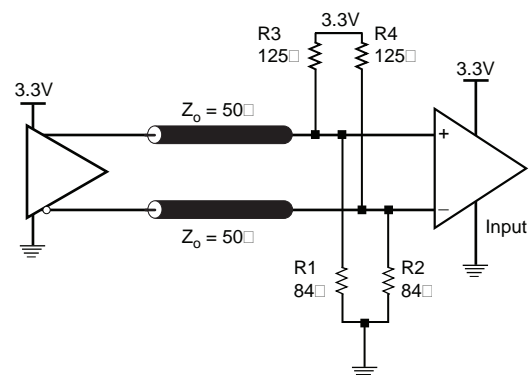


Figure 18 and Figure 19 show two different LVPECL termination schemes for 750mV amplitude setting which are recommended only as guidelines. Recommended values of R1/R2/R3/R4 for LVPECL termination (Figure 19; Thevenin Equivalent) for 350mV and 500mV amplitude settings can be found in the following table.

Table 33. LVPECL Output Termination, $V_{CCOX} = 3.3V \pm 5\%$

| Test Conditions | Bias Voltage | R1 [Ω] | R2 [Ω] | R3 [Ω] | R4 [Ω] |
|-------------------------|--------------------|-----------------|-----------------|-----------------|-----------------|
| 350mV Amplitude Setting | $V_{CCOX} - 1.6V$ | 105 | 105 | 97.6 | 97.6 |
| 500mV Amplitude Setting | $V_{CCOX} - 1.75V$ | 95.3 | 95.3 | 107 | 107 |
| 750mV Amplitude Setting | $V_{CCOX} - 2.0V$ | 84 | 84 | 125 | 125 |

VFQFPN EPAD Thermal Release Path

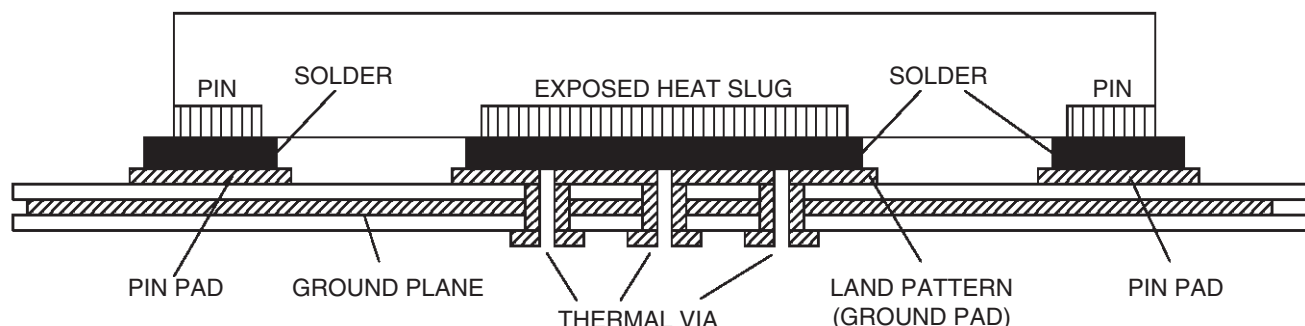
In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 20. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern.

Note: These recommendations are to be used as a guideline only.

For more information, see the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead-frame Base Package, Amkor Technology.

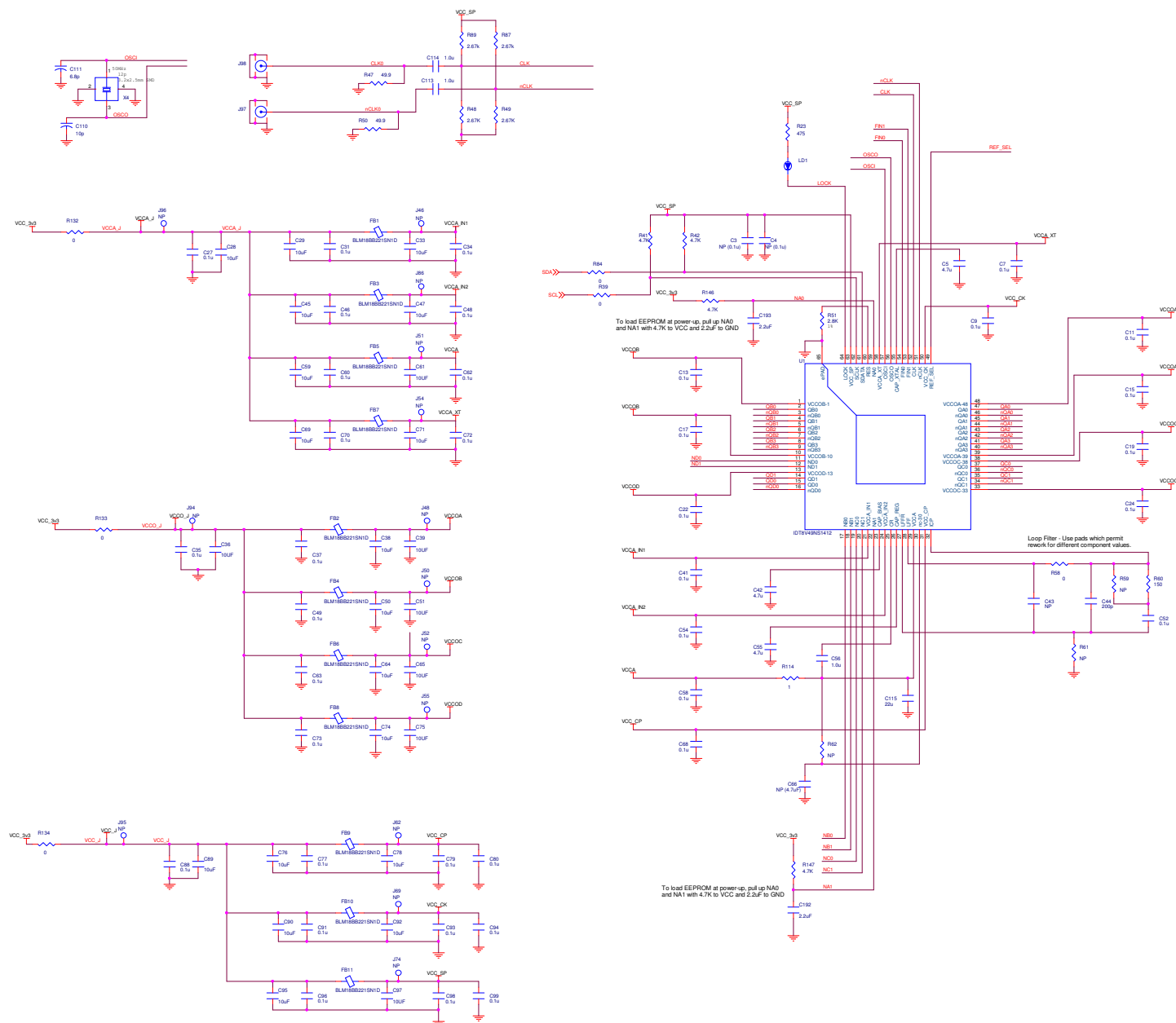
Figure 20. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to scale)



Schematic and Layout Recommendations

Figure 21 shows an example 8V49NS1412 application schematic operating the device at $V_{CC} = 3.3V$. This example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

Figure 21. 8V49NS1412 Application Schematic



Crystal layout is very important to minimize capacitive coupling between the crystal pads and leads and other metal in the circuit board. Capacitive coupling to other conductors has two adverse effects: it reduces the oscillator frequency leaving less tuning margin and noise coupling from power planes, and logic transitions on signal traces can pull the phase of the crystal resonance, inducing jitter. Routing I²C under the crystal is a common layout error, based on the assumption that it is a low frequency signal and will not affect the crystal oscillation. In fact, I²C transition times are short enough to capacitively couple into the crystal-oscillator loop if they are routed close enough to the crystal traces.

In layout, all capacitive coupling to the crystal from any signal trace is to be minimized, that is to the OSCI and OSCO pins, traces to the crystal pads, the crystal pads, and the tuning capacitors. Using a crystal on the top layer as an example, void all signal and power layers under the crystal connections between the top layer and the ground plane used by the 8V49NS1412. Then calculate the parasitic capacity to the ground and determine if it is large enough to preclude tuning the oscillator. If the coupling is excessive, particularly if the first layer under the crystal is a ground plane, a layout option is to void the ground plane and all deeper layers until the next ground plane is reached. The ground connection of the tuning capacitors should first be made between the capacitors on the top layer, then a single ground via is dropped to connect the tuning cap ground to the ground plane as close to the 8V49NS1412 as possible as shown in the schematic.

As with any high-speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8V49NS1412 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. The ferrite bead and the 0.1uF capacitor in each power pin filter should always be placed on the device side of the board. The other components can be on the opposite side of the PCB if space on the top side is limited. Pull-up and pull-down resistors to set configuration pins can all be placed on the PCB side opposite the device side to free up the device side area if necessary.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. Depending on the application, the filter may need to be adjusted to get a lower cutoff frequency to adequately attenuate low-frequency noise. Additionally, good general design practices for power plane voltage stability suggest adding bulk capacitance in the local area of all devices.

For additional layout recommendations and guidelines, contact clocks@idt.com.

Power Dissipation and Thermal Considerations

The 8V49NS1412 is a multi-functional, high-speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as each of these features and functions is enabled.

The device is designed and characterized to operate within the ambient industrial temperature range of -40°C to +85°C. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature.

The following power calculation examples were generated using a maximum ambient temperature and supply voltage. For many applications, the power consumption will be much lower. Contact Renesas technical support for any concerns on calculating the power dissipation for your own specific configuration.

Example 1. LVPECL, 750mV Output Swing

This section provides information on power dissipation and junction temperature when the device differential outputs are configured for LVPECL level, 750mV output swing. Equations and example calculations are also provided.

Table 34. Power Calculations Configuration #1

| Output | Output Style | Output Swing |
|--------|--------------|--------------|
| QA0 | LVPECL | 750mV |
| QA1 | LVPECL | 750mV |
| QA2 | LVPECL | 750mV |
| QA3 | LVPECL | 750mV |
| QB0 | LVPECL | 750mV |
| QB1 | LVPECL | 750mV |
| QB2 | LVPECL | 750mV |
| QB3 | LVPECL | 750mV |
| QC0 | LVPECL | 750mV |
| QC1 | LVPECL | 750mV |
| QD0 | LVPECL | 750mV |
| QD1 | LVC MOS | N/A |

1. Power Dissipation

The total power dissipation is the sum of the core power plus the power dissipated due to output loading. The following is the power dissipation for $V_{CC} = 3.465V$, which gives worst case results.

- Power(core)_{MAX} = $V_{CC_MAX} \times I_{EE_MAX}^{[1]} = 3.465V \times 523mA = 1812.2mW$
- Power(LVPECL outputs)_{MAX} = 34.2mW/Loaded Output pair. See [Junction Temperature](#).
If all outputs are loaded, the total power is $11 \times 34.2mW = 376.2mW$
- Total Power_{MAX}** = Power(core) + Power (LVPECL outputs) + Power (LVC MOS output)
= $1812.1mW + 376.2mW = 2188.3mW = 2.1883W$

2. Junction Temperature

Junction temperature, T_J , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_J , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_J is as follows: $T_J = T_A + P_D \times \theta_{JA}$:

T_J = Junction Temperature

T_A = Ambient Temperature

P_D = Power Dissipation (W) in desired operating configuration

θ_{JA} = Junction-to-Ambient Thermal Resistance

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance must be used. Assuming no air flow and a multi-layer board, the appropriate value is 15.6°C/W per [Table 36](#).

[1] Maximum QD1 output switching current is included.

Therefore, assuming $T_A = 85^\circ\text{C}$ and all outputs switching, T_J will be:

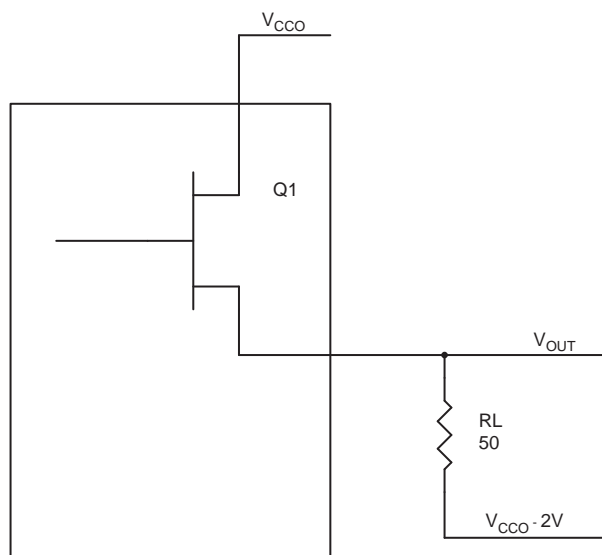
$$85^\circ\text{C} + 2.1883\text{W} \times 15.6^\circ\text{C/W} = 119.1^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

3. Power Dissipation due to output loading

This section calculates the power dissipation for the LVPECL output pair. LVPECL output driver circuit and termination are shown in Figure 22.

Figure 22. LVPECL Driver Circuit and Termination



To calculate worst case power dissipation at the output(s), use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCOX} - 2V$. These are typical calculations.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCOX_MAX} - 0.8V$
 $(V_{CCOX_MAX} - V_{OH_MAX}) = 0.8V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCOX_MAX} - 1.5V$
 $(V_{CCOX_MAX} - V_{OL_MAX}) = 1.5V$

Pd_H is the power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCOX_MAX} - 2V))/R_L] \times (V_{CCOX_MAX} - V_{OH_MAX}) = [(2V - (V_{CCOX_MAX} - V_{OH_MAX}))/R_L] \times (V_{CCOX_MAX} - V_{OH_MAX}) = [(2V - 0.8V)/50\Omega] \times 0.8V = 19.2mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCOX_MAX} - 2V))/R_L] \times (V_{CCOX_MAX} - V_{OL_MAX}) = [(2V - (V_{CCOX_MAX} - V_{OL_MAX}))/R_L] \times (V_{CCOX_MAX} - V_{OL_MAX}) = [(2V - 1.5V)/50\Omega] \times 1.5V = 15mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 34.2mW$$

Example 2. LVDS, 350mV Output Swing

This section provides information on power dissipation and junction temperature when the device differential outputs are configured for LVDS levels, 350mV output swing. Equations and example calculations are also provided.

Table 35. Power Calculations Configuration #2

| Output | Output Style | Output Swing |
|--------|--------------|--------------|
| QA0 | LVDS | 350mV |
| QA1 | LVDS | 350mV |
| QA2 | LVDS | 350mV |
| QA3 | LVDS | 350mV |
| QB0 | LVDS | 350mV |
| QB1 | LVDS | 350mV |
| QB2 | LVDS | 350mV |
| QB3 | LVDS | 350mV |
| QC0 | LVDS | 350mV |
| QC1 | LVDS | 350mV |
| QD0 | LVDS | 350mV |
| QD1 | LVC MOS | N/A |

1. Power Dissipation

The total power dissipation is the sum of the core power plus the power dissipation due to output loading. The following is the power dissipation for $V_{CCX} = V_{CCA_X} = V_{CCOX} = 3.465V$, which gives worst case results.

$$\begin{aligned}
 \text{Power}_{\text{MAX}} &= V_{CCX_MAX} \times I_{CCX_MAX} + V_{CCA_X_MAX} \times I_{CCA_X_MAX} + V_{CCOX_MAX} \times I_{CCOX_MAX} \\
 &= 3.465V \times 100mA + 3.465V \times 165mA + 3.465V (96mA + 96mA + 65mA + 86mA) \\
 &= 346.5mW + 571.1mW + 1188.5mW = 2106.7mW = \mathbf{2.107W}
 \end{aligned}$$

2. Junction Temperature

Junction temperature, T_J , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_J , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_J is as follows: $T_J = T_A + P_D \times \theta_{JA}$:

T_J = Junction Temperature

T_A = Ambient Temperature

P_D = Power Dissipation (W) in desired operating configuration

θ_{JA} = Junction-to-Ambient Thermal Resistance

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance must be used. Assuming no air flow and a multi-layer board, the appropriate value is 15.6°C/W per [Table 36](#).

Therefore, assuming $T_A = 85^\circ\text{C}$ and all outputs switching, T_J will be:

$$85^\circ\text{C} + 2.107W \times 15.6^\circ\text{C/W} = 117.9^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_J will vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

Reliability Information

Table 36. Thermal Resistance for 64-VFQFPN Package

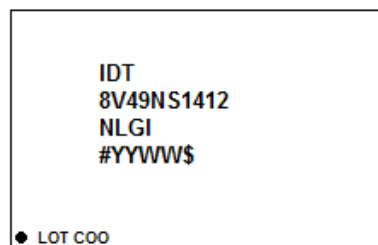
| Symbol | Thermal Parameter | Condition | Value | Unit |
|---------------------|---------------------|-------------|-------|------|
| $\theta_{JA}^{[a]}$ | Junction-to-Ambient | No air flow | 15.6 | °C/W |
| θ_{JC} | Junction-to-Case | | 15.3 | °C/W |
| θ_{JB} | Junction-to-Board | | 0.6 | °C/W |

[a] Theta J_A (θ_{JA}) values calculated using an 8-layer PCB (114.3mm x 101.6mm), with 2oz. (70μm) copper plating on all 8 layers, with ePad connected to 4 ground planes.

Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Marking Diagram



- Line 1 indicates the part number prefix.
- Line 2 indicates the part number.
- Line 3 indicates the part number suffix.
- Line 4:
 - “#”: stepping.
 - “YYWW” is the last two digits of the year and work week number that the part was assembled.
 - “\$” is the mark code.
- “LOT” indicates the lot number and “COO” indicates country of origin.

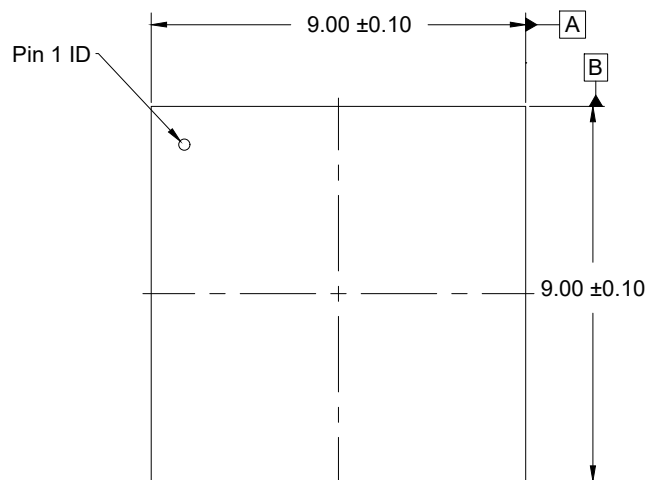
Ordering Information

| Part/Order Number | Package | Shipping Packaging | Temperature |
|-------------------|-------------------------------|--------------------|----------------|
| 8V49NS1412NLGI | 64-VFQFPN 9 × 9 mm, Lead-free | Tray | -40°C to +85°C |
| 8V49NS1412NLGI8 | 64-VFQFPN 9 × 9 mm, Lead-free | Tape and Reel | -40°C to +85°C |

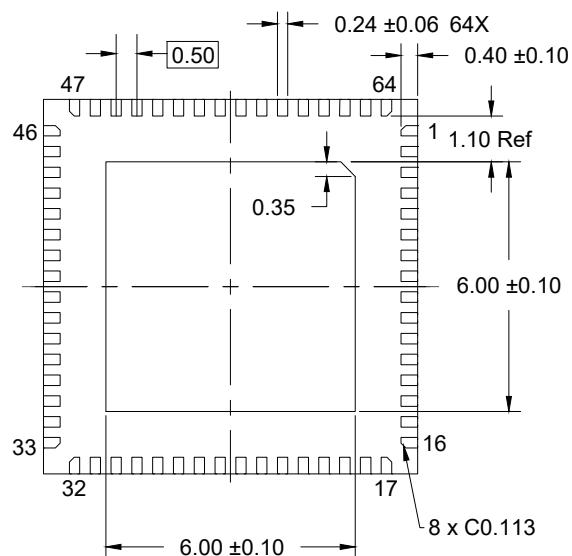
Note: “VFQFN” and “VFQFPN” have the same meaning of “Very Flat Quad Fine Pitch None-Lead”.

Revision History

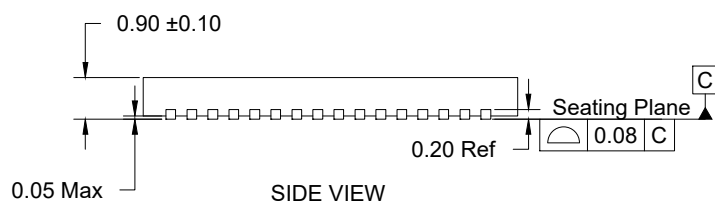
| Date | Description of Change |
|--------------------|--|
| September 28, 2022 | Changed all references of VFQFN to VFQFPN. |
| May 11, 2022 | Added phase noise and jitter data for 312.5MHz in Table 32 . |
| July 29, 2020 | Fixed a minor typo; no technical changes |
| May 14, 2018 | Added Figure 4 |
| April 11, 2018 | Initial release. |



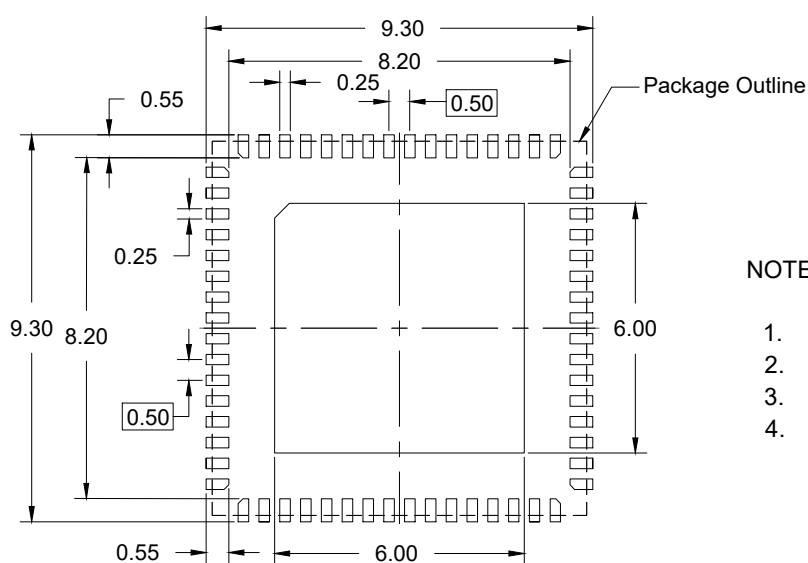
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.

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