Description

The 8V41NS0412 is a clock generator with four output dividers: three integer, and one that is either integer or fractional. When used with an external crystal, the 8V41NS0412 generates high performance timing geared towards the communications and datacom markets, especially for applications demanding extremely low phase noise, such as 10GE, 40GE, 100G, and 400GE.

The 8V41NS0412's versatile frequency configurations are optimized to deliver excellent phase noise performance. The device delivers an optimum combination of high clock frequency and low-phase noise performance, combined with high-power supply noise rejection.

The 8V41NS0412 supports HCSL type of output level on eleven of its outputs. In addition, there is a single LVCMOS output that has the option of providing a generated clock or acting as a reference bypass output.

The device can be configured to deliver specific configurations under pin control only, or additional configurations through an I^2C serial interface by an external processor.

The 8V41NS0412 is offered in a lead-free (RoHS6) 64-VFQFN package.

Typical Applications

- PCI Express Clocking
- 10G/40G/100G/400G Ethernet
- Gb Ethernet, Terabit IP switches / routers
- CPRI Interfaces
- Fiber Optics

Features

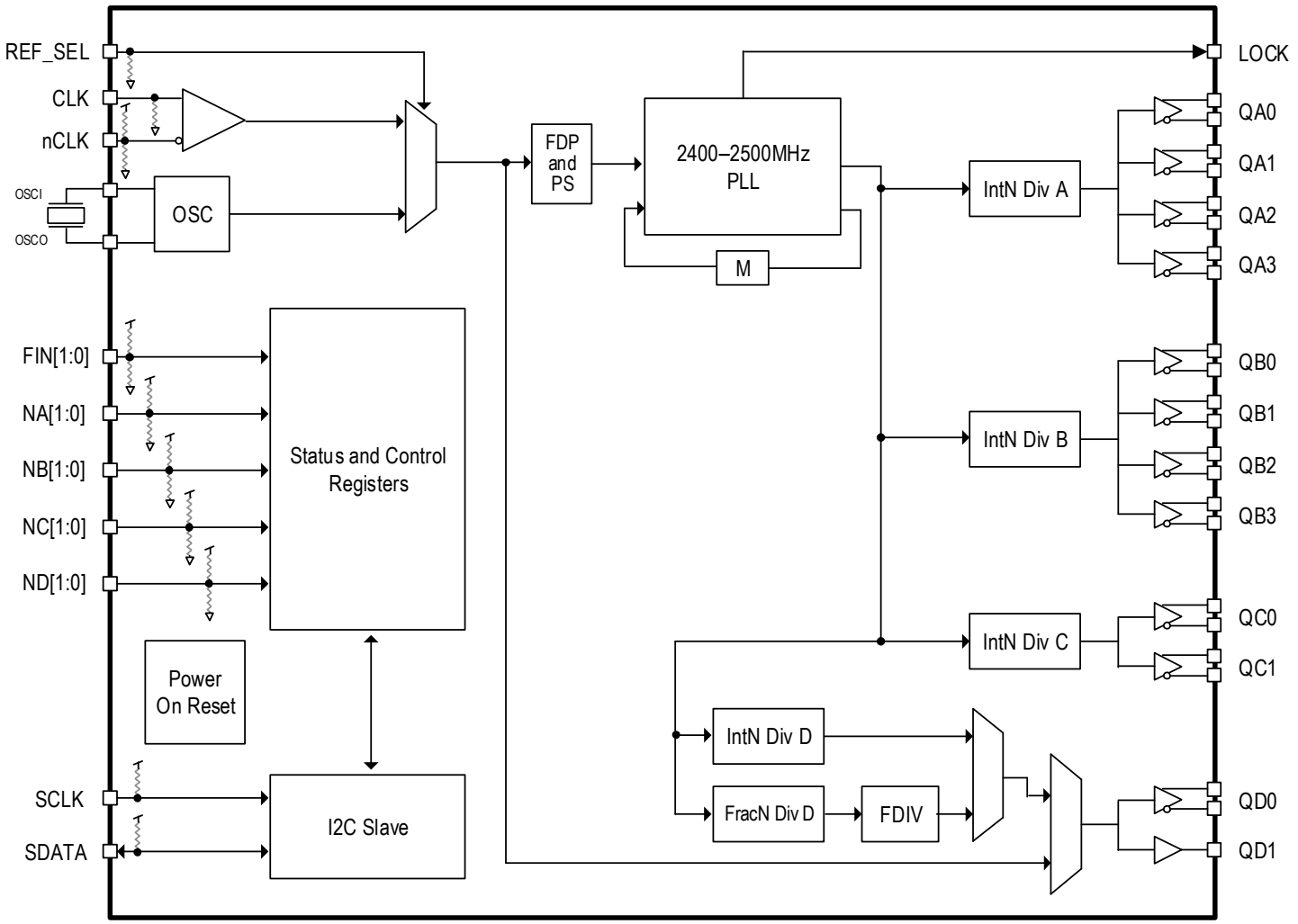
- Eleven differential HCSL outputs
- One LVCMOS output; input reference can be bypassed to this output
- The clock input operates in full differential mode (LVDS, LVPECL) or single-ended LVCMOS mode
- Driven from a crystal or differential clock input
- A 2.4–2.5GHz PLL frequency range supports Ethernet, SONET, and CPRI frequency plans
- 1.25GHz maximum output frequency
- Four integer output dividers with a range of output divide ratios (see Table 5)
- One fractional output divider can generate any desired output frequency
- Support of output power-down
- Excellent clock output phase noise

Offset Output	Frequency	Single-side Band Phase Noise
100kHz	156.25MHz	-143dBc/Hz

- Phase noise RMS, 156.25MHz, 12kHz to 20MHz integration range: 80fs (typical)
- Selected configurations can be controlled via the use of control input pins without need for serial port access
- LVCMOS compatible I^2C serial interface gives access to additional configurations by external processor or in combination with the control input pins
- Single 3.3V supply voltage
- Lead-free (RoHS 6) 64-VFQFN packaging
- -40°C to 85°C ambient operating temperature

Block Diagram

Figure 1. 8V41NS0412 Block Diagram

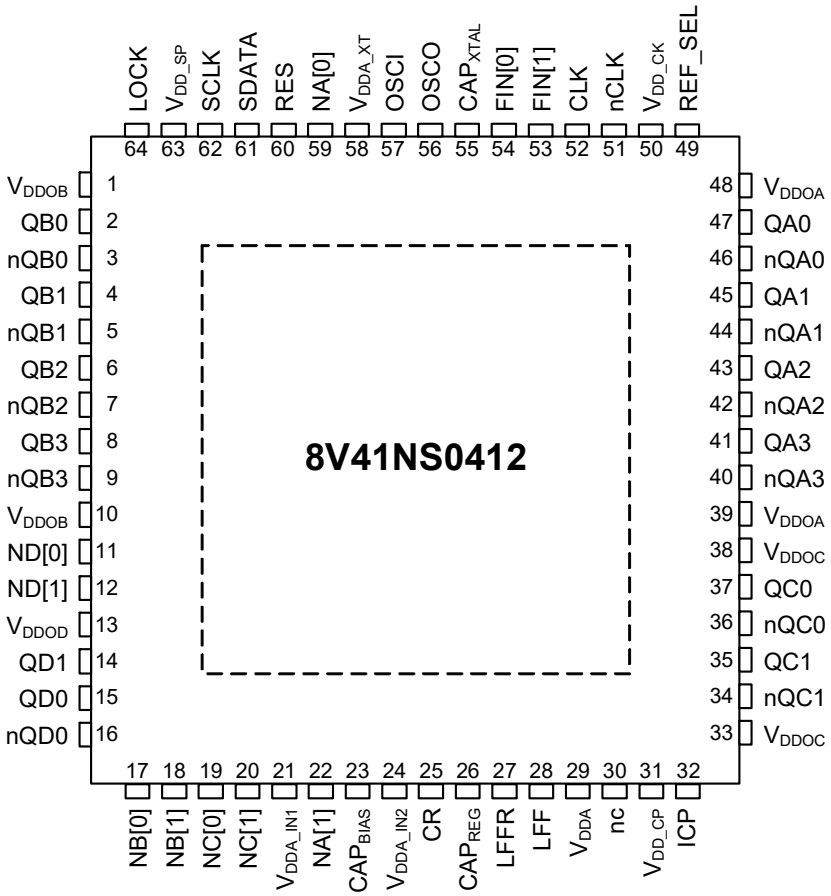


8V41NS0412 transistor count: 131,496

Contents

Pin Assignment

Figure 2. Pin Assignments for 9mm × 9mm 64-VFQFN Package – Top View



Pin Description

Table 1. Pin Descriptions[a]

Number	Name	Type	Description
1	V_{DDOB}	Power	Power supply voltage for output Bank B (3.3V).
2	QB0	Output	Differential clock output pair. HCSL interface levels.
3	nQB0	Output	
4	QB1	Output	Differential clock output pair. HCSL interface levels.
5	nQB1	Output	
6	QB2	Output	Differential clock output pair. HCSL interface levels.
7	nQB2	Output	
8	QB3	Output	Differential clock output pair. HCSL interface levels.
9	nQB3	Output	
10	V_{DDOB}	Power	Power supply voltage for output Bank B (3.3V).
11	ND[0]	Input (PU/PD)	Control input for output Bank D. 3-level signals (see Table 10).

Table 1. Pin Descriptions[a] (Cont.)

Number	Name	Type	Description
12	ND[1]	Input (PU/PD)	Control input for output Bank D. 3-level signals (see Table 10).
13	V_{DDOD}	Power	Power supply voltage for output Bank D (3.3V).
14	QD1	Output	Single-ended output clock. LVCMOS output levels.
15	QD0	Output	Differential clock output pair. HCSL interface levels.
16	nQD0	Output	
17	NB[0]	Input (PU/PD)	Control input for output Bank B. 3-level signals (see Table 8).
18	NB[1]	Input (PU/PD)	Control input for output Bank B. 3-level signals (see Table 8).
19	NC[0]	Input (PU/PD)	Control input for output Bank C. 3-level signals (see Table 9).
20	NC[1]	Input (PU/PD)	Control input for output Bank C. 3-level signals (see Table 9).
21	V_{DDA_IN1}	Power	Analog power supply voltage for PLL (3.3V).
22	NA[1]	Input (PU/PD)	Control input for output Bank A. 3-level signals (see Table 7).
23	CAP_{BIAS}	Analog	Internal VCO bias decoupling capacitor. Use a 4.7µF capacitor between the CAP_{BIAS} terminal and GND.
24	V_{DDA_IN2}	Power	Analog power supply voltage for VCO (3.3V).
25	CR	Analog	Internal VCO regulator decoupling capacitor. Use a 1µF capacitor between the CR and the V_{DDA} terminals.
26	CAP_{REG}	Analog	Internal VCO regulator decoupling capacitor. Use a 4.7µF capacitor between the CAP_{REG} terminal and GND.
27	LFFR	Analog	Ground return path pin for the PLL loop filter.
28	LFF	Output	Loop filter/charge pump output for the FemtoClock NG PLL. Connect to the external loop filter.
29	V_{DDA}	Power	Analog power supply voltage for VCO (3.3V).
30	nc	-	No connect. Do not use.
31	V_{DD_CP}	Power	Power supply voltage for PLL charge pump (3.3V).
32	ICP	Analog	Charge pump current input for PLL. Connect to LFF pin (28).
33	V_{DDOC}	Power	Power supply voltage for output Bank C (3.3V).
34	nQC1	Output	Differential clock output pair. HCSL interface levels.
35	QC1	Output	
36	nQC0	Output	Differential clock output pair. HCSL interface levels.
37	QC0	Output	
38	V_{DDOC}	Power	Power supply voltage for output Bank C (3.3V).
39	V_{DDOA}	Power	Power supply voltage for output Bank A (3.3V).

Table 1. Pin Descriptions[a] (Cont.)

Number	Name	Type	Description
40	nQA3	Output	Differential clock output pair. HCSL interface levels.
41	QA3	Output	
42	nQA2	Output	Differential clock output pair. HCSL interface levels.
43	QA2	Output	
44	nQA1	Output	Differential clock output pair. HCSL interface levels.
45	QA1	Output	
46	nQA0	Output	Differential clock output pair. HCSL interface levels.
47	QA0	Output	
48	V_{DDOA}	Power	Power supply voltage for output Bank A (3.3V).
49	REF_SEL	Input (PD)	Selects input reference source. LVCMOS interface levels. 0 = Crystal input on pins OSCI, OSCO (default) 1 = Reference clock input on pins CLK, nCLK
50	V_{DD_CK}	Power	Power supply voltage for input CLK, nCLK (3.3V).
51	nCLK	Input (PU/PD)	Inverting differential clock input. Internal resistor bias to $V_{DD\_CK}/2$.
52	CLK	Input (PD)	Non-inverting differential clock input.
53	FIN[1]	Input (PU/PD)	Control input for input reference frequencies. 3-level signals (see Table 3).
54	FIN[0]	Input (PU/PD)	Control input for input reference frequencies. 3-level signals (see Table 3).
55	CAP_{XTAL}	Analog	Crystal oscillator circuit decoupling capacitor. Use a 4.7µF capacitor between the CAP_{XTAL} and GND terminals.
56	OSCO	Output	Crystal oscillator interface.
57	OSCI	Input	Crystal oscillator interface.
58	V_{DDA_XT}	Power	Analog power supply voltage for the crystal oscillator (3.3V).
59	NA[0]	Input (PU/PD)	Control input for output Bank A. 3-level signals (see Table 7).
60	RES	Analog	Connect a 2.8kΩ (±2%) resistor to GND for output current calibration.
61	SDATA	I/O (PU)	I^2C data input/output. LVCMOS interface levels. Open-drain pin.
62	SCLK	Input (PU)	I^2C clock input. LVCMOS interface levels.
63	V_{DD_SP}	Power	Power supply voltage for the I^2C port (3.3V).
64	LOCK	Output	Lock status output. LVCMOS interface levels. Logic low = PLL not locked Logic high = PLL locked
ePad	GND	Power	Power supply ground. Exposed pad must be connected to ground.

[a] Internal pull-up (PU) and pull-down (PD) resistors are indicated in parentheses. For typical values, see Table 19.

Principles of Operation

The 8V41NS0412 can be locked to either an input reference clock or a 10MHz to 50MHz fundamental-mode crystal and generate a wide range of synchronized output clocks. Lock status can be monitored via the LOCK pin. For example, it could be used in either the transmit or receive path of Synchronous Ethernet or SONET/SDH equipment.

The 8V41NS0412 accepts a differential or single-ended input clock ranging from 5MHz up to 1GHz. It generates up to twelve output clocks with up to four different output frequencies, ranging from 10.91MHz up to 1.25GHz.

The device outputs are divided into four output banks. Each bank supports conversion of the input frequency to a different output frequency: one independent or integer related output frequency on Bank D (QD[0:1]). Three additional integer related frequencies are on Bank A (QA[0:3]), Bank B (QB[0:3]) and Bank C (QC[0:1]). All outputs within a bank will have the same frequency.

The device is programmable through an I^2C serial interface by an external processor or via control input pins.

Pin versus Register Control

The 8V41NS0412 can be configured by the use of input control pins and/or over an I^2C serial port. The pins / registers used to control each function are shown in Table 2. At power-up, control of each function is via the control input pins. Access over the serial port can change each function individually to be controlled by registers. This allows for any mixture of register or pin control. However any of the indicated functions can only be controlled by register or by pin at any given time, not by both. Use of register control will allow access to a wider range of configuration options but values are lost on power-down. If the output bank or PLL is controlled by control input pins (at power-up or through the Control Select bit), corresponding register values remain unchanged and have no impact on device functions.

Table 2. Control of Specific Functions

Function	Control Select Bit	Control Input Pins	Register Fields Affected
Prescaler and PLL Feedback divider	FIN_CTL	FIN[1:0]	PS[5:0], FDP, M[8:0]
Bank A Divider and output type	NA_CTL	NA[1:0]	NA[5:0], PD_A, PD_QAx
Bank B Divider and output type	NB_CTL	NB[1:0]	NB[5:0], PD_B, PD_QBx
Bank C Divider and output type	NC_CTL	NC[1:0]	NC[5:0], PD_C, PD_QCx
Bank D Divider and output type	ND_CTL	ND[1:0]	ND[5:0], ND_FINT[3:0], ND_FRAC[23:0], ND_DIVF[1:0], ND_DIV, ND_SRC, PD_D, PD_QDx

Changes to the control pins while the part is active are allowed, but limited and cannot be guaranteed a glitch-free output transition. During the state transition of the control pins, the output phase alignment (synchronization) may be lost and Bank D outputs in Fractional Mode (FOD) may not be available. If the I^2C registers are accessible, then assertion of the INIT_CLK bit or powering down and then powering up the device will restore phase alignment and activate the Fractional output frequency.

Glitch-free operation can be performed by disabling the outputs using the I^2C-accessible registers, then re-enabling once changes are completed.

Any change to the output dividers performed over the I^2C interface must be followed by an assertion of the INIT_CLK register bit to force the loading of the new divider values, as well as to synchronize the output dividers.

Input Clock Selection (REF_SEL)

The 8V41NS0412 needs to be provided with an input reference frequency either from its crystal input pins (OSCI, OSCO) or its reference clock input pins (CLK, nCLK). The REF_SEL input pin controls which source is used.

The crystal input on the 8V41NS0412 is capable of being driven by a parallel-resonant, fundamental mode crystal with a frequency of 10MHz to 50MHz.

The crystal input also supports being driven by a single-ended crystal oscillator or reference clock, but only a frequency from 10MHz to 50MHz can be used on these pins.

The reference clock input accepts clocks with frequencies ranging from 5MHz up to 1GHz. The input can accept LVPECL, LVDS, LVHSTL, HCSL, or LVCMOS inputs using 2.5V or 3.3V logic levels as shown in Applications Information.

Prescaler and PLL Configuration

When the input frequency (f_{IN}), whether generated by a crystal or clock input is known, and the desired PLL operating frequency has been determined, several constraints need to be met:

- The Phase/ Frequency Detector operating frequency (f_{PFD}) must be within the specified limits shown in Table 27. This is controlled by selecting a doubler (FDP) or an appropriate prescaler (PS) value. If multiple values are possible, a higher f_{PFD} will provide better phase noise performance.
- The VCO operating frequency (f_{VCO}) must be within the specified limits shown in Table 27. This is controlled by selecting an appropriate PLL feedback divider (M) value. Note that it may be necessary to choose a different prescaler value if the limits cannot be met by the available values of M. It may also be necessary to select an appropriate input frequency value.

Several preset configurations can be selected directly from the FIN[1:0] control input pins. These configurations are based on a particular input frequency f_{IN} and a particular f_{VCO} (see Table 3). These selections apply whether the input frequency is provided from the crystal or reference clock inputs

Table 3. Input Selection Control

FIN[1]	FIN[0]	f_{IN} (MHz)	f_{VCO} (MHz)
High	High	38.88	2488.32
High	Middle[a]	38.4	2457.6
High	Low	31.25	2500
Middle	High	312.5	2500
Middle	Middle	125	2500
Middle	Low	156.25	2500
Low	High	100	2500
Low	Middle	25	2500
Low	Low	50	2500

[a] A “middle” voltage level is defined in Table 22. Leaving the input pin open will also generate this level via a weak internal resistor network.

Alternatively, the user can directly access the registers for M, FDP, and PS over the serial interface for a wider range of options (see Table 4 for some examples).

Inputs do not support transmission of spread-spectrum clocking sources. Since this family is intended for high-performance applications, it will assume input reference sources to have stabilities of ±100ppm or better.

Table 4. PLL Frequency Control Examples

f_{IN} (MHz)	PS	FDP	f_{PFD} (MHz)	M	PLL Operating Frequency (MHz)
25	1	2	50	50	2500
39.0625	1	2	78.125	32	2500
50	1	2	100	25	2500
100	1	1	100	25	2500
125	1	1	125	20	2500
156.25	1	1	156.25	16	2500
200	2	1	100	25	2500
250	2	1	125	20	2500
312.5	2	1	156.25	16	2500
400	4	1	100	25	2500
500	4	1	125	20	2500
625	4	1	156.25	16	2500
19.44	1	2	38.88	64	2488.32
38.88	1	2	77.76	32	2488.32
38.4	1	2	76.8	32	2457.6

PLL Loop Bandwidth

The 8V41NS0412 PLL requires external loop components (resistor and capacitors) connecting in between ICP and LFF pins. The PLL loop bandwidth generally depends on the loop components, charge pump current, PFD frequency, and VCO gain.

Output Divider Frequency Sources

Output dividers associated with banks A, B and C take their input frequency directly from the PLL. Bank D also has the option to bypass the input frequency (after mux) directly to the output.

Integer Output Dividers (Banks A, B, C, and D)

The 8V41NS0412 supports four integer output dividers: one per output bank. Each integer output divider block independently supports one of several divide ratios as shown in their respective register descriptions (Table 13, Table 14, Table 15, or Table 16). Selected divide ratios can be chosen directly from the control input pins for that particular output bank. The remaining ratios can only be selected via the serial interface. Bank D may choose whether to use the integer divider or a separate fractional divider to generate the output frequency.

Some example output frequencies are shown in Table 5 for the minimum f_{VCO} (2400MHz), the maximum f_{VCO} (2500MHz) and two other common VCO frequencies. With appropriate input frequencies and configuration selections, any f_{VCO} and f_{OUT} between the minimum and maximum can be generated.

Table 5. Integer Output Divider Control Examples

Divide Ratio	f_{OUT} (MHz)			
	f_{VCO} = 2400MHz	f_{VCO} = 2457.6MHz	f_{VCO} = 2488.32MHz	f_{VCO} = 2500MHz
2	1200	1228.8	1244.16	1250
4	600	614.4	622.08	625
5	480	491.52	497.664	500
6	400	409.6	414.72	416.667
8	300	307.2	311.04	312.5
9	266.667	273.07	276.48	277.78
10	240	245.76	248.832	250
12	200	204.8	207.36	208.333
16	150	153.6	155.52	156.25
18	133.333	136.533	138.24	138.889
20	120	122.88	124.416	125
25	96	98.3	99.53	100
32	75	76.8	77.76	78.125
36	66.667	68.267	69.12	69.444
40	60	61.44	62.208	62.5
50	48	49.152	49.766	50
64	37.5	38.4	38.88	39.063
72	33.333	34.133	34.56	34.722
80	30	30.72	31.104	31.25
100	24	24.576	24.883	25
128	18.75	19.2	19.44	19.531
160	15	15.36	15.552	15.625
200	12	12.29	12.44	12.5
220	10.91	11.17	11.31	11.36

Fractional Output Divider (Bank D)

For the fractional output divider in Bank D, the output divide ratio is given by:

$$f_{OUT} = \frac{f_{VCO}}{2 \times \left(FINT + \frac{FRAC}{2^{24}}\right) \times (FDIV)}$$

Where,

- FINT = Integer part: 5, 6, ...(2^4-1) – given by ND_FINT[3:0]
- FRAC = Fractional part: 0, 1, 2, ...(2^{24}-1) – given by ND_FRAC[23:0]
- FDIV = post-divider: 1, 2 or 4 – given by ND_DIVF[1:0]

This provides a frequency range of 20 to 250MHz.

Output Drivers

Each of the four output banks are provided with pin or register-controlled output drivers. Differential outputs can be individually selected as HCSL or POWER-DOWN. When powered-down, both outputs of the differential output pair and the single-ended QD1 output will be in High-Impedance state.

Note that under pin-control, all differential outputs within an output bank will assume the same configuration. Pin-control does not allow configuration of individual outputs within a bank.

Pin Control of the Output Frequencies and Protocols

For pin-control settings, see Table 6 to Table 10. All of the output frequencies assume f_{VCO} = 2500MHz. With different f_{VCO} configurations, the pins may still be used to select the indicated divide ratios for each bank, but the f_{OUT} will be different.

The control pins do not affect the internal register values but act directly on the output structures. As a result, register values will not change to match the control input pin selections.

Each output bank can be powered up/down and enabled/ disabled by register bits. In the disabled state, an output will drive a logic low level. The default state is all outputs enabled. Pin-control does not require register access to enable the outputs. Additionally, individual outputs within a bank can be powered up/down by register bits only.

Table 6. Definition of Output Disabled / Power-down[a]

Output Condition	Q_{MN}[b]	nQ_{MN}[c]	QD1
DISABLED (register-control only)	LOW	HIGH	LOW
Buffer POWER-DOWN (pin-control or register-control)	High-Impedance	High-Impedance	High-Impedance

[a] Do not terminate the differential outputs when DISABLED or POWER-DOWN.

[b] Q_{MN} refers to output pins QA[0:3], QB[0:3], QC[0:1], and QD0.

[c] nQ_{MN} refers to output pins nQA[0:3], nQB[0:3], nQC[0:1], and nQD0.

Table 7. Bank A Divider / Driver Pin-Control
(3-level control signals)

NA[1]	NA[0]	Output Type	Divide Ratio	f_{OUT} (MHz)
Low	Low	HCSL	16	156.25
Low	Middle	HCSL	10	250
Low	High	HCSL	8	312.5
Middle	Low	HCSL	5	500
Middle	Middle	PD[a]	–	–
Middle	High	HCSL	20	125
High	Low	HCSL	25	100
High	Middle	HCSL	50	50
High	High	Reserved[b]		

[a] PD denotes Power-down.

[b] It is imperative not to connect or switch NA[1] and NA[0] pins to HIGH/Power Supply (V_{DD}) at any time

Table 8. Bank B Divider / Driver Pin-Control
(3-level control signals)

NB[1]	NB[0]	Output Type	Divide Ratio	f_{OUT} (MHz)
Low	Low	HCSL	16	156.25
Low	Middle	HCSL	10	250
Low	High	HCSL	8	312.5
Middle	Low	HCSL	5	500
Middle	Middle	PD[a]	–	–
Middle	High	HCSL	20	125
High	Low	HCSL	25	100
High	Middle	HCSL	50	50
High	High	HCSL	100	25

[a] PD denotes Power-down.

Table 9. Bank C Divider / Driver Pin-Control
(3-level control signals)

NC[1]	NC[0]	Output Type	Divide Ratio	f_{OUT} (MHz)
Low	Low	HCSL	16	156.25
Low	Middle	HCSL	10	250
Low	High	HCSL	8	312.5
Middle	Low	HCSL	5	500
Middle	Middle	PD[a]	–	–
Middle	High	HCSL	20	125
High	Low	HCSL	25	100
High	Middle	HCSL	50	50
High	High	HCSL	100	25

[a] PD denotes Power-down.

Table 10. Bank D Divider / Driver Pin-Control
(3-level control signals)

ND[1]	ND[0]	QD0	QD1	Divide Ratio	f_{OUT} (MHz)
		Output Type			
Low	Low	HCSL	Hi-Imp[a]	16	156.25
Low	Middle	HCSL	Hi-Imp	20	125
Low	High	HCSL	Hi-Imp	25	100
Middle	Low	PD	LVCMOS	75	33.333
Middle	Middle	PD[b]	Hi-Imp	-	–
Middle	High	–	–	–	–
High	Low	HCSL	Hi-Imp	18.75	133.33
High	Middle	HCSL	Hi-Imp	37.5	66.66
High	High	HCSL	LVCMOS	N/A	f_{IN}

[a] Hi-Imp denotes High-Impedance.

[b] PD denotes Power-down.

Device Start-up and Reset Behavior

The 8V41NS0412 has an internal power-on reset (POR) circuit. The POR circuit will remain active for a maximum of 175msec after device power-up when recommended CR (pin 25) value is used, 1.0uF. For faster power-up to Lock Time, a minimum CR value of 0.1uF can be used.

While in the reset state (POR active), the device will operate as follows:

1. All registers will return to and be held in their default states as indicated in the applicable register description.
2. All internal state machines will be in their reset conditions.
3. The serial interface will not respond to read or write cycles.
4. Lock status will be cleared.

Upon the internal POR circuit expiring, the device will exit reset and begin self-configuration. Self-configuration initiates the loading of appropriate values indicated by the control input pins and the default values into the registers indicated in the register descriptions.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock the PLL to the input frequency, if available. Once the PLL is locked, all the outputs will be synchronized.

Serial Control Port Description

Serial Control Port Configuration Description

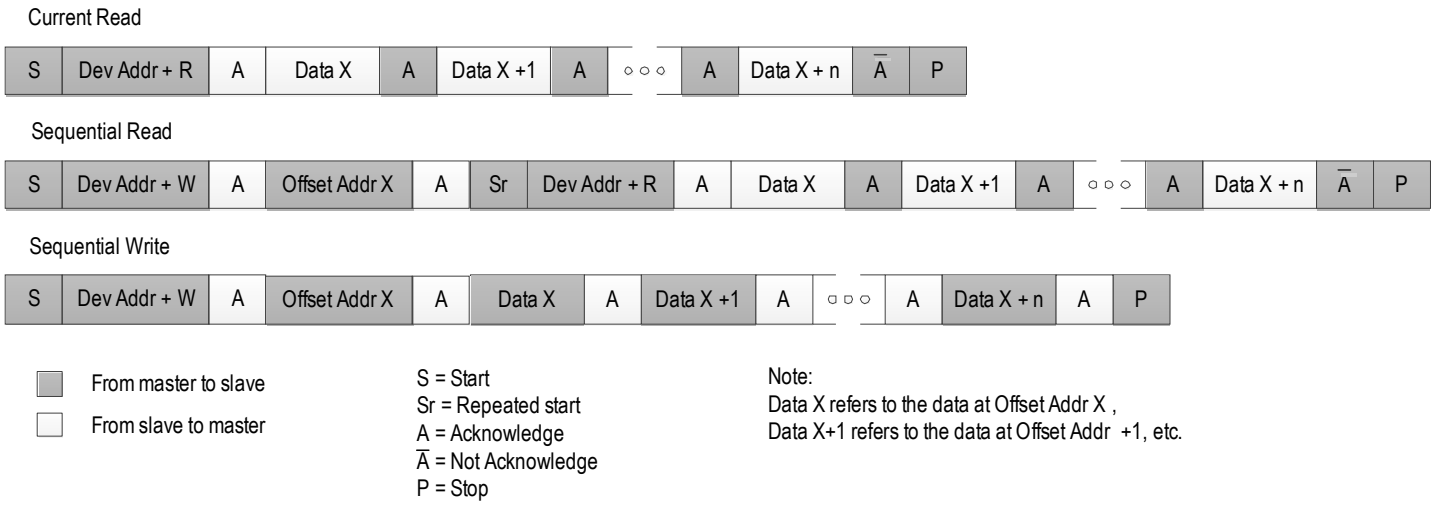
The 8V41NS0412 has a serial control port that can respond as a slave in an I^2C compatible configuration at a base address of 1101100b, to allow access to any of the internal registers for device programming or examination of internal status.

I^2C Mode Operation

The I^2C interface is designed to fully support v1.2 of the I^2C Specification for Fast mode operation. The 8V41NS0412 acts as a slave device on the I^2C bus at 400kHz using a fixed base address of 1101100b. The interface accepts byte-oriented block write and block read operations. One address byte specifies the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer.

For full electrical I^2C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

Figure 3. I^2C Slave Read and Write Cycle Sequencing



Register Description

Table 11. Register Blocks

Register Ranges Offset (Hex)	Register Block Description
00–08	Prescaler and PLL Control Registers
09–0F	Reserved[a]
10–17	Bank A Control Registers
18–1F	Bank B Control Registers
20–27	Bank C Control Registers
28–31	Bank D Control Registers
32–3C	Reserved
3D–40	Device Control Registers
41–FF	Reserved

[a] Reserved registers should not be written to and have indeterminate read values.

Table 12. Prescaler and PLL Control Register Bit Field Locations and Descriptions

Prescaler and PLL Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00	Rsvd	Rsvd	PS[5:0]					
01	Rsvd							FDP
02	Rsvd						FIN_CTL	OSC_LOW
03	Rsvd							
04	Rsvd							M[8]
05	M[7:0]							
06	Rsvd							
07	Rsvd							
08	Rsvd			CP[4:0]				

Prescaler and PLL Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
PS[5:0]	R/W	000000b	Prescaler – scales input frequency by the value: 00h = Reserved 01h – 3Fh = divide by the value used (e.g. 04 = divide-by-4) Note: When FDP = 1, prescalar values are ignored and have no impact on device functions.
FDP	R/W	1b	Input Frequency Doubler: 0 = Disabled 1 = Enabled
FIN_CTL	R/W	0b	Prescaler and PLL Configuration Control: 0 = PS, FDP, and M settings determined by FIN[1:0] control pins 1 = PS, FDP, and M settings determined by register settings over I^2C
OSC_LOW	R/W	0b	Crystal Oscillator Gain Control Selection: 0 = Normal gain for crystal frequencies of 25MHz and up 1 = Low gain for crystal frequencies less than 25MHz
M[8:0]	R/W	019h	PLL Feedback Divider Ratio: 000h–003h = Reserved (do not use) 004h–1FFh = Divide f_{VCO} by the value (e.g. 04 = divide by -4)
CP[4:0]	R/W	11001b	PLL Charge Pump Current Control: I_{CP} = 200µA × (CP[4:0] + 1) Maximum charge pump current is 6.4mA. Default setting is 5.2mA: ((25 + 1) × 200µA).
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 13. Bank A Control Register Bit Field Locations and Descriptions

Bank A Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
10	Rsvd		NA[5:0]					
11	Rsvd							
12	PD_A	Rsvd						NA_CTL
13	Rsvd							
14	PD_QA0	Rsvd						
15	PD_QA1	Rsvd						
16	PD_QA2	Rsvd						
17	PD_QA3	Rsvd						

Bank A Control Register Block Field Descriptions					
Bit Field Name[a]	**Field Type**	**Default Value**	**Description**		
NA[5:0]	R/W	0Dh	Divider Ratio for Bank A: Any changes made to this register will not take effect until the INIT_CLK register bit is toggled.		
			00 0000b = Reserved		
			00 0001b = Reserved	01 0110b = ÷30	10 1011b = ÷88
			00 0010b = ÷2	01 0111b = ÷32	10 1100b = ÷90
			00 0011b = ÷3	01 1000b = ÷33	10 1101b = ÷96
			00 0100b = ÷4	01 1001b = ÷35	10 1110b = ÷100
			00 0101b = ÷5	01 1010b = ÷36	10 1111b = ÷108
			00 0110b = ÷6	01 1011b = ÷40	11 0000b = ÷110
			00 0111b = ÷8	01 1100b = ÷42	11 0001b = ÷112
			00 1000b = ÷9	01 1101b = ÷44	11 0010b = ÷120
			00 1001b = ÷10	01 1110b = ÷45	11 0011b = ÷128
			00 1010b = ÷12	01 1111b = ÷48	11 0100b = ÷132
			00 1011b = ÷14	10 0000b = ÷50	11 0101b = ÷140
			00 1100b = ÷15	10 0001b = ÷54	11 0110b = ÷144
			00 1101b = ÷16	10 0010b = ÷55	11 0111b = ÷160
			00 1110b = ÷18	10 0011b = ÷56	11 1000b = ÷176
			00 1111b = ÷20	10 0100b = ÷60	11 1001b = ÷180
			01 0000b = ÷21	10 0101b = ÷64	11 1010b = ÷200
			01 0001b = ÷22	10 0110b = ÷66	11 1011b = ÷220
			01 0010b = ÷24	10 0111b = ÷70	11 1100b = Reserved
			01 0011b = ÷25	10 1000b = ÷72	11 1101b = Reserved
			01 0100b = ÷27	10 1001b = ÷80	11 1110b = Reserved
			01 0101b = ÷28	10 1010b = ÷84	11 1111b = Reserved

Bank A Control Register Block Field Descriptions			
Bit Field Name[a]	**Field Type**	**Default Value**	**Description**
PD_A	R/W	0b	Power-down Bank A: 0 = Bank A and all QA outputs powered and operate normally. 1 = Bank A and all QA outputs powered-down. When powering-down the output bank, it is recommended to also write a 1 to the PD_QAx registers.
NA_CTL	R/W	0b	Bank A Configuration Control: 0 = NA[5:0] and PD_A settings are determined by NA[1:0] control pins 1 = NA[5:0] and PD_A settings are determined by register settings over I^2C
PD_QAx	R/W	0b	Power-down Output QAx: 0 = QAx output powered and operates normally 1 = QAx output powered-down
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

[a] Where x = 0, 1, 2, or 3.

Table 14. Bank B Control Register Bit Field Locations and Descriptions

Bank B Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18	Rsvd		NB[5:0]					
19	Rsvd							
1A	PD_B	Rsvd						NB_CTL
1B	Rsvd							
1C	PD_QB0	Rsvd						
1D	PD_QB1	Rsvd						
1E	PD_QB2	Rsvd						
1F	PD_QB3	Rsvd						

Bank B Control Register Block Field Descriptions					
Bit Field Name[a]	**Field Type**	**Default Value**	**Description**		
NB[5:0]	R/W	0Dh	Divider Ratio for Bank B: Any changes made to this register will not take effect until the INIT_CLK register bit is toggled.		
			00 0000b = Reserved		
			00 0001b = Reserved	01 0110b = ÷30	10 1011b = ÷88
			00 0010b = ÷2	01 0111b = ÷32	10 1100b = ÷90
			00 0011b = ÷3	01 1000b = ÷33	10 1101b = ÷96
			00 0100b = ÷4	01 1001b = ÷35	10 1110b = ÷100
			00 0101b = ÷5	01 1010b = ÷36	10 1111b = ÷108
			00 0110b = ÷6	01 1011b = ÷40	11 0000b = ÷110
			00 0111b = ÷8	01 1100b = ÷42	11 0001b = ÷112
			00 1000b = ÷9	01 1101b = ÷44	11 0010b = ÷120
			00 1001b = ÷10	01 1110b = ÷45	11 0011b = ÷128
			00 1010b = ÷12	01 1111b = ÷48	11 0100b = ÷132
			00 1011b = ÷14	10 0000b = ÷50	11 0101b = ÷140
			00 1100b = ÷15	10 0001b = ÷54	11 0110b = ÷144
			00 1101b = ÷16	10 0010b = ÷55	11 0111b = ÷160
			00 1110b = ÷18	10 0011b = ÷56	11 1000b = ÷176
			00 1111b = ÷20	10 0100b = ÷60	11 1001b = ÷180
			01 0000b = ÷21	10 0101b = ÷64	11 1010b = ÷200
			01 0001b = ÷22	10 0110b = ÷66	11 1011b = ÷220
			01 0010b = ÷24	10 0111b = ÷70	11 1100b = Reserved
			01 0011b = ÷25	10 1000b = ÷72	11 1101b = Reserved
			01 0100b = ÷27	10 1001b = ÷80	11 1110b = Reserved
			01 0101b = ÷28	10 1010b = ÷84	11 1111b = Reserved

Bank B Control Register Block Field Descriptions			
Bit Field Name[a]	**Field Type**	**Default Value**	**Description**
PD_B	R/W	0b	Power-down Bank B: 0 = Bank B and all QB outputs powered and operate normally 1 = Bank B and all QB outputs powered-down. When powering-down the output bank, it is recommended to also write a 1 to the PD_QBx registers.
NB_CTL	R/W	0b	Bank B Configuration Control: 0 = NB[5:0] and PD_B settings are determined by NB[1:0] control pins 1 = NB[5:0] and PD_B settings are determined by register settings over I^2C
PD_QBx	R/W	0b	Power-down Output QBx: 0 = QBx output powered and operates normally. 1 = QBx output powered-down
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

[a] Where x = 0, 1, 2, or 3.

Table 15. Bank C Control Register Bit Field Locations and Descriptions

Bank C Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
20	Rsvd		NC[5:0]					
21	Rsvd							
22	PD_C	Rsvd						NC_CTL
23	Rsvd							
24	PD_QC0	Rsvd						
25	PD_QC1	Rsvd						

Bank C Control Register Block Field Descriptions					
Bit Field Name[a]	**Field Type**	**Default Value**	**Description**		
NC[5:0]	R/W	0Dh	Divider Ratio for Bank C: Any changes made to this register will not take effect until the INIT_CLK register bit is toggled.		
			00 0000b = Reserved 00 0001b = Reserved 00 0010b = ÷2 00 0011b = ÷3 00 0100b = ÷4 00 0101b = ÷5 00 0110b = ÷6 00 0111b = ÷8 00 1000b = ÷9 00 1001b = ÷10 00 1010b = ÷12 00 1011b = ÷14 00 1100b = ÷15 00 1101b = ÷16 00 1110b = ÷18 00 1111b = ÷20 01 0000b = ÷21 01 0001b = ÷22 01 0010b = ÷24 01 0011b = ÷25 01 0100b = ÷27 01 0101b = ÷28	01 0110b = ÷30 01 0111b = ÷32 01 1000b = ÷33 01 1001b = ÷35 01 1010b = ÷36 01 1011b = ÷40 01 1100b = ÷42 01 1101b = ÷44 01 1110b = ÷45 01 1111b = ÷48 10 0000b = ÷50 10 0001b = ÷54 10 0010b = ÷55 10 0011b = ÷56 10 0100b = ÷60 10 0101b = ÷64 10 0110b = ÷66 10 0111b = ÷70 10 1000b = ÷72 10 1001b = ÷80 10 1010b = ÷84	10 1011b = ÷88 10 1100b = ÷90 10 1101b = ÷96 10 1110b = ÷100 10 1111b = ÷108 11 0000b = ÷110 11 0001b = ÷112 11 0010b = ÷120 11 0011b = ÷128 11 0100b = ÷132 11 0101b = ÷140 11 0110b = ÷144 11 0111b = ÷160 11 1000b = ÷176 11 1001b = ÷180 11 1010b = ÷200 11 1011b = ÷220 11 1100b = Reserved 11 1101b = Reserved 11 1110b = Reserved 11 1111b = Reserved
PD_C	R/W	0b	Power-down Bank C: 0 = Bank C and all QC outputs powered and operate normally 1 = Bank C and all QC outputs powered-down. When powering-down the output bank, it is recommended to also write a 1 to the PD_QCx registers.		

Bank C Control Register Block Field Descriptions			
Bit Field Name[a]	**Field Type**	**Default Value**	**Description**
NC_CTL	R/W	0b	Bank C Configuration Control: 0 = NC[5:0] and PD_C settings are determined by NC[1:0] control pins 1 = NC[5:0] and PD_C settings are determined by register settings over I^2C
PD_QCx	R/W	0b	Power-down Output QCx: 0 = QCx output powered and operates normally. 1 = QCx output powered-down.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

[a] Where x = 0 or 1.

Table 16. Bank D Control Register Bit Field Locations and Descriptions

Bank D Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
28	ND_FRAC[7:0]							
29	ND_FRAC[15:8]							
2A	ND_FRAC[23:16]							
2B	Rsvd				ND_FINT[3:0]			
2C	Rsvd		ND[5:0]					
2D	Rsvd				ND_DIVF[1:0]		ND_DIV	ND_SRC
2E	PD_D	Rsvd						ND_CTL
2F	Rsvd							
30	PD_QD0	Rsvd						
31	PD_QD1	Rsvd						

Bank D Control Register Block Field Descriptions			
Bit Field Name[a]	**Field Type**	**Default Value**	**Description**
ND_FRAC[23:0]	R/W	600000h	Fractional portion of divider ratio for fractional divider for Bank D: Fraction used in divide ratio = ND_FRAC[23:0] / 2^{24}
ND_FINT[3:0]	R/W	1001b	Integer portion of divider ratio for fractional divider for Bank D: 0h–4h= Reserved 5h–Fh = divide by the value used (e.g. 5 = divide-by-5)

Bank D Control Register Block Field Descriptions			
Bit Field Name[a]	**Field Type**	**Default Value**	**Description**
ND[5:0]	R/W	0Dh	Divider Ratio for Bank D: Any changes made to this register will not take effect until the INIT_CLK register bit is toggled. 00 0000b = Reserved 00 0001b = Reserved 00 0010b = ÷ 2 00 0011b = ÷ 3 00 0100b = ÷ 4 00 0101b = ÷ 5 00 0110b = ÷ 6 00 0111b = ÷ 8 00 1000b = ÷ 9 00 1001b = ÷ 10 00 1010b = ÷ 12 00 1011b = ÷ 14 00 1100b = ÷ 15 00 1101b = ÷ 16 00 1110b = ÷ 18 00 1111b = ÷ 20 01 0000b = ÷ 21 01 0001b = ÷ 22 01 0010b = ÷ 24 01 0011b = ÷ 25 01 0100b = ÷ 27 01 0101b = ÷ 28 01 0110b = ÷ 30 01 0111b = ÷ 32 01 1000b = ÷ 33 01 1001b = ÷ 35 01 1010b = ÷ 36 01 1011b = ÷ 40 01 1100b = ÷ 42 01 1101b = ÷ 44 01 1110b = ÷ 45 01 1111b = ÷ 48 10 0000b = ÷ 50 10 0001b = ÷ 54 10 0010b = ÷ 55 10 0011b = ÷ 56 10 0100b = ÷ 60 10 0101b = ÷ 64 10 0110b = ÷ 66 10 0111b = ÷ 70 10 1000b = ÷ 72 10 1001b = ÷ 80 10 1010b = ÷ 84 10 1011b = ÷ 88 10 1100b = ÷ 90 10 1101b = ÷ 96 10 1110b = ÷ 100 10 1111b = ÷ 108 11 0000b = ÷ 110 11 0001b = ÷ 112 11 0010b = ÷ 120 11 0011b = ÷ 128 11 0100b = ÷ 132 11 0101b = ÷ 140 11 0110b = ÷ 144 11 0111b = ÷ 160 11 1000b = ÷ 176 11 1001b = ÷ 180 11 1010b = ÷ 200 11 1011b = ÷ 220 11 1100b = Reserved 11 1101b = Reserved 11 1110b = Reserved 11 1111b = Reserved Note: QD1 CMOS output should be powered-off for output frequencies greater than the maximum listed for it in Table 27.
ND_DIVF[1:0]	R/W	00b	Post-divider Ratio for fractional divider for Bank D: 00 = ÷1 01 = ÷2 10 = ÷4 11 = Reserved
ND_DIV	R/W	0b	Control which divider is used to provide output frequency for Bank D: 0 = Integer divider D (ND configures this) 1 = Fractional mode (ND_FINT, ND_FRAC and ND_DIVF configure this)
ND_SRC	R/W	0b	Output Source Selection for Bank D: 0 = Bank D is driven from the integer or fractional divider as selected by ND_DIV 1 = Bank D is driven from the input reference (after the input mux)

Bank D Control Register Block Field Descriptions			
Bit Field Name[a]	**Field Type**	**Default Value**	**Description**
PD_D	R/W	0b	Power-down Bank D: 0 = Bank D and all QD outputs powered and operate normally. 1 = Bank D and all QD outputs powered-down. QD1 output is in High-Impedance. When powering-down the output Bank, it is recommended to also write a 1 to the PD_QDx registers.
ND_CTL	R/W	0b	Bank D Configuration Control: 0 = ND[5:0], ND_FRAC[23:0], ND_FINT[3:0], ND_DIVF[1:0], ND_DIV, ND_SRC, PD_D, and PD_QD1 settings are determined by ND[1:0] control pins. 1 = ND[5:0], ND_FRAC[23:0], ND_FINT[3:0], ND_DIVF[1:0], ND_DIV, ND_SRC, PD_D, and PD_QD1 settings are determined by register settings over I^2C.
PD_QDx	R/W	0b	Power-down Output QDx: 0 = QDx outputs powered and operate normally. 1 = QD0 output powered-down.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

[a] Where x = 0 or 1.

Table 17. Device Control Register Bit Field Locations and Descriptions

Device Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
3D	INIT_CLK	Rsvd						
3E	RELOCK	Rsvd						
3F	PB_CAL	Rsvd						
40	Rsvd				EN_A	EN_B	EN_C	EN_D

Device Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
INIT_CLK	W/O[a]	0b	Writing a 1 to this bit location will cause output dividers to be synchronized. Must be done every time a divider value is changed. This bit will auto-clear.
RELOCK	W/O[a]	0b	Writing a 1 to this bit location will cause the PLL to re-lock. This bit will auto-clear.
PB_CAL	W/O[a]	0b	Precision Bias Calibration: Setting this bit to 1 will start the calibration of an internal precision bias current source. The bias current is used as reference for outputs configured as reference for the charge pump currents. This bit will auto-clear.
EN_A	R/W	1b	Output Enable Control for Bank A: 0 = Bank A outputs QA[0:3] disabled to logic-low state (QAx = 0, nQAx = 1) 1 = Bank A outputs QA[0:3] enabled
EN_B	R/W	1b	Output Enable Control for Bank B: 0 = Bank B outputs QB[0:3] disabled to logic-low state (QBx = 0, nQBx = 1) 1 = Bank B outputs QB[0:3] enabled
EN_C	R/W	1b	Output Enable Control for Bank C: 0 = Bank C outputs QC[0:1] disabled to logic-low state (QCx = 0, nQCx = 1) 1 = Bank C outputs QC[0:1] enabled
EN_D	R/W	1b	Output Enable Control for Bank D: 0 = Bank D outputs QD[0:1] disabled to logic-low state (QD0 = 0, nQD0 = 1, QD1 = 0) 1 = Bank D outputs QD[0:1] enabled Note: If Bank D is powered down via the PD_D bit or the QD1 output is powered down by the PD_QD1 bit, then QD1 will be in High-Impedance regardless of the state of this bit.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

[a] These bits are read as 0. When a 1 is written to them, it will have the indicated effect and then self-clear back to 0.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8V41NS0412 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 18. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD}	3.6V
Inputs, V_I OSCI Other Inputs	 -0.5V to 3.6V -0.5V to 3.6V
Outputs, V_O (LVCMOS)	-0.5V to 3.6V
Outputs, V_O (HCSL)	-0.5V to V_{DD} +0.5V
Maximum Junction Temperature, t_{JMAX}	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 19. Input Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance[a]			3.5		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

[a] This specification does not apply to OSCI and OSCO pins.

Table 20. Output Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{OUT}	Output Impedance	LOCK	V_{DD}[a] = 3.3V		20		W
		QD1			30		W

[a] V_{DD} denotes V_{DD_SP}, V_{DDOD}.

Table 21. Power Supply DC Characteristics, V_{DD_x}[a] = V_{DDOX}[b] = 3.3V ±5%, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD_X}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA_X}[c]	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDOX}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD_X}[d]	Core Supply Voltage			90	110	mA
I_{DDA_X}[e]	Analog Supply Current			138	165	mA
I_{DDOX}[f][g]	Output Supply Current	All differential outputs are enabled but not loaded[h]		225	265	mA
		All differential outputs are enabled but not loaded – QD1 output is powered down		200	235	mA

[a] V_{DD_x} denotes V_{DD_CP}, V_{DD_CK}, V_{DD_SP}.

[b] V_{DDOX} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}.

[c] V_{DDA_X} denotes V_{DDA_IN1}, V_{DDA_IN2}, V_{DDA}, V_{DDA_XT}.

[d] I_{DD_X} denotes I_{DD_CP}, I_{DD_CK}, I_{DD_SP}.

[e] I_{DDA_X} denotes I_{DDA_IN1}, I_{DDA_IN2}, I_{DDA}, I_{DDA_XT}.

[f] Internal maximum dynamic switching current is included.

[g] I_{DDOX} denotes I_{DDOA}, I_{DDOB}, I_{DDOC}, I_{DDOD}.

[h] QD1 output is terminated with 50Ω to V_{DDOX}/2.

Table 22. LVCMOS DC Characteristics for 3-level Pins, V_{DD_X}[a] = V_{DDOX}[b] = 3.3V ±5%, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	FIN[1:0], NA[1:0], NB[1:0], NC[1:0], ND[1:0]		0.7 × V_{DD}[c]		3.465	V
V_{IM}	Input Middle Voltage			0.4 × V_{DD}[c]		0.6 × V_{DD}[c]	V
V_{IL}	Input Low Voltage			-0.3		0.3 × V_{DD}[c]	V
I_{IH}	Input High Current	FIN[1:0], NA[1:0], NB[1:0], NC[1:0], ND[1:0]	V_{DD}[c] = V_{IN} = 3.465V			150	µA
I_{IM}	Input Middle Current	FIN[1:0], NA[1:0], NB[1:0], NC[1:0], ND[1:0]	V_{IN} = V_{DD}[c] / 2		±1		µA
I_{IL}	Input Low Current	FIN[1:0], NA[1:0], NB[1:0], NC[1:0], ND[1:0]	V_{DD}[c] = 3.465V, V_{IN} = 0V	-150			µA

[a] V_{DD_x} denotes V_{DD_CP}, V_{DD_CK}, V_{DD_SP}.

[b] V_{DDOX} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}.

[c] V_{DD} denotes V_{DDA_IN1}, V_{DD_CK}.

Table 23. LVCMOS DC Characteristics for 2-level Pins, V_{DD_X}[a] = V_{DDOX}[b] = 3.3V ±5%, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			0.7 × V_{DD}[c]		3.465	V
V_{IL}	Input Low Voltage	REF_SEL		-0.3		0.3 × V_{DD}[c]	V
		SDATA, SCLK		-0.3		0.15 × V_{DD}[c]	V
I_{IH}	Input High Current	SCLK, SDATA	V_{DD}[c] = V_{IN} = 3.465V			5	µA
		REF_SEL	V_{DD}[c] = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	SCLK, SDATA	V_{DD}[c] = 3.465V, V_{IN} = 0V	-150			µA
		REF_SEL	V_{DD}[c] = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	LOCK	I_{OH} = -4mA	2.2			V
V_{OL}	Output Low Voltage	SDATA, LOCK	I_{OL} = 4mA			0.45	V

[a] V_{DD_x} denotes V_{DD_CP}, V_{DD_CK}, V_{DD_SP}.

[b] V_{DDOX} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}.

[c] V_{DD} denotes V_{DD_CK}, V_{DD_SP}.

Table 24. Differential Input DC Characteristics, V_{DD_X}[a] = V_{DDOX}[b] = 3.3V ±5%, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK_IN, nCLK_IN	V_{DD}[c] = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_IN	V_{DD}[c] = 3.465V, V_{IN} = 0V	-5			µA
		nCLK_IN	V_{DD}[c] = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-peak Voltage[d], [e]	CLK_IN, nCLK_IN		0.2		1.4	V
V_{CMR}	Common Mode Input Voltage[d][e]	CLK_IN, nCLK_IN		GND + 1.1		V_{DD}[c] – 0.3	V

[a] V_{DD_x} denotes V_{DD_CP}, V_{DD_CK}, V_{DD_SP}.

[b] V_{DDOX} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}.

[c] V_{DD} denotes V_{DD_CK}.

[d] Common mode voltage is defined as the cross point.

[e] Input voltage cannot be less than GND – 300mV or more than V_{DD}.

Table 25. LVCMOS DC Characteristics for QD1 Output, V_{DD_x}[a] = V_{DDOD} = 3.3V+/-5%

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	QD1, I_{OH} = -8mA	2.6			V
V_{OL}	Output Low Voltage	QD1, I_{OL} = 8mA			0.5	V

[a] V_{DD_x} denotes V_{DD_CP}, V_{DD_CK}, V_{DD_SP}.

Table 26. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		50	MHz
Equivalent Series Resistance (ESR)	> 32 MHz			30	Ω
	≤ 32 MHz			50	
Load Capacitance (C_L)	50MHz Crystal		8	12	pF
	25MHz Crystal		12	22	
Shunt Capacitance	> 32 MHz			3	pF
	≤ 32 MHz			7	pF
Maximum Crystal Drive Level			200		µW
Frequency Stability (total)		−100		100	ppm

AC Electrical Characteristics

Table 27. AC Characteristics[a] V_{DD_X}[b] = V_{DDOX}[c] = 3.3V +5%, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Frequency			2400		2500	MHz
f_{PFD}	Phase / Frequency Detector Frequency			5		200	MHz
f_{OUT}	Output Frequency	QA[0:3] nQA[0:3] QB[0:3] nQB[0:3] QC[0:1] nQC[0:1]		10.91		1250	MHz
		QD0, nQD0	Integer divider selected	10.91		1250	MHz
			Fractional divider selected	20		250	MHz
		QD1	Integer divider selected	10.91		250	MHz
			Fractional divider selected	20		250	MHz
*t*sk(b)	Bank Skew[d][e][f]	Bank A				45	ps
		Bank B				45	
		Bank C				20	
t_R / t_F	Output Rise/Fall Time	QA[0:3] nQA[0:3] QB[0:3] nQB[0:3] QC[0:1] nQC[0:1] QD0, nQD0	20% to 80%			325	ps
		QD1	20% to 80%		700	1100	
odc	Output Duty Cycle[g]	QA[0:3] nQA[0:3] QB[0:3] nQB[0:3] QC[0:1] nQC[0:1], QD0, nQD0		45	50	55	%
		QD1	F_{OUT} < 156.25MHz	45	50	55	%
			$F_{OUT} \geq$ 156.25MHz	40	50	60	%
t_{LOCK}	PLL Lock Time[h]				10		ms

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] V_{DD_x} denotes V_{DD_CP}, V_{DD_CK}, V_{DD_SP}.

[c] V_{DDOX} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}.

[d] Defined as skew among outputs from same bank at the same supply voltage with equal load conditions. Measured at the output differential crosspoints.

[e] This parameter is defined in accordance with JEDEC Standard 65.

[f] This parameter is guaranteed by characterization. Not tested in production

[g] Duty cycle of bypassed signals (input reference clock or crystal input) is not adjusted by the device.

[h] PLL lock time is defined as time from input clock availability to frequency locked output. The following loop filter component values can be used: R_Z = 150Ω, C_Z = 0.1µF C_P = 200pF. For more information, see Applications Information.

Table 28. Qmn[a] and QD1 Phase Noise and Jitter Characteristics, V_{DD_X}[b] = V_{DDOX}[c] = 3.3V+5%, T_A = -40°C to +85°C[d][e][f][g]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
*t*jit(Ø)	RMS Phase Jitter random	Qmn = 156.25MHz	Integration range: 12kHz – 20MHz		80	95	fs
	RMS Phase Jitter random	Qmn = 125MHz	Integration range: 12kHz – 20MHz		81		fs
	RMS Phase Jitter random	Qmn = 100MHz	Integration range: 12kHz – 20MHz		105		fs
	RMS Phase Jitter random	Qmn = 25MHz	Integration range: 12kHz – 5MHz		172		fs
	RMS Phase Jitter random	QD0 = 133.3333MHz (fractional)[h]	Integration range: 12kHz – 20MHz		115		fs
	RMS Phase Jitter random	QD1= 125MHz	Integration range: 12kHz – 20MHz		170		fs
	RMS Phase Jitter random[i]	QAn = 156.25MHz	Integration range: 12kHz – 20MHz		110		fs
		QBn = 100MHz	Integration range: 12kHz – 20MHz		120		fs
		QCn = 25MHz	Integration range: 12kHz – 5MHz		172		fs
		QD0 = 133.3333MHz (fractional)	Integration range: 12kHz – 20MHz		115		fs
Φ_N(10)	Single-side Band Noise Power, 10Hz from carrier		Qmn = 156.25MHz		-78		dBc/Hz
Φ_N(100)	Single-side Band Noise Power, 100Hz from carrier		Qmn = 156.25MHz		-115.4		dBc/Hz
Φ_N(1k)	Single-side Band Noise Power, 1kHz from carrier		Qmn = 156.25MHz		-130.5		dBc/Hz
Φ_N(10k)	Single-side Band Noise Power, 10kHz from carrier		Qmn = 156.25MHz		-137.6		dBc/Hz
Φ_N(100k)	Single-side Band Noise Power, 100kHz from carrier		Qmn = 156.25MHz		-143.6		dBc/Hz
Φ_N(1M)	Single-side Band Noise Power, 1MHz from carrier		Qmn = 156.25MHz		-154.7		dBc/Hz
Φ_N(10M)	Single-side Band Noise Power, 10MHz from carrier		Qmn = 156.25MHz		-162		dBc/Hz
Φ_N(∝)	Noise Floor (≥30MHz from carrier)		Qmn = 156.25MHz		-162.1		dBc/Hz

[a] Qmn denotes the differential outputs QA[0:3], QB[0:3], QC[0:1] or QD0.

[b] V_{DD_x} denotes V_{DD_CP}, V_{DD_CK}, V_{DD_SP}.

[c] V_{DDOX} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}.

[d] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[e] All outputs enabled and configured for the same output frequency unless otherwise noted.

[f] Characterized using a 50MHz crystal unless otherwise noted.

[g] The following loop filter component values were used: R_Z = 150Ω, C_Z = 0.1µF, CP = 200pF. PLL charge pump current control set at 5.2mA.

[h] QAx = 156.25MHz, QBx = 156.25MHz, QCx = 156.25MHz and QD1 = OFF.

[i] QAx = 156.25MHz, QBx = 100MHz, QCx = 25MHz, QD0 = 133.3333MHz (fractional) and QD1 = OFF.

Table 29. HCSL AC Characteristics[a] V_{DD_X}[b] = V_{DDOX}[c] = 3.3V+5%, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{RB}	Ring-Back Voltage Margin[d] [e]	Q[A:D], nQ[A:D]		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed[d] [e]	Q[A:D], nQ[A:D]		500			ps
V_{MAX}	Absolute Max Output Voltage[f] [g]	Q[A:D], nQ[A:D]				1150	mV
V_{MIN}	Absolute Min output voltage[f] [h]	Q[A:D], nQ[A:D]		-300			mV
V_{CROSS}	Absolute Crossing voltage[f] [i] [j]	Q[A:D], nQ[A:D]		200		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges[f] [k]	Q[A:D], nQ[A:D]				140	mV
t_{SLEW+}	Rising Edge Rate[d] [l]	Q[A:D], nQ[A:D]		1.3		6.8	V/ns
t_{SLEW-}	Falling Edge Rate[d] [l]	Q[A:D], nQ[A:D]		1.3		6.8	V/ns

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] V_{DD_x} denotes V_{DD_CP}, V_{DD_CK}, V_{DD_SP}.

[c] V_{DDOX} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}.

[d] Measurement taken from differential waveform.

[e] t_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV range.

[f] Measurement taken from single-ended waveform.

[g] Defined as the maximum instantaneous voltage including overshoot.

[h] Defined as the minimum instantaneous voltage including undershoot.

[i] Measured at the crossing point where the instantaneous voltage value of the rising edge of Q[Ax:Dx] equals the falling edge of nQ[Ax:Dx].

[j] Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

[k] Defined as the total variation of all crossing voltages of rising Q[Ax:Dx] and falling nQ[Ax:Dx]. This is the maximum allowed variance in V_{cross} for any particular system.

[l] Measured from -150mV to +150mV on the differential waveform (derived from Q[Ax:Dx] minus nQ[Ax:Dx]). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

Table 30. PCI Express Jitter Specifications, [a] V_{DD_X}[b] = V_{DDOX}[c] = 3.3V +5%, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions[d]	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_j(PCIe Gen 1)	Phase Jitter Peak-to-peak[e] [f]	Evaluation Band: 0Hz – Nyquist (clock frequency/2)		6.1		86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter, RMS[f] [g]	High Band: 1.5MHz – Nyquist (clock frequency/2)		0.4		3.10	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter, RMS[f] [g]	Low Band: 10kHz – 1.5MHz		0.13		3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter, RMS[f] [h]	Evaluation Band: 0Hz – Nyquist (clock frequency/2)		0.08		0.8	ps

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] V_{DD_x} denotes V_{DD_CP}, V_{DD_CK}, V_{DD_SP}.

[c] V_{DDOX} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}.

[d] f = 100MHz, 50MHz Crystal input and Doubler is ON (FDP = 1)

[e] Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.

[f] This parameter is guaranteed by characterization. Not tested in production.

[g] RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).

[h] RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.

Phase Noise Plots

Figure 4. Typical Phase Noise at 156.25MHz

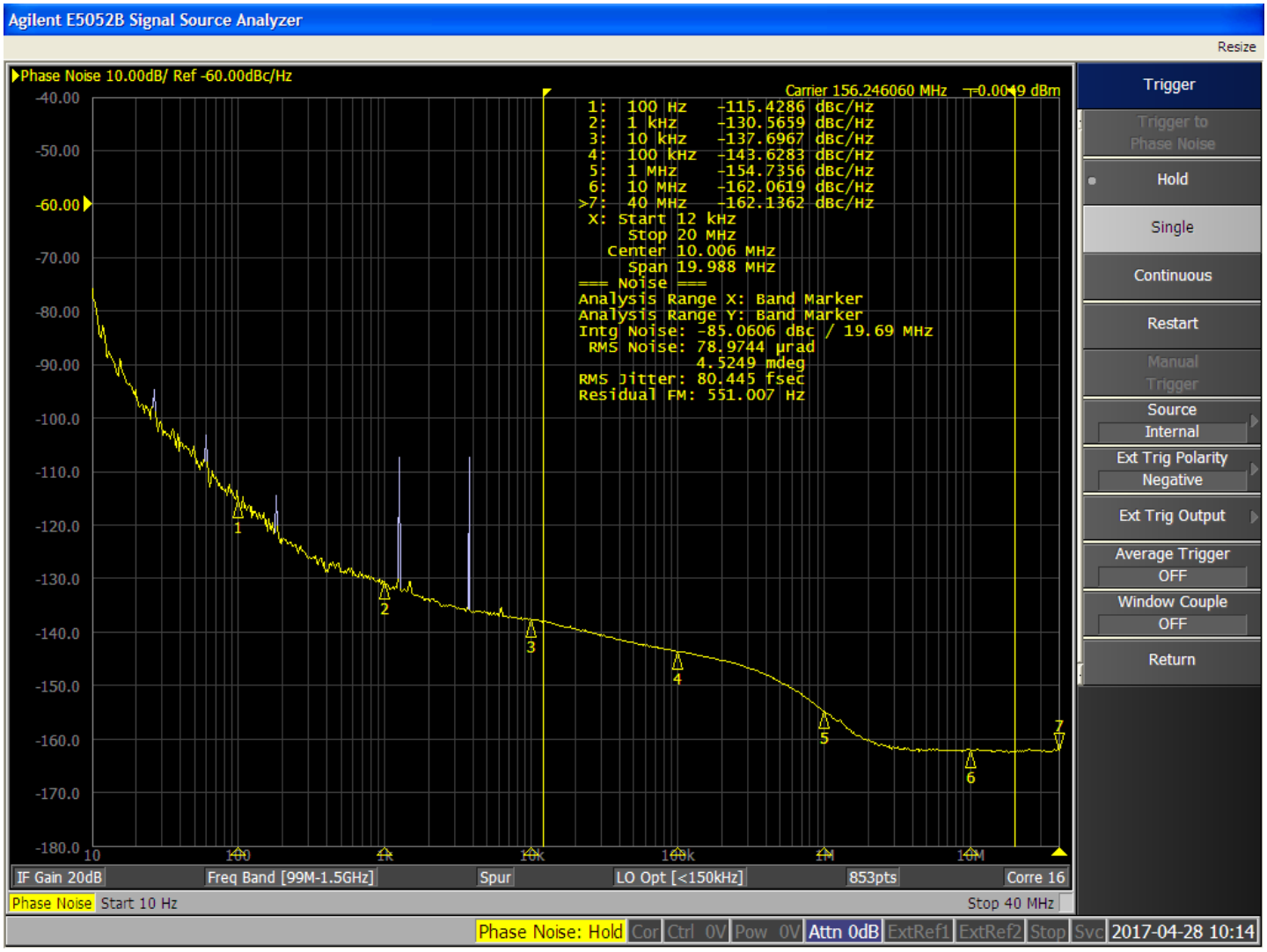


Figure 5. Typical Phase Noise at 125MHz

Applications Information

Recommendations for Unused Input and Output Pins

Inputs

LVCMOS Control Pins

All control pins have internal pull-up and/or pull-down resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs

HCSL Outputs

All unused differential outputs can be left floating. We recommended that there is no trace attached.

LVCMOS Output

QD1 output can be left floating if unused. There should be no trace attached.

Overdriving the XTAL Interface

The OSCI input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The OSCO pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 6 shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver.

Figure 6. LVCMOS Driver to XTAL Input Interface

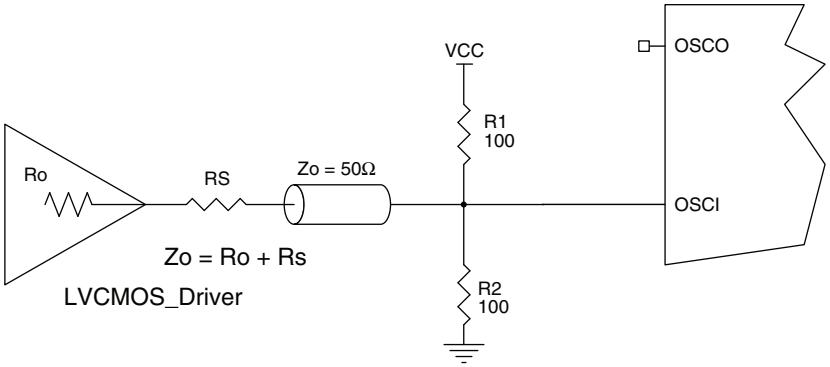
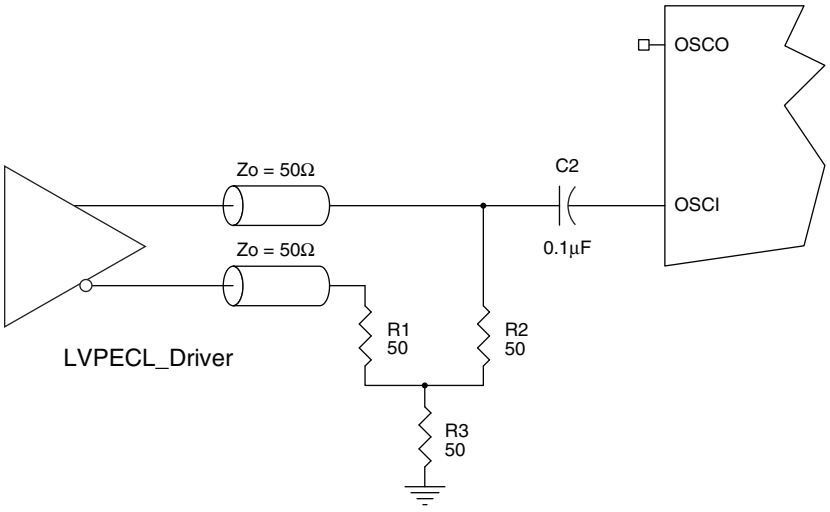


Figure 7 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the OSCI input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

Figure 7. LVPECL Driver to XTAL Input Interface

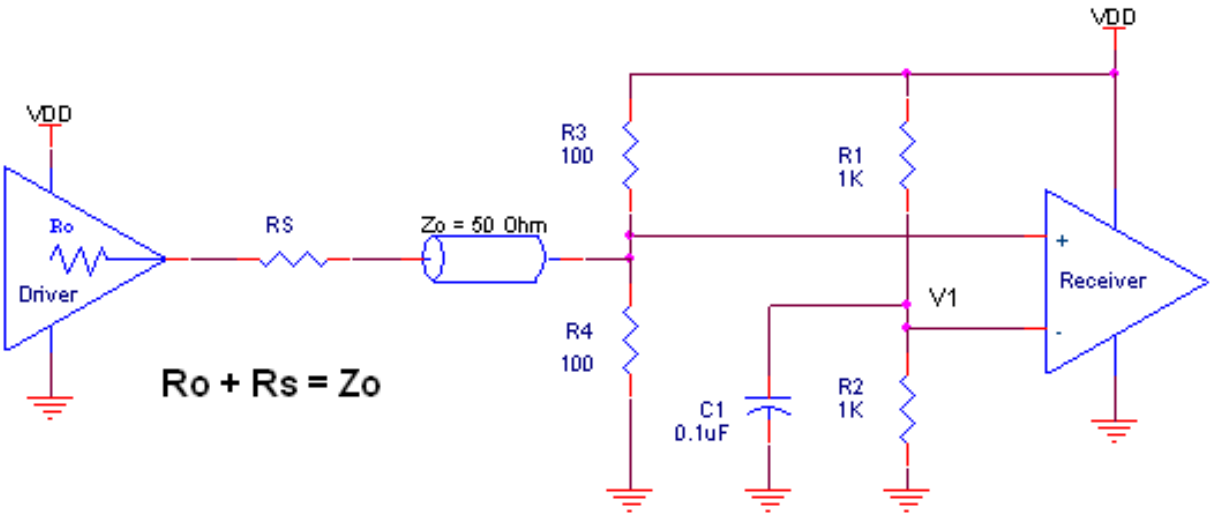


Wiring the Differential Input to Accept Single-Ended Levels

Figure 8 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Suggested edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

Figure 8. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



3.3V Differential Clock Input Interface

CLK/nCLK accepts LVDS, LVPECL and other differential signals. Both V_{SWING} and V_{OX} must meet the V_{PP} and V_{CMR} input requirements. Figure 9 to Figure 11 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples of direct-coupled termination only.

Figure 9. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

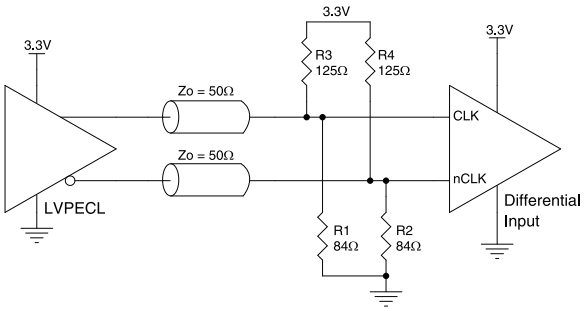


Figure 10. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

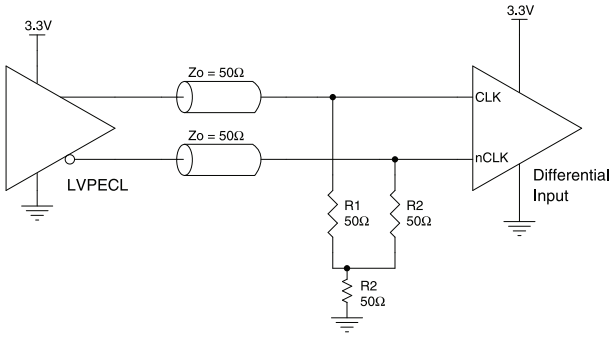
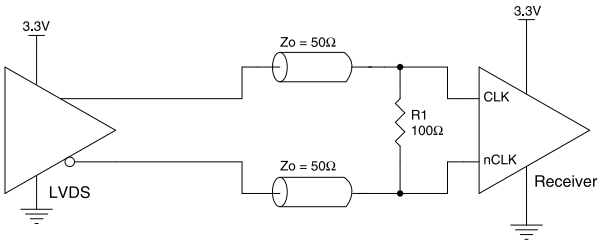


Figure 11. CLK/nCLK Input Driven by a 3.3V LVDS Driver



Recommended Termination

Figure 12 is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 12. Recommended Source Termination (Where the Driver and Receiver will be on Separate PCBs)

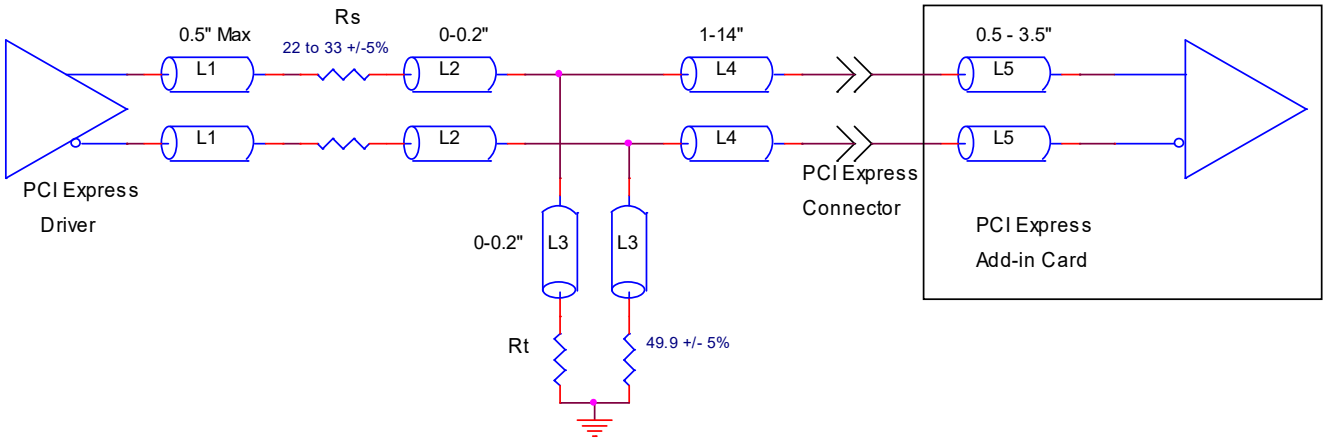
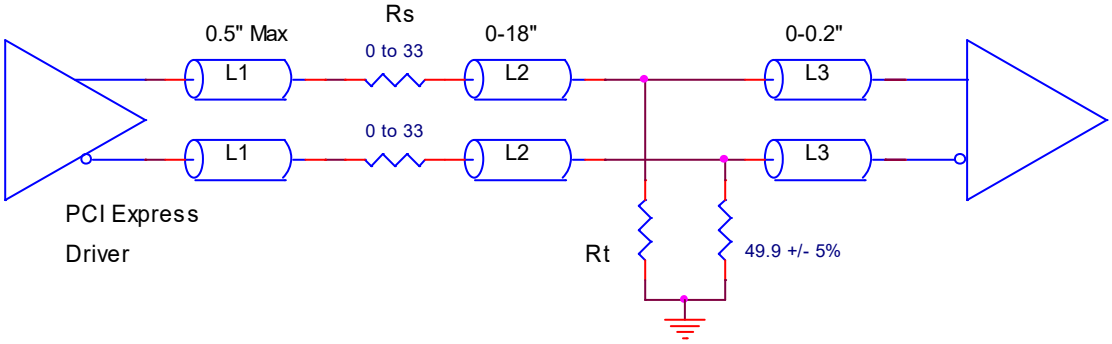


Figure 13 is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 13. Recommended Termination (Where a Point-to-Point Connection can be used)



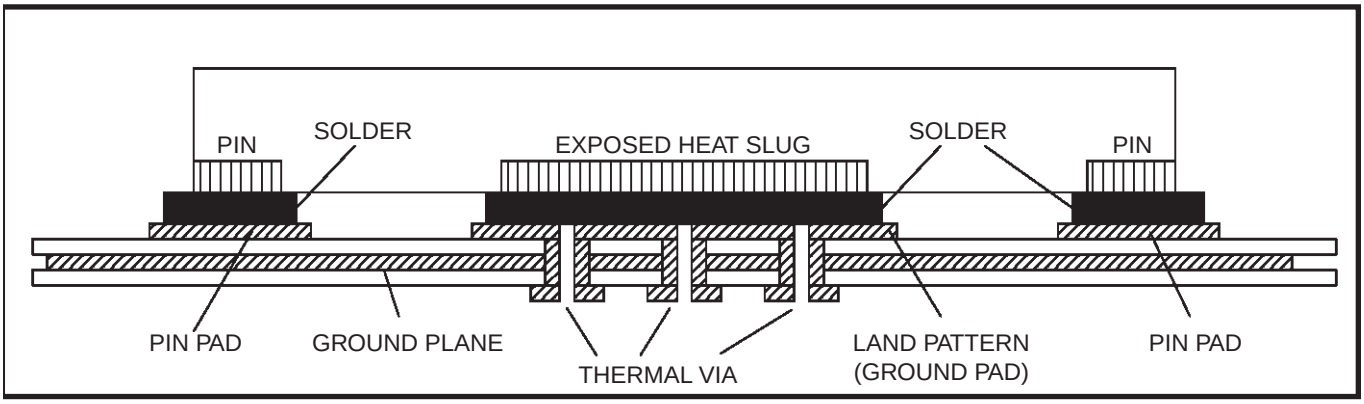
VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 14. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. Renesas recommends to use as many vias connected to ground as possible. It also recommends that the via diameter should be 12 to 13 mils (0.30 to 0.33 mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern.

Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

Figure 14. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to Scale)



PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

In the jitter analysis, the transmit (Tx) and receive (Rx) SerDes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

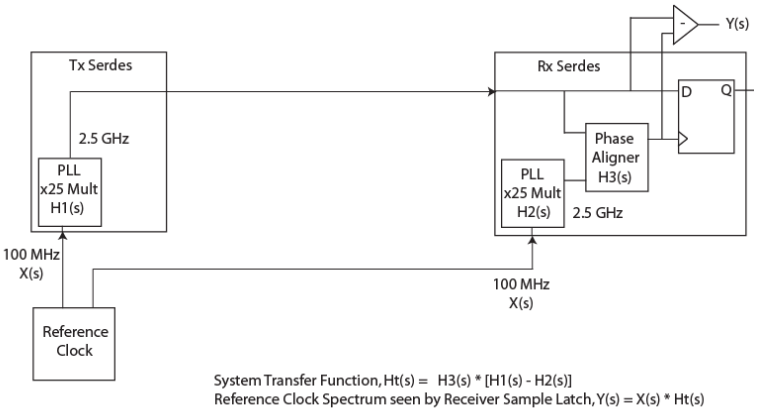
$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

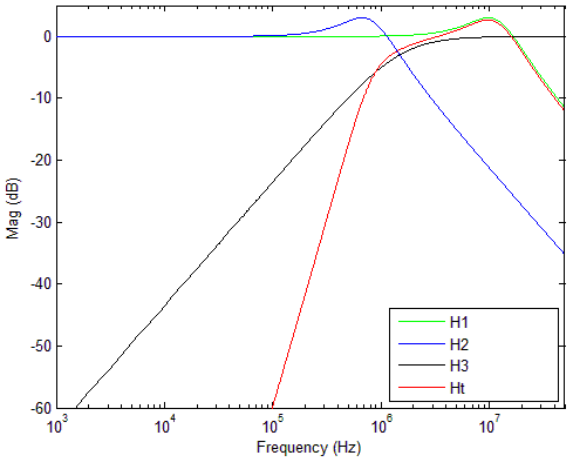
In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s) × H3(s) × [H1(s) – H2(s)].

Figure 15. PCI Express Common Clock Architecture



For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g. for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

Figure 16. PCIe Gen 1 Magnitude of Transfer Function



For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (low band) and 1.5MHz – Nyquist (high band). The plots show the individual transfer functions as well as the overall transfer function Ht.

Figure 17. PCIe Gen 2A Magnitude of Transfer Function

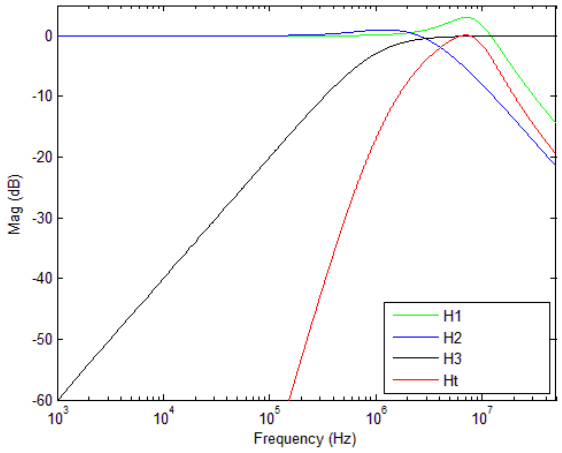
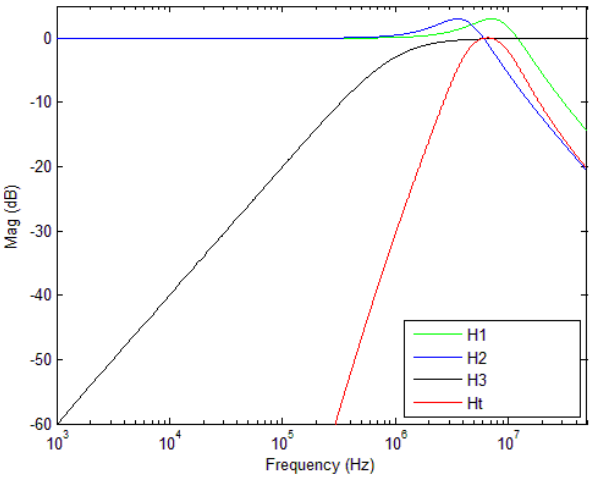
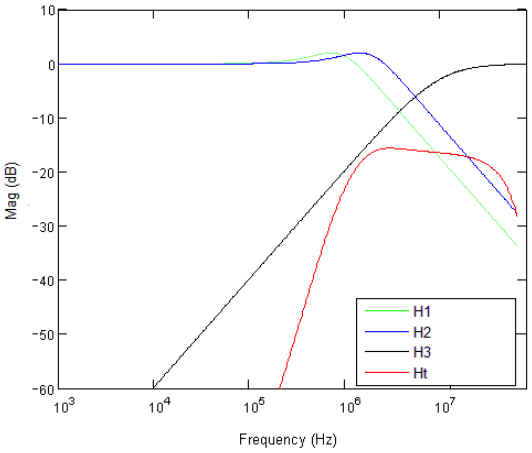


Figure 18. PCIe Gen 2B Magnitude of Transfer Function



For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.

Figure 19. PCIe Gen 3 Magnitude of Transfer Function



For a more thorough overview of PCI Express jitter analysis methodology, please refer to Renesas application note, *PCI Express Reference Clock Requirements.*

Schematic and Layout Recommendations

Figure 20 and Figure 21 show an example 8V41NS0412 application schematic operating the device at V_{CC} = 3.3V. This example focuses on functional connections and is not configuration specific. Refer to Pin Description to ensure that the logic control inputs are properly set for the application.

Figure 20. 8V41NS0412 Application Schematic – Page 1

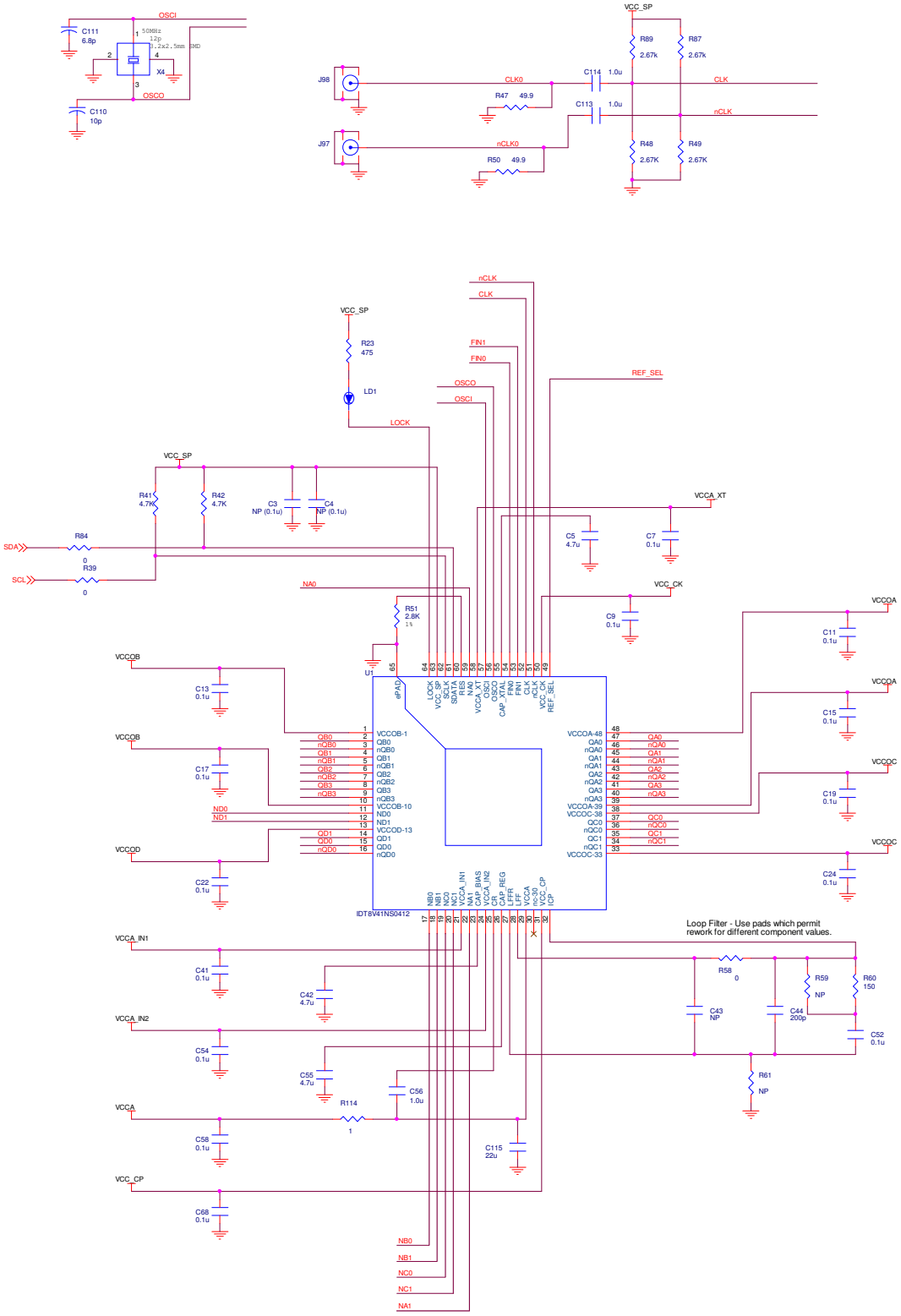
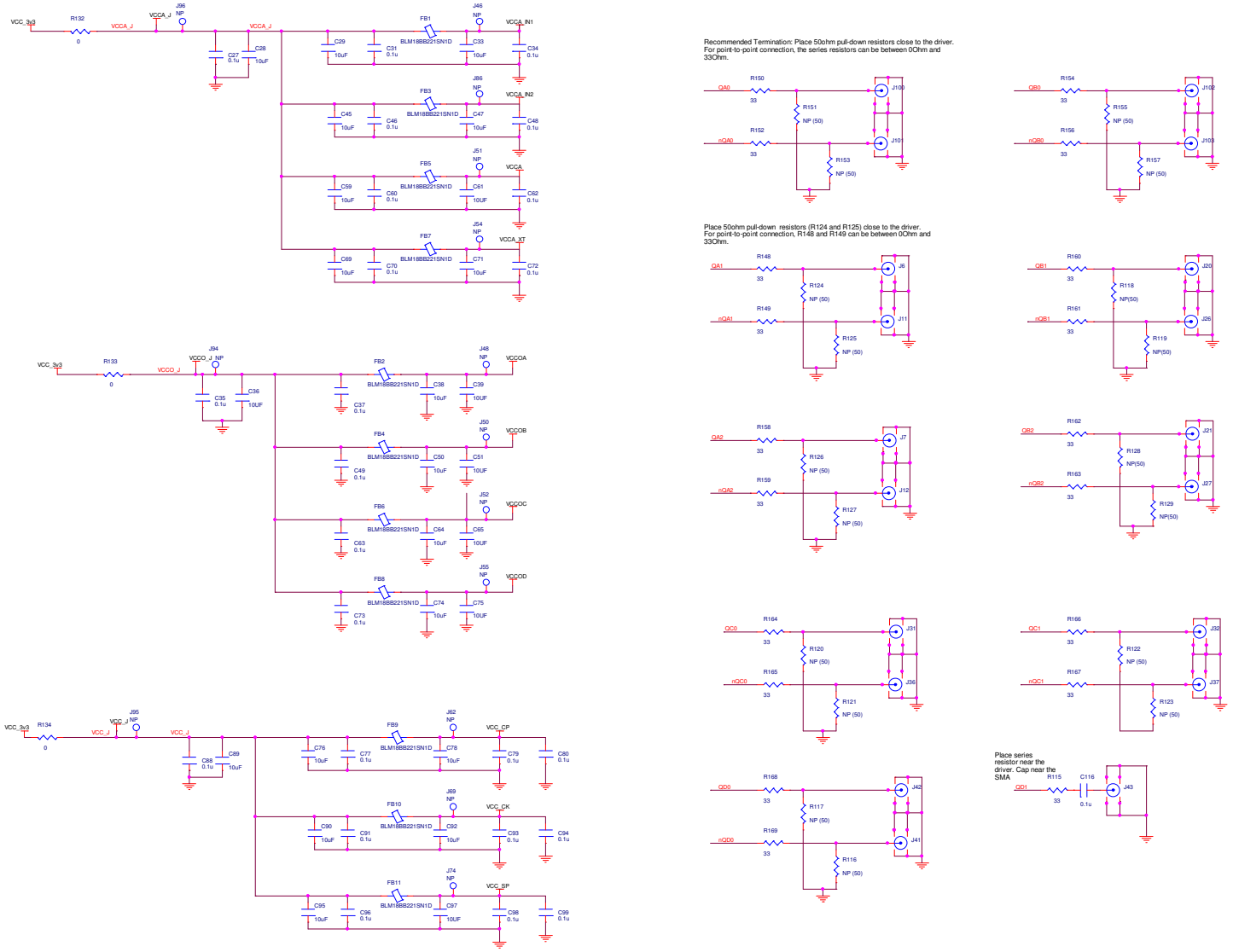


Figure 21. 8V41NS0412 Application Schematic – Page 2



To demonstrate the range of output stage configurations possible, the application schematic assumes that the 8V41NS0412 is programmed over I^2C. For alternative DC coupled LVPECL options, please see Renesas Application Note, AN-828; for AC coupling options, use Renesas Application Note, AN-844.

For a 12pF parallel resonant crystal, tuning capacitors C145 and C146 are recommended for frequency accuracy. Depending on the parasitic of the PCB layout, these values may require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C145 and C146. For this device, the crystal tuning capacitors are required for proper operation.

Crystal layout is very important to minimize capacitive coupling between the crystal pads and leads and other metal in the circuit board. Capacitive coupling to other conductors has two adverse effects: it reduces the oscillator frequency leaving less tuning margin and noise coupling from power planes, and logic transitions on signal traces can pull the phase of the crystal resonance, inducing jitter. Routing I^2C under the crystal is a common layout error, based on the assumption that it is a low frequency signal and will not affect the crystal oscillation. In fact, I^2C transition times are short enough to capacitively couple into the crystal-oscillator loop if they are routed close enough to the crystal traces.

In layout, all capacitive coupling to the crystal from any signal trace is to be minimized, that is to the OSCI and OSCO pins, traces to the crystal pads, the crystal pads, and the tuning capacitors. Using a crystal on the top layer as an example, void all signal and power layers under the crystal connections between the top layer and the ground plane used by the 8V41NS0412. Then calculate the parasitic capacity to the ground and determine if it is large enough to preclude tuning the oscillator. If the coupling is excessive, particularly if the first layer under the crystal is a ground plane, a layout option is to void the ground plane and all deeper layers until the next ground plane is reached. The ground connection of the tuning capacitors should first be made between the capacitors on the top layer, then a single ground via is dropped to connect the tuning cap ground to the ground plane as close to the 8V41NS0412 as possible as shown in the schematic.

As with any high-speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8V41NS0412 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. The ferrite bead and the 0.1uF capacitor in each power pin filter should always be placed on the device side of the board. The other components can be on the opposite side of the PCB if space on the top side is limited. Pull-up and pull-down resistors to set configuration pins can all be placed on the PCB side opposite the device side to free up the device side area if necessary.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. Depending on the application, the filter may need to be adjusted to get a lower cutoff frequency to adequately attenuate low-frequency noise. Additionally, good general design practices for power plane voltage stability suggest adding bulk capacitance in the local area of all devices.

Power Dissipation and Thermal Considerations

The 8V41NS0412 is a multi-functional, high speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as each of these features and functions is enabled.

The 8V41NS0412 device was designed and characterized to operate within the ambient industrial temperature range of -40°C to 85°C. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature.

The power calculation examples below were generated using a maximum ambient temperature and supply voltage. For many applications, the power consumption will be lower. Please contact Renesas technical support for any concerns on calculating the power dissipation for your own specific configuration.

Example of Junction Temperature Calculation

This section provides information on power dissipation and junction temperature. Equations and example calculations are also provided.

Table 31. Power Calculations Configuration #1

Output	Output Style
QA0	HCSL
QA1	HCSL
QA2	HCSL
QA3	HCSL
QB0	HCSL
QB1	HCSL
QB2	HCSL
QB3	HCSL
QC0	HCSL
QC1	HCSL
QD0	HCSL
QD1	LVCMOS

1. Power Dissipation.

The total power dissipation is the sum of the core power plus the power dissipated due to output loading.
The following is the power dissipation for V_{DD} = 3.465V and Temperature = 85°C.

- Power(core)$_{MAX}$ = V_{DD_MAX} × (I_{DD_MAX} + I_{DDA_MAX} + I_{DDO_MAX}[1]) = 3.465V × (110 + 165 + 265)mA = **1871.1mW**
- Power(HCSL outputs)$_{MAX}$ = 40.7mW/loaded output pair.
  - If all outputs are loaded, the total power is 11 × 40.7mW = **447.7mW**
- **Total Power**$_{MAX}$ = Power(core) + Power (HCSL outputs) = 1871.1mW + 447.7mW = **2318.8mW**

2. Junction Temperature.

Junction temperature, T_J, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_J, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_J is as follows: $T_J = T_A + P_D \times \theta_{JA}$:

T_J = Junction Temperature

T_A = Ambient Temperature

$_{PD}$ = Power Dissipation (W) in desired operating configuration

θ_{JA} = Junction-to-Ambient Thermal Resistance

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance must be used. Assuming no air flow and a multi-layer board, the appropriate value is 15.6°C/W per Table 32.

[1] I_{DDO_MAX} includes all output current including LVCMOS switching current.

Therefore, assuming T_A = 85°C and all outputs switching, T_J will be:

85°C + 2.3188W × 15.6°C/W = 121.2°C. This is below the limit of 125°C.

This calculation is only an example. T_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 32. Thermal Resistance Table for 64-pin VFQFN Package

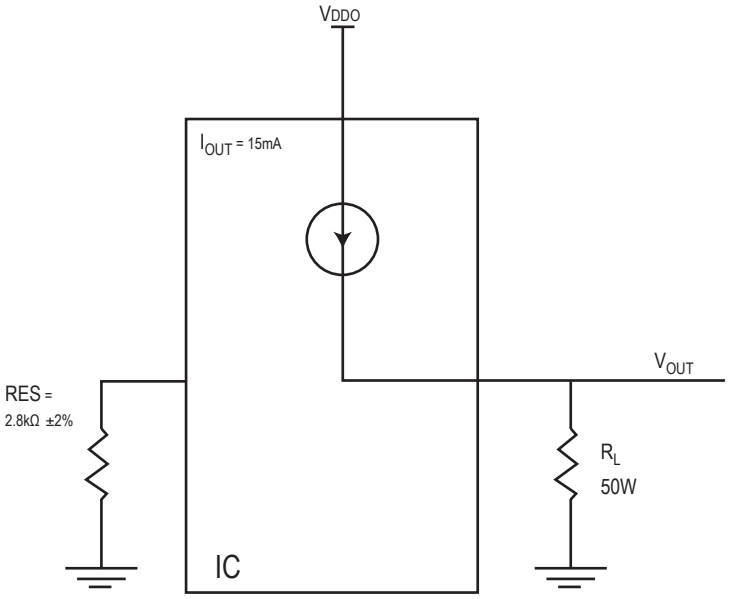
Symbol	Thermal Parameter	Condition	Value	Unit
θ_{JA}[a]	Junction-to-Ambient	No air flow	15.6	°C/W
θ_{JC}	Junction-to-Case		15.3	°C/W
θ_{JB}	Junction-to-Board		0.6	°C/W

[a] Theta J_A (θ_{JA}) values calculated using an 8-layer PCB (114.3 × 101.6mm), with 2oz. (70µm) copper plating on all 8 layers, with ePad connected to 4 ground planes.

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair. HCSL output driver circuit and termination are shown in Figure 22.

Figure 22. HCSL Driver Circuit and Termination



HCSL is a current steering output which sources a maximum of 15mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when $V_{DDO–MAX}$.

Power = $(V_{DDO\_MAX} – V_{OUT}) \times I_{OUT}$
since $V_{OUT} = I_{OUT} \times R_L$

Power = $(V_{DDO\_MAX} – I_{OUT} \times R_L) \times I_{OUT}$

= (3.465V – 15mA × 50Ω) × 15mA

Total Power Dissipation per output pair = **40.7mW**

Package Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/64-vfqfpn-package-outline-drawing-90-x-90-x-09-mm-body-05mm-pitch-epad-60-x-60-mm-nlg64p5

Marking Diagram

1. Line 1 indicates the part number prefix.
2. Line 2 indicates the part number.
3. Line 3 indicates the part number suffix.
4. “YYWW”: date code
   “#”: stepping
   “YY” is the last two digits of the year;
   “WW” is a work week number that the part was assembled;
   “$” is the mark code.

Ordering Information

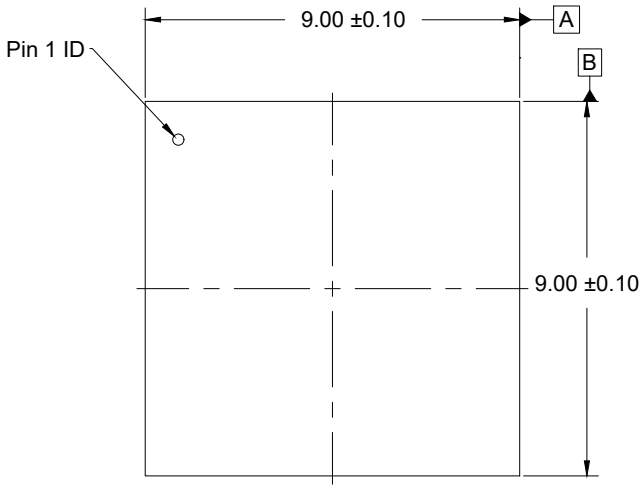
Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V41NS0412NLGI	IDT8V41NS0412NLGI	9 × 9 mm 64-VFQFN, Lead-Free	Tray	-40°C to +85°C
8V41NS0412NLGI8	IDT8V41NS0412NLGI	9 × 9 mm 64-VFQFN, Lead-Free	Tape and Reel	-40°C to +85°C

Revision History

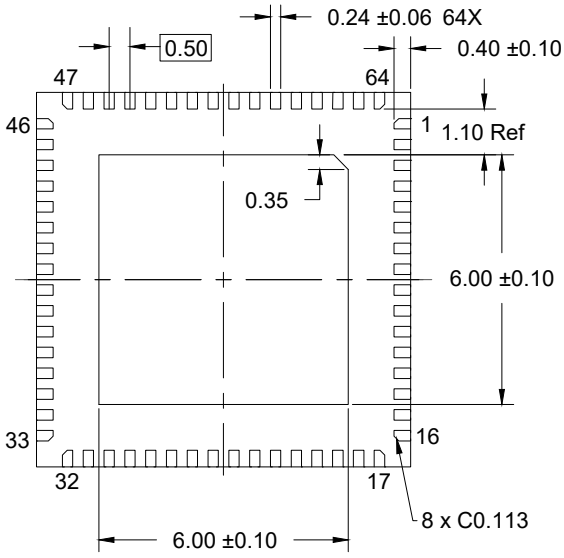
Revision Date	Description of Change
August 27, 2020	Removed all references to the function, “No active receivers should be connected to QA outputs” in Table 7 to Table 10, and in Table 13 to Table 16
April 25, 2018	Initial release.

Package Outline Drawing

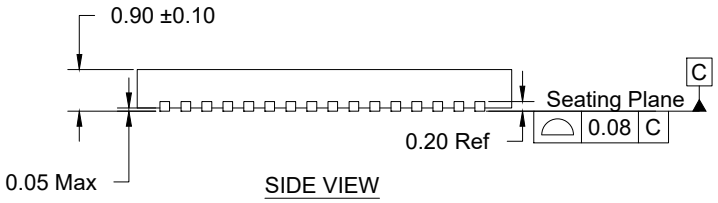
Package Code: NLG64P5
64-VFQFPN 9.0 x 9.0 x 0.9 mm Body, 0.50mm Pitch
PSC-4147-05, Revision: 06, Date Created: Aug 07, 2023



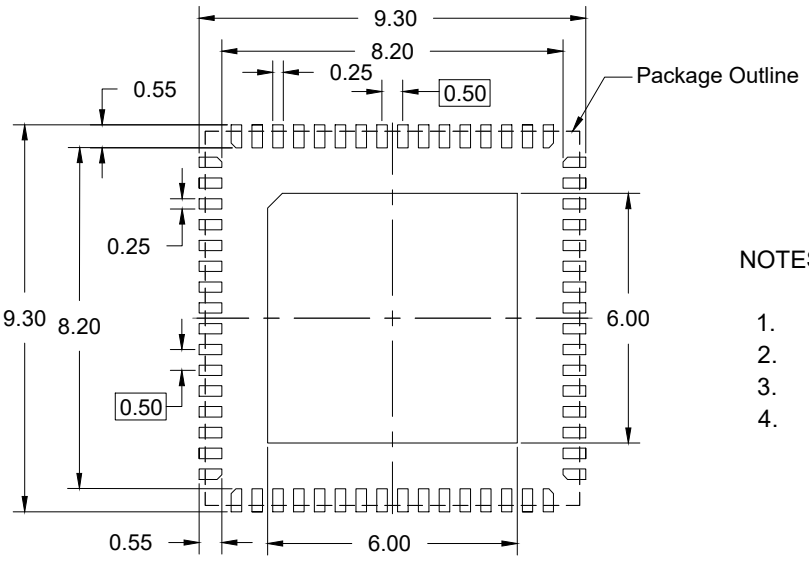
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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