## Description

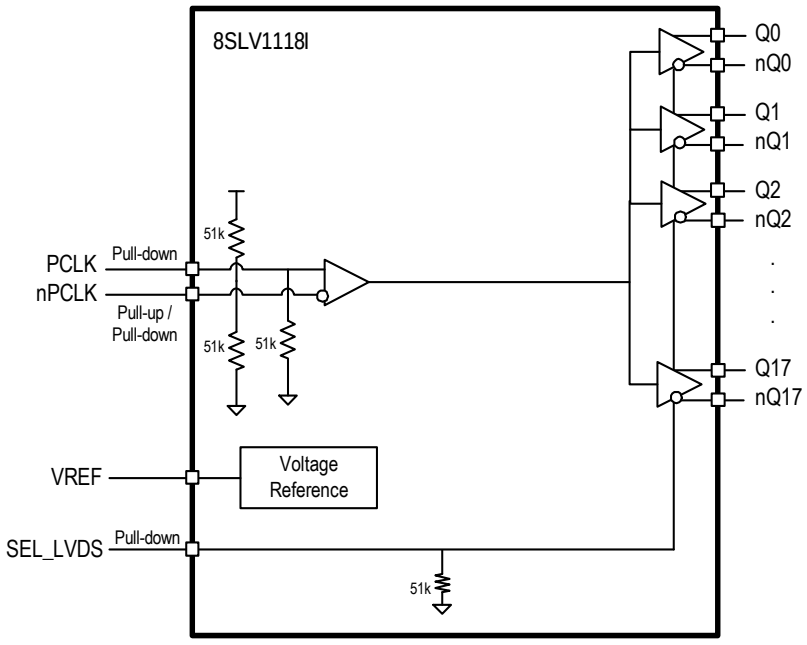
The 8SLVS1118 is a high-performance, low-power, differential 1:18 output fanout buffer. This highly versatile device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. Guaranteed output-to-output and part-to-part skew characteristics make the 8SLVS1118 ideal for clock distribution applications that demand well-defined performance and repeatability.

The device is characterized to operate from a 2.5V or 3.3V power supply. The integrated bias voltage references enable easy interfacing AC-coupled signals to the device inputs.

## Features

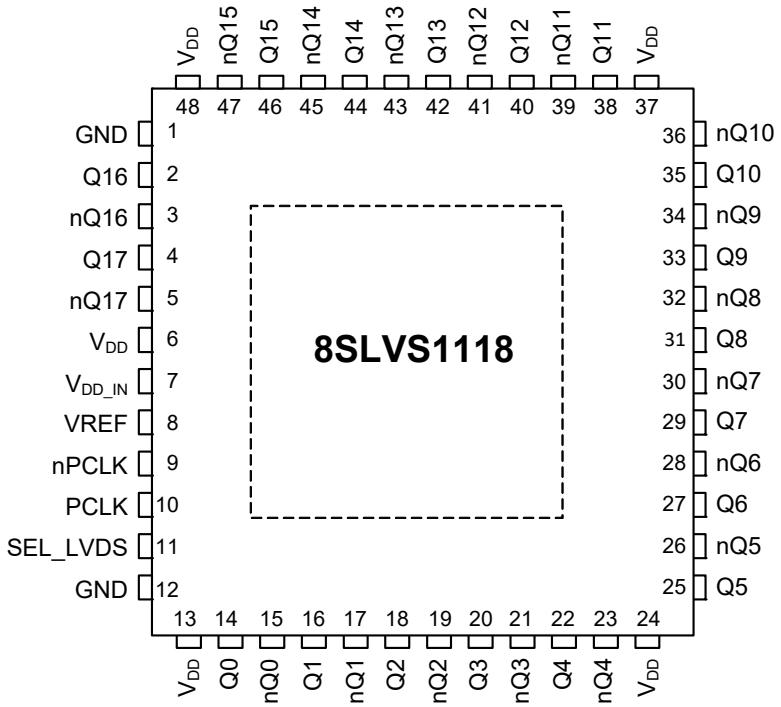
- 1:18, low skew, low additive jitter LVPECL/LVDS fanout buffer
- Low power consumption
- Differential PCLK, nPCLK clock pair accepts the following differential/single-ended input levels: LVDS, LVPECL, and LVCMOS
- Maximum input clock frequency: 2GHz
- Propagation delay: 290ps (typical)
- Output skew: 40ps (typical)
- Low additive phase jitter, RMS: 39fs (typical), Integration Range: 12kHz – 20MHz, ($f_{REF}$ = 156.25MHz, $V_{PP}$ = 1V, $V_{DD}$ = 3.3V)
- Full 2.5V and 3.3V supply voltage modes
- Device current consumption: 180mA (typical) IEE for LVPECL output mode, 400mA (typical) IDD for LVDS output mode
- 48-VFQFPN, lead-free (RoHS 6) packaging
- Transistor count: 1762
- -40°C to +85°C ambient operating temperature
- Supports case temperature up to 105°C

## Block Diagram



## Pin Assignment

Figure 1. Pin Assignment for 7mm × 7mm VFQFPN Package – Top View




## Pin Descriptions

Table 1. Pin Descriptions[a]

| Number | Name | Type | Description |
|---|---|---|---|
| 1 | GND | Power | Ground supply pin. |
| 2 | Q16 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 3 | nQ16 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 4 | Q17 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 5 | nQ17 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 6 | $V_{DD}$ | Power | Output power supply pin. |
| 7 | $V_{DD\_IN}$ | Power | Power supply pin. |
| 8 | VREF | Output | Bias voltage reference for the PCLK, nPCLK input pair. |
| 9 | nPCLK | Input [PD/PU] | Inverting differential clock/data input. |
| 10 | PCLK | Input [PD] | Non-inverting differential clock/data input. |
| 11 | SEL_LVDS | Input [PD] | Control input. Output amplitude select for differential outputs. |
| 12 | GND | Power | Power supply ground. |
| 13 | $V_{DD}$ | Power | Output power supply pin. |
| 14 | Q0 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 15 | nQ0 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 16 | Q1 | Output | Differential output pair. LVPECL/ LVDS interface levels. |

Table 1. Pin Descriptions[a] (Cont.)

| Number | Name | Type | Description |
|---|---|---|---|
| 17 | nQ1 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 18 | Q2 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 19 | nQ2 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 20 | Q3 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 21 | nQ3 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 22 | Q4 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 23 | nQ4 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 24 | $V_{DD}$ | Power | Output power supply pin. |
| 25 | Q5 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 26 | nQ5 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 27 | Q6 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 28 | nQ6 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 29 | Q7 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 30 | nQ7 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 31 | Q8 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 32 | nQ8 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 33 | Q9 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 34 | nQ9 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 35 | Q10 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 36 | nQ10 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 37 | $V_{DD}$ | Power | Output power supply pin. |
| 38 | Q11 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 39 | nQ11 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 40 | Q12 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 41 | nQ12 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 42 | Q13 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 43 | nQ13 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 44 | Q14 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 45 | nQ14 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 46 | Q15 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 47 | nQ15 | Output | Differential output pair. LVPECL/ LVDS interface levels. |
| 48 | $V_{DD}$ | Power | Output power supply pin. |
| ePad | GND_EPAD | Power | Exposed pad of package. Connect to ground. |

[a] Pull-up (PU) and pull-down (PD) resistors are indicated in parentheses. *Pull-up* and *pull-down* refers to internal input resistors. For typical values, see DC Input Characteristics.

## Function Table

Table 2. SEL_LVDS Output Amplitude Selection Table

| SEL_LVDS | Qx Output Amplitude (mV) |
|---|---|
| 0 (default) | 750 (LVPECL) |
| 1 | 450 (LVDS) |

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8SLVS1118 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD\_IN}$ | 3.6V |
| Inputs, $V_I$ | -0.5V to 3.6V |
| Outputs, $I_O$ (LVDS)<br>Continuous Current<br>Surge current | <br>10mA<br>15mA |
| Outputs, $I_O$ (LVPECL)<br>Continuous Current<br>Surge current | <br>50mA<br>100mA |
| Input Sink/source, $I_{REF}$ | ±2mA |
| Maximum Junction Temperature, $T_{J,MAX}$ | 125°C |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |
| ESD – Human Body Model[a] | 2000V |
| ESD – Charged Device Model[a] | 1500V |

[a] According to JEDEC JS-001-2012/JESD22-C101E.

# DC Electrical Characteristics

Table 4. DC Input Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 2 | | pF |
| $R_{PULLDOWN}$ | Input Pull-down Resistor | | | 51 | | kΩ |
| $R_{PULLUP}$ | Input Pull-up Resistor | | | 51 | | kΩ |

Table 5. Power Supply DC Characteristics, $V_{DD\_IN} = V_{DD} = 3.3V \pm 5\%$, $T_A = -40°C$ to $+85°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD\_IN}$ | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DD}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD\_IN}$ | Power Supply Current | | | | 15 | mA |
| $I_{EE}$ | Power Supply Current | SEL_LVDS = 0 | | | 220 | mA |
| $I_{DD}$ | Output Supply Current | SEL_LVDS = 1 | | | 480 | mA |

Table 6. Power Supply DC Characteristics, $V_{DD\_IN} = V_{DD} = 2.5V \pm 5\%$, $T_A = -40°C$ to $+85°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD\_IN}$ | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{DD}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD\_IN}$ | Power Supply Current | | | | 13 | mA |
| $I_{EE}$ | Power Supply Current | SEL_LVDS = 0 | | | 215 | mA |
| $I_{DD}$ | Output Supply Current | SEL_LVDS = 1 | | | 475 | mA |

Table 7. LVCMOS Inputs DC Characteristics, $V_{DD\_IN} = V_{DD} = 2.5V \pm 5\%$, $3.3V \pm 5\%$, $T_A = -40°C$ to $+85°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | $V_{DD\_IN} = 3.3V \pm 5\%$ | 2 | | $V_{DD\_IN} + 0.3$ | V |
| | | | $V_{DD\_IN} = 2.5V \pm 5\%$ | 1.7 | | $V_{DD\_IN} + 0.3$ | V |
| $V_{IL}$ | Input Low Voltage | | $V_{DD\_IN} = 3.3V \pm 5\%$ | -0.3 | | 0.8 | V |
| | | | $V_{DD\_IN} = 2.5V \pm 5\%$ | -0.3 | | 0.7 | V |
| $I_{IH}$ | Input High Current | SEL_LVDS | $V_{DD\_IN} = V_{IN} = V_{DD\_MAX}$ | | | 150 | µA |
| $I_{IL}$ | Input Low Current | SEL_LVDS | $V_{DD\_IN} = V_{DD\_MAX}$, $V_{IN} = 0V$ | -10 | | | µA |

Table 8. LVDS DC Characteristics – $V_{DD}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 370 | | 490 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | | 1.9 | | 2.7 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | | 50 | mV |

Table 9. LVDS DC Characteristics – $V_{DD}$ = 2.5V ± 5%, $T_A$ = -40°C to +85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 360 | | 480 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | | 1.1 | | 1.9 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | | 50 | mV |

Table 10. LVPECL DC Characteristics, $V_{DD\_IN}$ = $V_{DD}$ = 2.5V ±5%, 3.3V ±5%, $T_A$ = -40°C to +85°C[a]

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | PCLK, nPCLK | $V_{IN} = V_{DD\_IN} = V_{DD\_MAX}$ | | | 150 | µA |
| $I_{IL}$ | Input Low Current | PCLK | $V_{IN}$ = 0V, $V_{DD\_IN} = V_{DD\_MAX}$ | -10 | | | µA |
| | | nPCLK | $V_{IN}$ = 0V, $V_{DD\_IN} = V_{DD\_MAX}$ | -150 | | | µA |
| VREF | Reference Voltage | | $I_{REF}$ = 100µA, $V_{DD\_IN}$ = 3.3V | 2.05 | | 2.45 | V |
| | | | $I_{REF}$ = 100µA, $V_{DD\_IN}$ = 2.5V | 1.55 | | 1.85 | |
| $V_{OH}$ | Output High Voltage[b] | | | $V_{DD}$ – 1.1 | | $V_{DD}$ – 0.7 | V |
| $V_{OL}$ | Output Low Voltage[b] | | | $V_{DD}$ – 1.8 | | $V_{DD}$ – 1.4 | V |

[a] Core supply voltage cannot be lower than the output supply voltage.

[b] Outputs terminated with 50Ω to $V_{DD}$ – 2V.

# AC Electrical Characteristics

Table 11. AC Electrical Characteristics, $V_{DD\_IN}$ = $V_{DD}$ = 2.5V ±5%, 3.3V ±5%, $T_A$ = -40°C to +85°C[a]

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{REF}$ | Input Frequency | | | | | 2 | GHz |
| $\Delta V/\Delta t$ | Input Edge Rate | | | 1.5 | | | V/ns |
| $t_{PD}$ | Propagation Delay[b], [c] | PCLK to any Qx | | | 290 | 400 | ps |
| *t*sk(o) | Output Skew[d], [e] | | | | 40 | 60 | ps |
| *t*sk(p) | Pulse Skew[f] | | $f_{REF}$ = 100MHz | | 4 | 20 | ps |
| *t*sk(pp) | Part-to-part Skew[e], [g] | | | | | 200 | ps |
| $t_{JIT}$ | Buffer Additive Phase Jitter, RMS; $V_{DDIN}$ = $V_{DD}$ = 3.3V 750mV amplitude; see Additive Phase Jitter | | $f_{REF}$ = 156.25MHz; square wave, $V_{PP}$ = 1V; Integration range: 1kHz – 40MHz | | 57 | 60 | fs |
| | | | $f_{REF}$ = 156.25MHz square wave, $V_{PP}$ = 1V; Integration range: 12kHz – 20MHz | | 39 | 43 | fs |
| $\Phi_N$(≥30M) | Clock Single-side Band Phase Noise | | ≥30MHz offset from carrier and noise floor | | ≤-160 | | dBc/Hz |
| $t_R$ / $t_F$ | Output Rise/ Fall Time | | 10–90% | | 160 | 300 | ps |
| | | | 20–80% | | 105 | 200 | ps |
| $V_{PP}$ | Input Voltage Amplitude[h], [i] | PCLK, nPCLK | | 0.15 | | 1.2 | V |
| $V_{PP\_DIFF}$ | Differential Input Voltage Amplitude | PCLK, nPCLK | | 0.3 | | 2.4 | V |
| $V_{CMR}$ | Common Mode Input Voltage[h], [i], [j] | | | 1.125 | | $V_{DD}$ – ($V_{PP/2}$) | V |
| $VO_{(pp)}$ | Output Voltage Swing, Peak-to-peak | | SEL_LVDS = 0 | 0.55 | 0.73 | 0.95 | V |
| | | | SEL_LVDS = 1 | 0.30 | 0.43 | 0.60 | V |
| $V_{DIFF\_OUT}$ | Differential Output Voltage Swing, Peak-to-peak | | SEL_LVDS = 0 | 1.10 | 1.46 | 1.90 | V |
| | | | SEL_LVDS = 1 | 0.60 | 0.86 | 1.20 | V |
| $V_{OD}$ | Differential Output Voltage | LVPECL Outputs | SEL_LVDS = 0, outputs loaded with 50Ω to $V_{DD}$ – 2V | 550 | 730 | 950 | mV |
| | | LVDS Outputs | SEL_LVDS = 1, outputs loaded with 100Ω | 300 | 430 | 600 | mV |

Table 11. AC Electrical Characteristics, $V_{DD\_IN} = V_{DD} = 2.5V \pm 5\%, 3.3V \pm 5\%$, $T_A = -40°C$ to $+85°C$[a]

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Offset Voltage | LVDS Outputs | SEL_LVDS = 1, $V_{DDIN} = V_{DD} = 3.3V$ | 2.05 | 2.25 | 2.45 | V |
| | | | SEL_LVDS = 1, $V_{DDIN} = V_{DD} = 2.5V$ | 1.25 | 1.45 | 1.65 | V |

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Measured from the differential input crossing point to the differential output crossing point.

[c] Input $V_{PP} = 400mV$.

[d] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

[e] This parameter is defined in accordance with JEDEC Standard 65.

[f] Output pulse skew is the absolute value of the difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

[g] Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

[h] $V_{IL}$ should not be less than -0.3V. VIH should not be higher than $V_{DD\_IN}$.

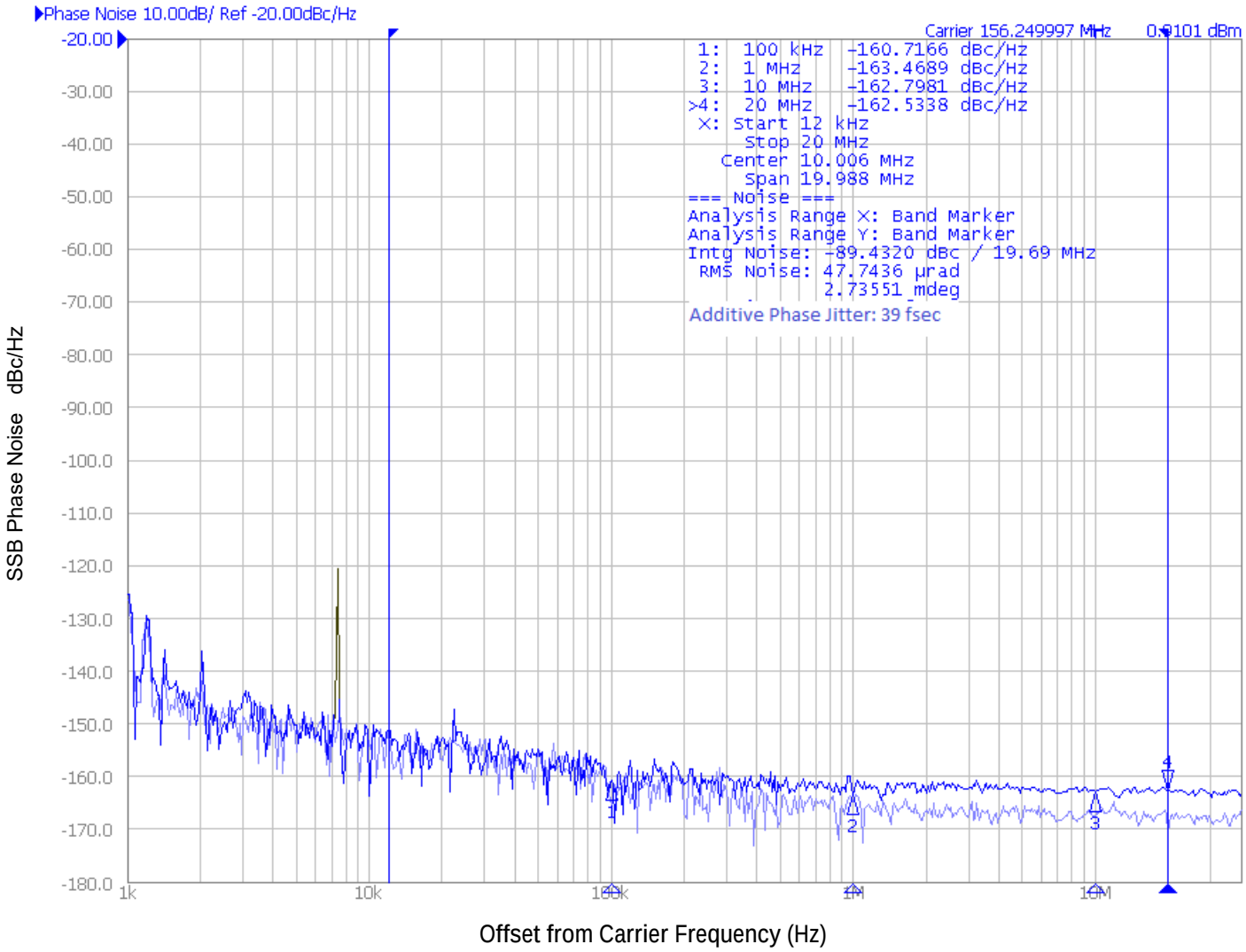
[i] For single-ended LVCMOS input applications, refer to application section, Wiring the Differential Input to Accept Single-Ended Levels.

[j] Common Mode Input Voltage is defined as the cross-point voltage.

## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

Figure 2. Additive Phase Jitter. Frequency: 156.25MHz, Integration Range: 12kHz to 20MHz = 39fs Typical




As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Measured using a Wenzel 156.25MHz Oscillator as the input source.

# Applications Information

## Recommendations for Unused Input and Output Pins

### Inputs

#### *PCLK/nPCLK Inputs*

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

### Outputs

#### *LVDS Outputs*

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

#### *LVPECL Outputs*

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

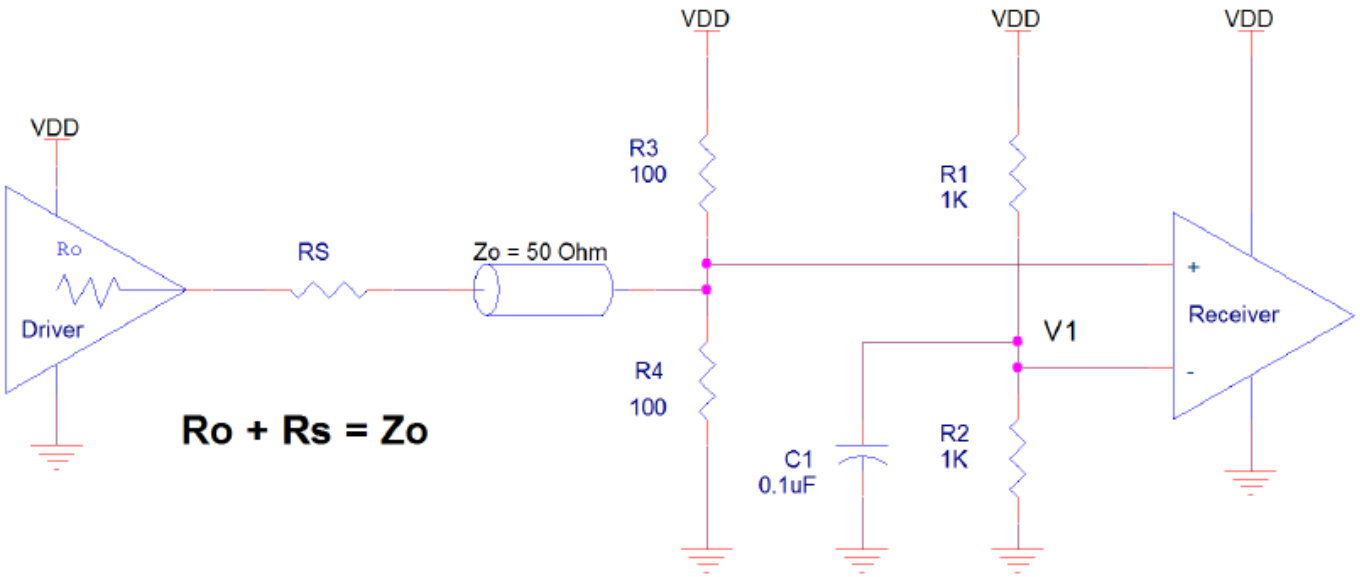
#### *VREF*

The unused VREF pin can be left floating. We recommend that there is no trace attached.

## Wiring the Differential Input to Accept Single-Ended Levels

Figure 3 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the $V_1$ in the center of the input voltage swing. For example, if the input clock swing is 1.8V and $V_{DD} = 1.8V$, R1 and R2 value should be adjusted to set $V_1$ at 0.9V. The values below are for when both the single ended swing and $V_{DD}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 3. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{DD}$ +0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ($Z_T$) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance ($Z_0$) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source.

The standard termination schematic as shown in Figure 4 can be used with either type of output structure. Figure 5, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 4. Standard LVDS Termination

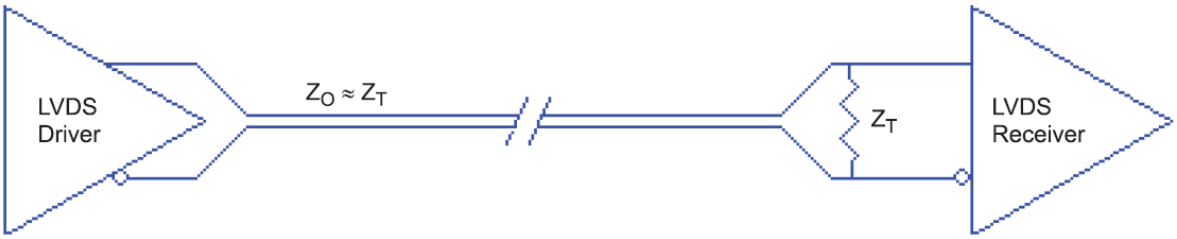
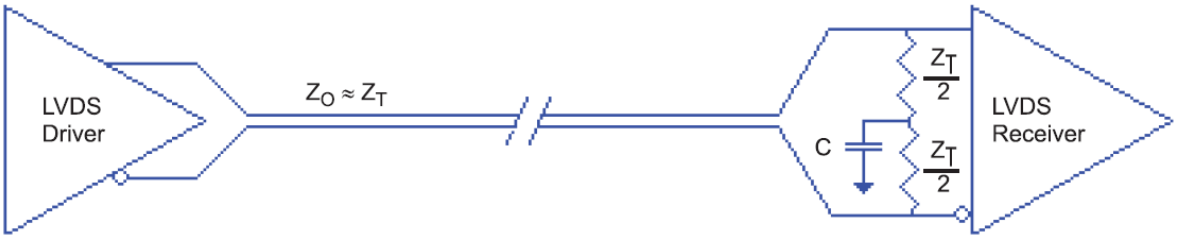



Figure 5. Optional LVDS Termination



## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figure 6 and Figure 7 show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

Figure 6. 3.3V LVPECL Output Termination

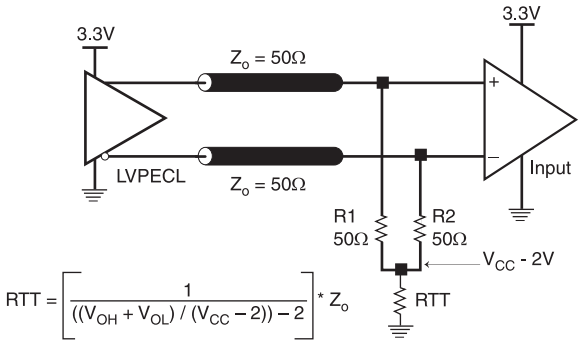
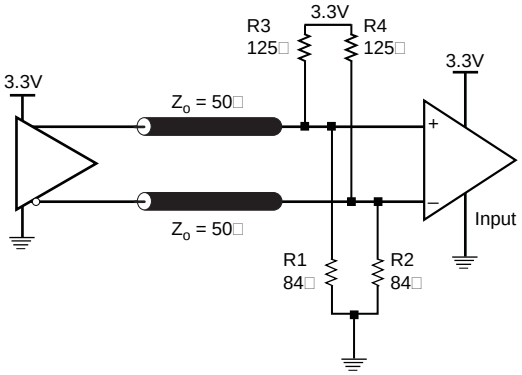



Figure 7. 3.3V LVPECL Output Termination



## Termination for 2.5V LVPECL Outputs

Figure 8 and Figure 9 show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{DD}$ – 2V. For $V_{DD}$ = 2.5V, the $V_{DD}$ – 2V is very close to ground level. The R3 in Figure 9 can be eliminated and the termination is shown in Figure 10.

Figure 8. 2.5V LVPECL Driver Termination Example

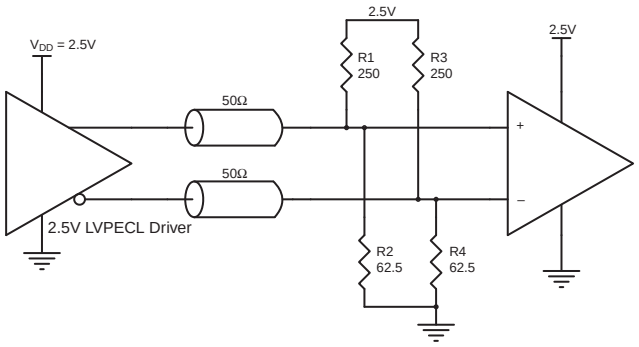



Figure 9. 2.5V LVPECL Driver Termination Example

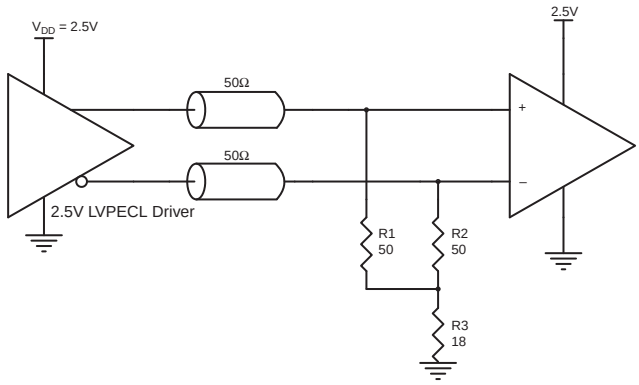
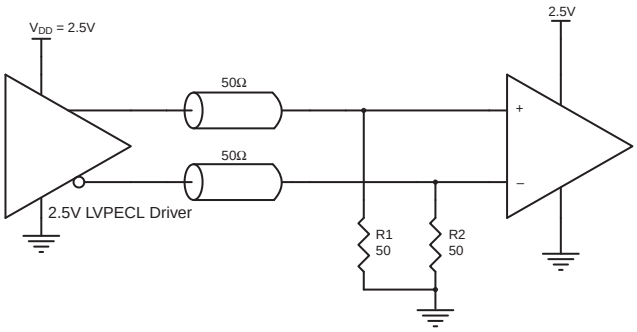



Figure 10. 2.5V LVPECL Driver Termination Example



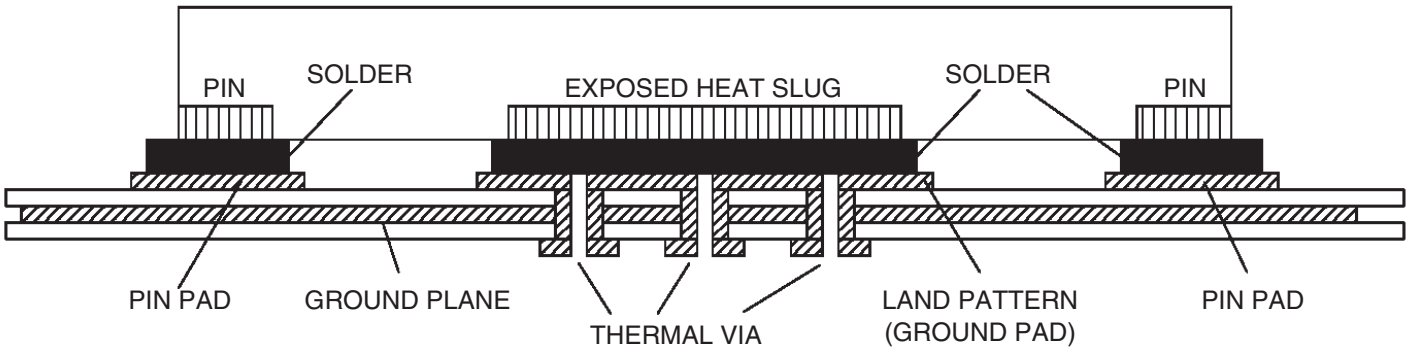
## VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 11. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12mils to 13mils (0.30mm to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern.

Note: These recommendations are to be used as a guideline only. For further information, please refer to the application note on the *Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead-frame Base Package, Amkor Technology.*

Figure 11. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to scale)



## Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter $\Psi_{JB}$ (Psi-JB) to calculate the junction temperature ($T_J$) and ensure it does not exceed the maximum allowed junction temperature in the Absolute Maximum Ratings table.

The junction-to-board thermal characterization parameter, $\Psi_{JB,}$ is calculated using the following equation:

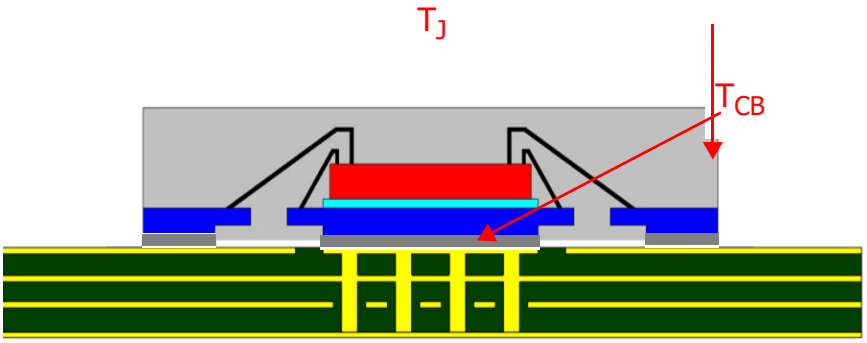
$T_J = T_{CB} + \Psi_{JB} \times P_{D,}$ where

$T_J$ = Junction temperature at steady state condition in ($^oC$).

$T_{CB}$ = Case temperature (Bottom) at steady state condition in ($^oC$).

$\Psi_{JB}$ =Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.

$P_D$ = power dissipation (W) in desired operating configuration.




The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature ($T_{CB}$). A good connection ensures that temperature at the exposed pad ($T_{CB}$) and the board temperature ($T_B$) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example Calculation for Junction Temperature ($T_J$): $T_J = T_{CB} + \Psi_{JB} \times P_D$

| | |
|---|---|
| Package type | 48-VFQFPN |
| Body size (mm) | 7 × 7 × 0.8 |
| ePad size (mm) | 5.65 × 5.65 |
| Thermal Via | 5 × 5 Matrix |
| $\Psi_{JB}$ | 1.2$^o$C/W |
| $T_{CB}$ | 105$^o$C |
| $P_D$ | 1.715W |

For the above variables, the junction temperature is equal to 107.1$^o$C. Since this is below the maximum junction temperature of 125$^o$C, there are no long-term reliability concerns.

## Power Considerations (LVDS Output Mode)

This section provides information on power dissipation and junction temperature for the 8SLVS1118.
Equations and example calculations are also provided.

1. Power Dissipation.

The following is the power dissipation for $V_{DD\_IN}$ = $V_{DD}$ = 3.465V, which gives worst case results.

Maximum current at 85°C: $I_{DD\_IN\_MAX}$ + $I_{DD\_MAX}$ = 495mA.

$Power_{\_MAX}$ = 3.465V x 495mA = 1715mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 22.4°C/W per Table 12.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.715W * 22.4°C/W = 123.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 12. Thermal Resistance $\theta_{JA}$ for 48-VFQFPN, Forced Convection

| $\theta_{JA}$ (°C/W) vs. Air Flow (m/s) | | | |
|---|---|---|---|
| Meters per Second | 0 | 1 | 2 |
| 48-Lead VFQFN Multi-Layer PCB, JEDEC Standard Test Boards | 22.4 | 18.9 | 17.4 |

## Power Considerations (LVPECL Output Mode)

This section provides information on power dissipation and junction temperature for the 8SLVS1118.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8SLVS1118 is the sum of the core power plus the power dissipated at the output(s).
The following is the power dissipation for $V_{DD\_IN}$ = 3.465V, which gives worst case results.

Note: Please refer to Section 3 for details on calculating power dissipated at the outputs.

Power $(core)_{MAX} = V_{DD\_IN} * I_{EE\_MAX}$ = 3.465V * 220mA = 762.3mW

Power $(outputs)_{MAX}$ = 35mW/Loaded Output pair
If all outputs are loaded, the total power is 18 * 35mW = 630mW

Total $Power\_{MAX}$ (3.465V, with all outputs switching) = 762.3mW + 630mW = 1392.3mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 22.4°C/W per Table 13.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.3923W * 22.4°C/W = 116.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

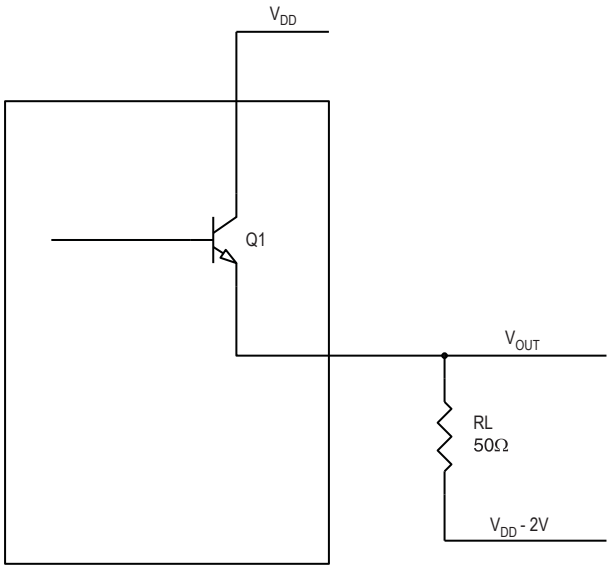
Table 13. Thermal Resistance $\theta_{JA}$ for 48-VFQFPN, Forced Convection

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 22.4°C/W | 18.9°C/W | 17.4°C/W |

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair. LVPECL output driver circuit and termination are shown in Table 10.

Figure 12. LVPECL Driver Circuit and Termination




To calculate worst case power dissipation at the output(s), use the following equations which assume a 50Ω load, and a termination voltage of $V_{DD}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{DD\_MAX} – 0.7V$
  $(V_{DD\_MAX} – V_{OH\_MAX}) = 0.7V$
- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{DD\_MAX} – 1.4V$
  $(V_{DD\_MAX} – V_{OL\_MAX}) = 1.4V$

Pd_H is the power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{DD\_MAX} – 2V))/R_L] * (V_{DD\_MAX} – V_{OH\_MAX}) = [(2V – (V_{DD\_MAX} – V_{OH\_MAX}))/R_L] * (V_{DD\_MAX} – V_{OH\_MAX}) = [(2V – 0.7V)/50Ω] * 0.7V = 18.2mW$

$Pd\_L = [(V_{OL\_MAX} – (V_{DD\_MAX} – 2V))/R_L] * (V_{DD\_MAX} – V_{OL\_MAX}) = [(2V – (V_{DD\_MAX} – V_{OL\_MAX}))/R_L] * (V_{DD\_MAX} – V_{OL\_MAX}) = [(2V – 1.4V)/50Ω] * 1.4V = 16.8mW$

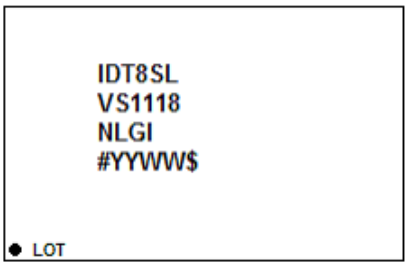
Total Power Dissipation per output pair = Pd_H + Pd_L = 35mW

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/48-vfqfpn-package-outline-drawing-70-x-70-x-085-mm-body-05mm-pitchepad-565-x-565-mm-nlg48p1

## Marking Diagram



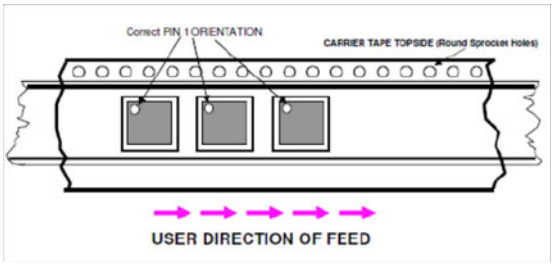
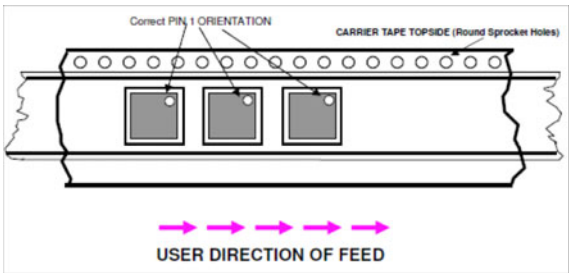

1. Line 1, line 2, and line 3 indicates the part number.
2. Line 4:
   - "#" indicates stepping.
   - "YYWW" indicates the date code
     (YY denotes the last two digits of the year, and
     "WW" denotes a work week number that the part was assembled.
   - "$" indicates the mark code.

## Ordering Information

Table 14. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 8SLVS1118NLGI | IDT8SLVS1118NLGI | 48-VFQFPN, Lead-Free | Tray | -40°C to +85°C |
| 8SLVS1118NLGI8 | IDT8SLVS1118NLGI | 48-VFQFPN, Lead-Free; Quadrant 1 (EIA-481-C) | Tape & Reel, Pin 1 Orientation: EIA-481-C | |
| 8SLVS1118NLGI/W | IDT8SLVS1118NLGI | 48-VFQFPN, Lead-Free; Quadrant 2 (EIA-481-D/E) | Tape & Reel, Pin 1 Orientation: EIA-481-D/E | |

Table 15. Pin 1 Orientation in Tape and Reel Packaging

| Part Number Suffix | Pin 1 Orientation | Illustration |
|---|---|---|
| 8SLVS1118NLGI8 | Quadrant 1 (EIA-481-C) |  |
| 8SLVS1118NLGI/W | Quadrant 2 (EIA-481-D/E) |  |

# Revision History

| Revision Date | Description of Change |
|---|---|
| January 15, 2019 | ▪ Removed “2.5V LVPECL Input with Built-in 50Ω Termination Interface”<br>▪ Removed “3.3V LVPECL Input with Built-in 50Ω Termination Interface”<br>▪ Updated the package outline drawings; however, no mechanical changes |
| July 17, 2017 | Initial release. |

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com


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