

## Description

The 8S89296 is a high performance LVDS programmable delay line. The delay can vary from 2.2ns to 12.5ns in 10ps steps. The 8S89296 is characterized to operate from a 2.5V power supply and is guaranteed over industrial temperature range.

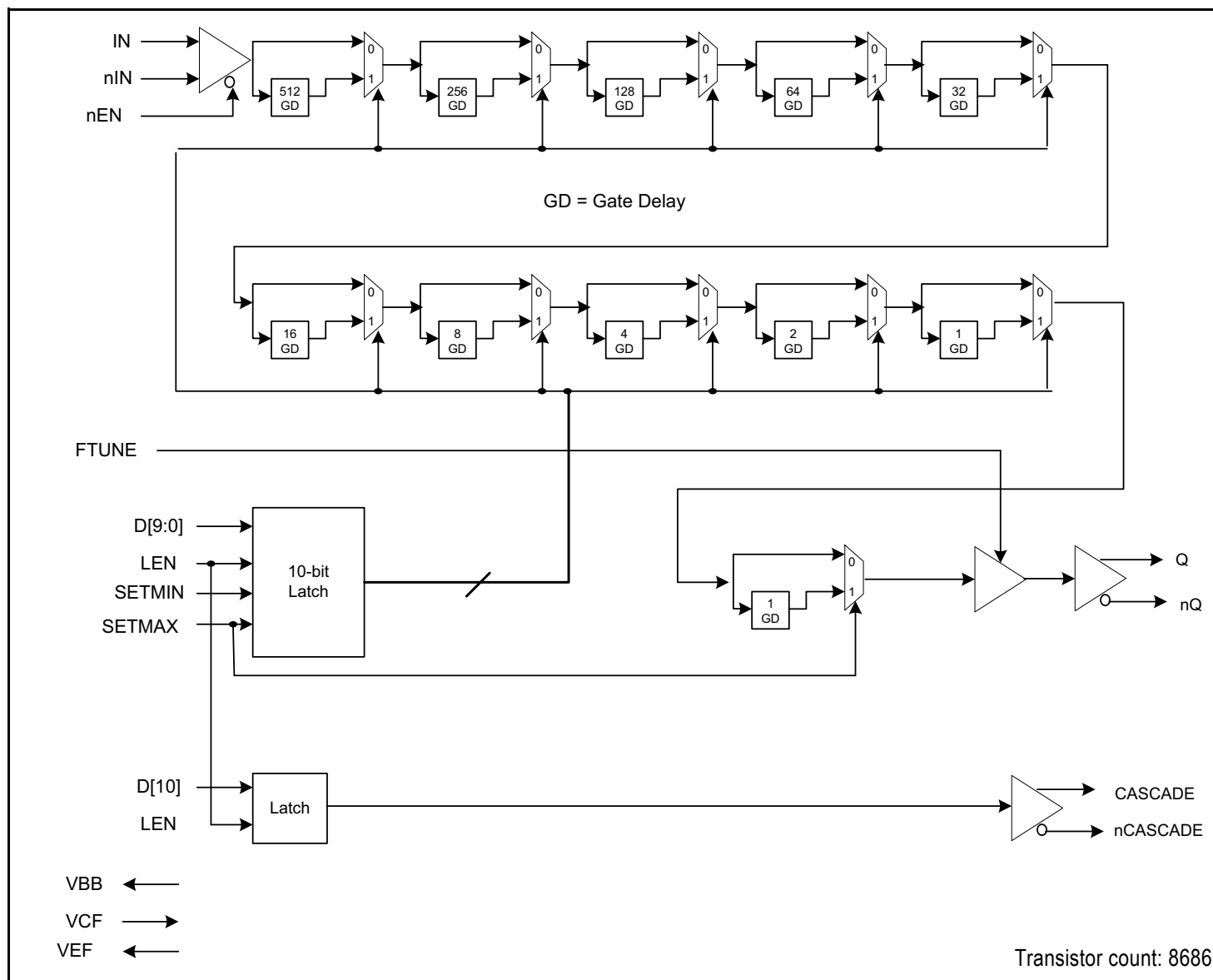
The delay of the device varies in discrete steps based on a control word. A 10-bit long control word sets the delay in 10ps increments. Also, the input pins IN and nIN default to an equivalent low state when left floating. The control register can accept CMOS or TTL level signals.

## Features

- One LVDS level output
- One differential clock input pair
- Differential input clock (IN, nIN) can accept the following signaling levels: LVPECL, LVDS, CML
- Maximum frequency: 800MHz
- Programmable Delay Range: 2.2ns to 12.5ns in 10ps steps
- D[10:0] can accept LVPECL, LVCMOS or LVTTTL levels
- Full 2.5V supply voltages
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

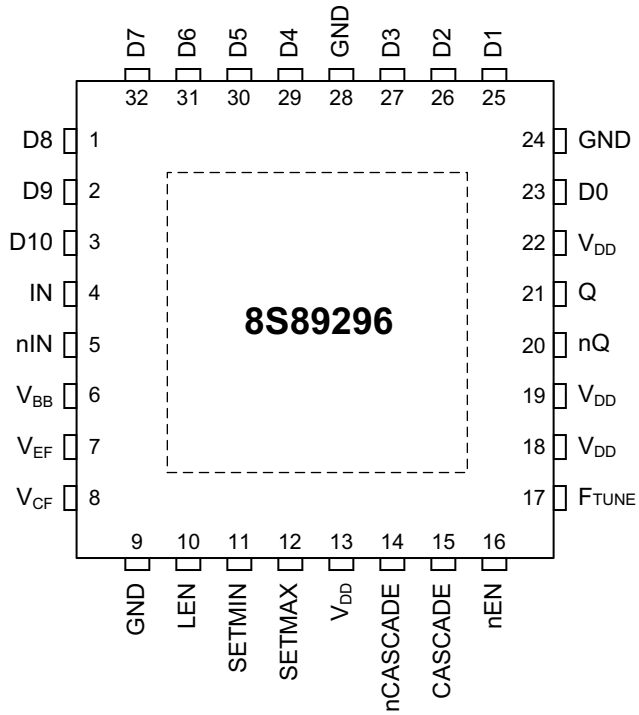
## Block Diagram

Figure 1: Block Diagram



## Pin Assignments

Figure 2: Pin Assignments for 5mm x 5mm 32-Lead Package



## Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

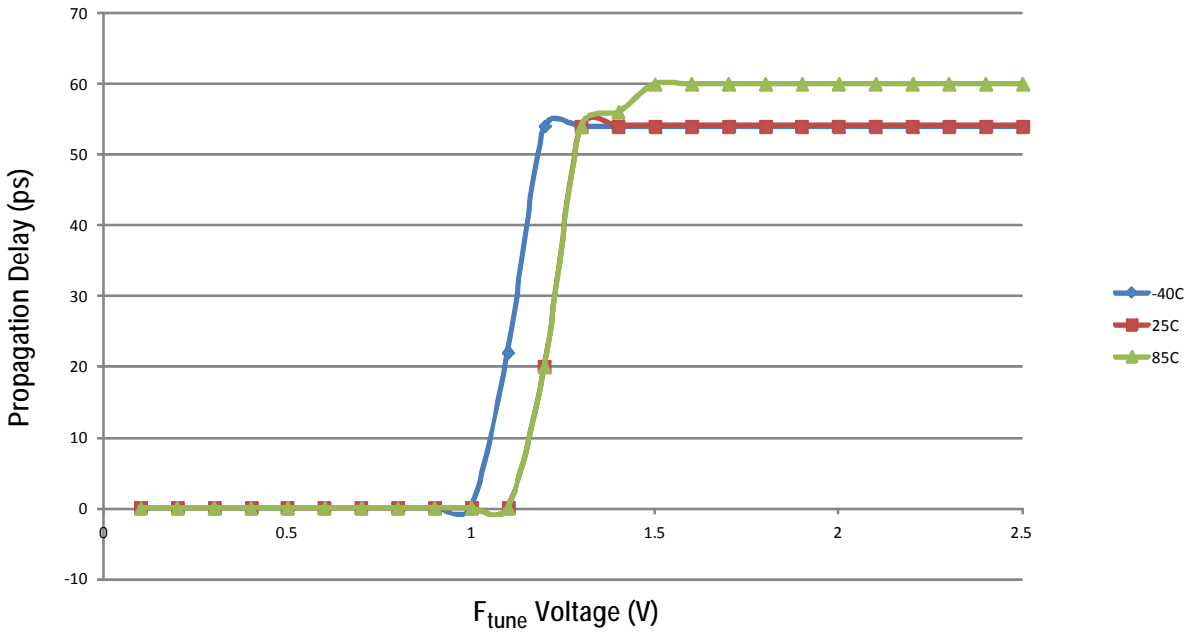
| Number | Name            | Type <sup>[a]</sup> | Description   |
|--------|-----------------|---------------------|---|
| 1      | D8              | Input (PD)          | Parallel data input D8.<br>Single-ended LVCMOS, LVTTTL, LVPECL interface levels.  |
| 2      | D9              | Input (PD)          | Parallel data input D9.<br>Single-ended LVCMOS, LVTTTL, LVPECL interface levels.  |
| 3      | D10             | Input (PD)          | Parallel data input D10.<br>Single-ended LVCMOS, LVTTTL, LVPECL interface levels.   |
| 4      | IN              | Input (PD)          | Non-inverting differential input.   |
| 5      | nIN             | Input (PU/ PD)      | Inverting differential input.   |
| 6      | V <sub>BB</sub> | Output              | Reference voltage output. This pin can be used to re-bias AC-coupled inputs to IN and nIN. When used, de-couple to V <sub>DD</sub> using a 0.01μF capacitor. If not used, leave floating.     |
| 7      | V <sub>EF</sub> | Output              | Reference voltage output. See <a href="#">Table 4</a> .   |
| 8      | V <sub>CF</sub> | Input               | Reference voltage input. The voltage driven on V <sub>CF</sub> sets the logic transition threshold for D[10:0].   |
| 9      | GND             | Power               | Power supply ground.  |
| 10     | LEN             | Input (PD)          | D inputs LOAD and HOLD control input. When HIGH, latches the D[10:0] bits. When LOW, the D[10:0] latches are transparent. Single-ended LVPECL interface levels. See <a href="#">Table 3</a> . |

Table 1: Pin Descriptions

| Number | Name              | Type <sup>[a]</sup> | Description   |
|--------|-------------------|---------------------|---|
| 11     | SETMIN            | Input (PD)          | Minimum delay set logic input. When HIGH, D[10:0] registers are reset. When LOW, the delay is set by SETMAX or D[10:0]. Default is LOW when left floating. Single-ended LVPECL interface levels. See <a href="#">Table 5</a> .  |
| 12     | SETMAX            | Input (PD)          | Maximum delay set logic input. When SETMAX is set HIGH and SETMIN is set LOW, D[10:0] = 1111111111. When SETMAX is LOW, the delay is set by SETMIN or D[10:0]. Default is LOW when left floating. Single-ended LVPECL interface levels. See <a href="#">Table 5</a> . |
| 13     | V <sub>DD</sub>   | Power               | Positive supply pin.  |
| 14     | nCASCADE          | Output              | LVDS inverted output.   |
| 15     | CASCADE           | Output              | LVDS non-inverted output.   |
| 16     | nEN               | Input (PD)          | Single-ended control enable pin. When LOW, Q is delayed from IN. When HIGH, Q is a differential LOW. Default is LOW when left floating. Single-ended LVPECL interface levels. See <a href="#">Table 2</a> .   |
| 17     | F <sub>TUNE</sub> | Analog Input        | Fine tune delay control input. By varying the input voltage, it provides an additional delay.   |
| 18     | V <sub>DD</sub>   | Power               | Positive supply pin.  |
| 19     | V <sub>DD</sub>   | Power               | Positive supply pin.  |
| 20     | nQ                | Output              | Differential output pair. LVDS interface levels.  |
| 21     | Q                 | Output              | Differential output pair. LVDS interface levels.  |
| 22     | V <sub>DD</sub>   | Power               | Positive supply pin.  |
| 23     | D0                | Input (PD)          | Parallel data input D0. Single-ended LVCMOS, LVTTTL, LVPECL interface levels.   |
| 24     | GND               | Power               | Power supply ground.  |
| 25     | D1                | Input (PD)          | Parallel data input D1. Single-ended LVCMOS, LVTTTL, LVPECL interface levels.   |
| 26     | D2                | Input (PD)          | Parallel data input D2. Single-ended LVCMOS, LVTTTL, LVPECL interface levels.   |
| 27     | D3                | Input (PD)          | Parallel data input D3. Single-ended LVCMOS, LVTTTL, LVPECL interface levels.   |
| 28     | GND               | Power               | Power supply ground.  |
| 29     | D4                | Input (PD)          | Parallel data input D4. Single-ended LVCMOS, LVTTTL, LVPECL interface levels.   |
| 30     | D5                | Input (PD)          | Parallel data input D5. Single-ended LVCMOS, LVTTTL, LVPECL interface levels.   |
| 31     | D6                | Input (PD)          | Parallel data input D6. Single-ended LVCMOS, LVTTTL, LVPECL interface levels.   |
| 32     | D7                | Input (PD)          | Parallel data input D7. Single-ended LVCMOS, LVTTTL, LVPECL interface levels.   |

a. Pull-up (PU) and pull-down (PD) resistors are indicated in parentheses. *Pullup* and *Pulldown* refer to internal input resistors. See [Table 7, Pin Characteristics](#), for typical values.

Figure 3: Propagation Delay vs.  $F_{TUNE}$  Voltage Graph



## Function Tables

Table 2: Delay Enable

| nEN         | Q, nQ              |
|-------------|--------------------|
| 0 (default) | IN, nIN delayed    |
| 1           | Q = LOW, nQ = HIGH |

Table 3: Digital Control Latch

| LEN         | Latch Action         |
|-------------|----------------------|
| 0 (default) | Pass through D[10:0] |
| 1           | Latched D[10:0]      |

Table 4:  $V_{CF}$  Connection for D[10:0] Logic Interface

| Input    | $V_{CF}$ Connection | D[10:0] Logic Interface |
|----------|---------------------|-------------------------|
| $V_{CF}$ | $V_{EF}^{[a]}$      | LVPECL                  |
| $V_{CF}$ | No Connect          | LVC MOS                 |
| $V_{CF}$ | 1.5V source         | LVTTL                   |

a. Connect  $V_{CF}$  (pin 8) to  $V_{EF}$  (pin 7).

Table 5: Theoretical Delta Delay Values<sup>[a]</sup>

| D[9:0] Value | SETMIN | SETMAX | Programmable Delay <sup>[b]</sup> (ps) |
|--------------|--------|--------|--|
| XXXXXXXXXX   | H      | L      | 0                                      |
| 000000000    | L      | L      | 0 (default)                            |
| 000000001    | L      | L      | 10                                     |
| 000000010    | L      | L      | 20                                     |
| 000000011    | L      | L      | 30                                     |
| 000000100    | L      | L      | 40                                     |
| 000000101    | L      | L      | 50                                     |
| 000000110    | L      | L      | 60                                     |
| 000000111    | L      | L      | 70                                     |
| 000001000    | L      | L      | 80                                     |
| 0000010000   | L      | L      | 160                                    |
| 0000100000   | L      | L      | 320                                    |
| 0001000000   | L      | L      | 640                                    |
| 0010000000   | L      | L      | 1280                                   |
| 0100000000   | L      | L      | 2560                                   |
| 1000000000   | L      | L      | 5120                                   |
| 1111111111   | L      | L      | 10230                                  |
| XXXXXXXXXX   | L      | H      | 10240                                  |

a. Refer to [Table 13](#), *AC Characteristics*, for typical step delay values.

b. Inherent propagation delay not included.

Propagation delay = inherent propagation delay + programmable delay.

Inherent Propagation delay equals the propagation delay with the programmable delay = 0ps.

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8S89296 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 6: Absolute Maximum Ratings Table

| Item   | Rating                   |
|--|--------------------------|
| Supply voltage, $V_{DD}$                                     | 4.6V                     |
| Inputs, $V_I$  | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, $I_O$ (LVDS)<br>Continuous current<br>Surge current | 10mA<br>15mA             |
| Junction temperature, $T_J$                                  | 125°C                    |
| Storage temperature, $T_{STG}$                               | -65°C to 150°C           |

## DC Electrical Characteristics

Table 7: DC Input Characteristics

| Symbol         | Parameter                | Test Conditions | Minimum | Typical | Maximum | Units      |
|----------------|--------------------------|-----------------|---------|---------|---------|------------|
| $C_{IN}$       | Input capacitance        |                 |         | 2       |         | pF         |
| $R_{PULLUP}$   | Input pull-up resistor   |                 |         | 50      |         | k $\Omega$ |
| $R_{PULLDOWN}$ | Input pull-down resistor |                 |         | 50      |         | k $\Omega$ |

Table 8: Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

| Symbol   | Parameter               | Test Conditions           | Minimum | Typical | Maximum | Units |
|----------|-------------------------|---------------------------|---------|---------|---------|-------|
| $V_{DD}$ | Positive supply voltage |                           | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$ | Power supply current    | No load, maximum $V_{DD}$ |         |         | 158     | mA    |

Table 9: LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

| Symbol   | Parameter          | Test Conditions                        | Minimum | Typical | Maximum        | Units   |
|----------|--------------------|--|---------|---------|----------------|---------|
| $V_{IH}$ | Input high voltage |  | 1.7     |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input low voltage  |  | -0.3    |         | 0.7            | V       |
| $I_{IH}$ | Input high current | D[10:0] $V_{DD} = V_{IN} = 2.625V$     |         |         | 150            | $\mu A$ |
| $I_{IL}$ | Input low current  | D[10:0] $V_{DD} = 2.625V, V_{IN} = 0V$ | -10     |         |                | $\mu A$ |

Table 10: LVPECL Differential DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $GND = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ 

| Symbol    | Parameter                        |         | Test Conditions                | Minimum         | Typical         | Maximum         | Units   |
|-----------|----------------------------------|---------|--------------------------------|-----------------|-----------------|-----------------|---------|
| $I_{IH}$  | Input high current               | IN, nIN | $V_{DD} = V_{IN} = 2.625V$     |                 |                 | 150             | $\mu A$ |
| $I_{IL}$  | Input low current                | IN      | $V_{DD} = 2.625V, V_{IN} = 0V$ | -10             |                 |                 | $\mu A$ |
|           |                                  | nIN     | $V_{DD} = 2.625V, V_{IN} = 0V$ | -150            |                 |                 | $\mu A$ |
| $V_{PP}$  | Peak-to-peak voltage             |         |                                | 0.15            |                 | 1.3             | V       |
| $V_{CMR}$ | Common mode range <sup>[a]</sup> |         |                                | $GND + 0.95$    |                 | $V_{DD}$        | V       |
| $V_{BB}$  | Output voltage reference         |         | $I_{BB} = +150\mu A$           | $V_{DD} - 1.55$ | $V_{DD} - 1.35$ | $V_{DD} - 1.15$ | V       |
| $V_{EF}$  | Mode connection                  |         | $I_{EF} = +150\mu A$           | $V_{DD} - 1.55$ | $V_{DD} - 1.35$ | $V_{DD} - 1.15$ | V       |

a. Common mode input voltage is defined as  $V_{IH}$ .

 Table 11: LVPECL Single-Ended DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $GND = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ 

| Symbol   | Parameter                         |                                   | Test Conditions                | Minimum          | Typical | Maximum          | Units   |
|----------|-----------------------------------|-----------------------------------|--------------------------------|------------------|---------|------------------|---------|
| $V_{IH}$ | Input high voltage <sup>[a]</sup> | D[10:0], LEN, nEN, SETMIN, SETMAX |                                | $V_{DD} - 1.2$   |         | $V_{DD} - 0.940$ | V       |
| $V_{IL}$ | Input low voltage <sup>[a]</sup>  | D[10:0], LEN, nEN, SETMIN, SETMAX |                                | $V_{DD} - 1.870$ |         | $V_{DD} - 1.45$  | V       |
| $I_{IH}$ | Input high current                | D[10:0], LEN, nEN, SETMIN, SETMAX | $V_{DD} = V_{IN} = 2.625V$     |                  |         | 150              | $\mu A$ |
| $I_{IL}$ | Input low current                 | D[10:0], LEN, nEN, SETMIN, SETMAX | $V_{DD} = 2.625V, V_{IN} = 0V$ | -10              |         |                  | $\mu A$ |

a. To enable LVPECL interface levels on pins D[10:0], pin 7 must be connected to pin 8. See [Table 4](#).

 Table 12: LVDS DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ 

| Symbol          | Parameter                   | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| $V_{OD}$        | Differential output voltage |                 | 350     |         | 650     | mV    |
| $\Delta V_{OD}$ | $V_{OD}$ magnitude change   |                 |         |         | 50      | mV    |
| $V_{OS}$        | Offset voltage              |                 | 1.10    |         | 1.30    | V     |
| $\Delta V_{OS}$ | $V_{OS}$ magnitude change   |                 |         |         | 50      | mV    |

## AC Electrical Characteristics

Table 13: AC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ <sup>[a], [b]</sup>

| Symbol          | Parameter                             |                | Test Conditions             | Minimum | Typical  | Maximum | Units |
|-----------------|---------------------------------------|----------------|-----------------------------|---------|----------|---------|-------|
| $f_{OUT}$       | Output frequency                      | Q, nQ output   |                             |         |          | 800     | MHz   |
| $t_{PD}$        | Propagation delay                     | IN to Q, nQ    | Dx = 0                      | 1700    | 2200     | 2700    | ps    |
|                 |                                       | IN to Q, nQ    | Dx = 1023                   | 9500    | 12500    | 15000   | ps    |
|                 |                                       | nEN to Q, nQ   | Dx = 0                      | 1700    | 2400     | 3200    | ps    |
| $t_{PD\_RANGE}$ | Programmable propagation range        |                | $t_{PD\_MAX} - t_{PD\_MIN}$ | 8000    |          |         | ps    |
| $\Delta t$      | Step Delay                            |                | D0 = HIGH                   |         | 15       |         | ps    |
|                 |                                       |                | D1 = HIGH                   |         | 25       |         | ps    |
|                 |                                       |                | D2 = HIGH                   |         | 45       |         | ps    |
|                 |                                       |                | D3 = HIGH                   |         | 85       |         | ps    |
|                 |                                       |                | D4 = HIGH                   |         | 165      |         | ps    |
|                 |                                       |                | D5 = HIGH                   |         | 330      |         | ps    |
|                 |                                       |                | D6 = HIGH                   |         | 645      |         | ps    |
|                 |                                       |                | D7 = HIGH                   |         | 1270     |         | ps    |
|                 |                                       |                | D8 = HIGH                   |         | 2540     |         | ps    |
|                 |                                       |                | D9 = HIGH                   |         | 5075     |         | ps    |
|                 |                                       |                | D[9:0] = HIGH               |         | 10135    |         | ps    |
| INL             | Integral non-linearity <sup>[c]</sup> |                |                             |         | $\pm 10$ |         | ps    |
| $t_S$           | Setup time                            | D to LEN       |                             |         | -20      |         | ps    |
|                 |                                       | D to IN, nIN   |                             |         | -80      |         | ps    |
|                 |                                       | nEN to IN, IN  |                             |         | -35      |         | ps    |
| $t_H$           | Hold time                             | LEN to D       |                             |         | -175     |         | ps    |
|                 |                                       | IN, nIN to nEN |                             |         | -575     |         | ps    |
| $t_R$           | Release time                          | nEN to IN, nIN |                             |         | 250      |         | ps    |
|                 |                                       | SETMAX to LEN  |                             |         | 225      |         | ps    |
|                 |                                       | SETMIN to LEN  |                             |         | 240      |         | ps    |
| $t_R / t_F$     | Output rise/fall time                 | Q, nQ          | 20% to 80% at 100MHz        | 70      |          | 300     | ps    |
| odc             | Output duty cycle                     |                |                             | 40      |          | 60      | %     |

a. Characterized up to  $f_{OUT} = 800MHz$  unless noted otherwise.

b. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

c. Deviation from a linear delay (actual Min. to Max.) in the 1024 programmable steps.



## Applications Information

### Recommendations for Unused Input Pins

Inputs:

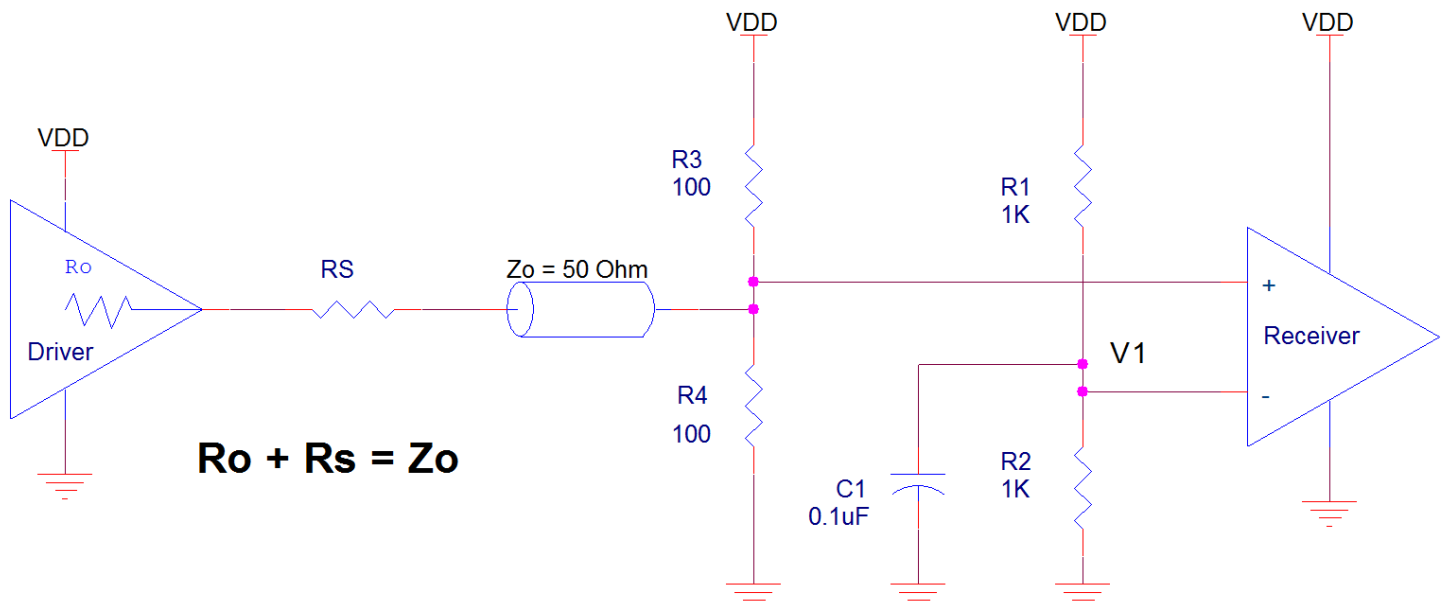
#### LVC MOS Control Pins

All control pins have internal pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Wiring the Differential Input to Accept Single-Ended Levels

Figure 4 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{DD} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_{REF}$  at 1.25V. The values below are for when both the single ended swing and  $V_{DD}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVC MOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVC MOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than -0.3V and  $V_{IH}$  cannot be more than  $V_{DD} + 0.3V$ . Suggest edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

Figure 4: Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



## 2.5V LVPECL Clock Input Interface

The IN/nIN accepts LVPECL, LVDS, CML and other differential signals. Both differential signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figure 5 to Figure 9* show interface examples for the IN/nIN input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

Figure 5. IN/nIN Input Driven by a CML Driver

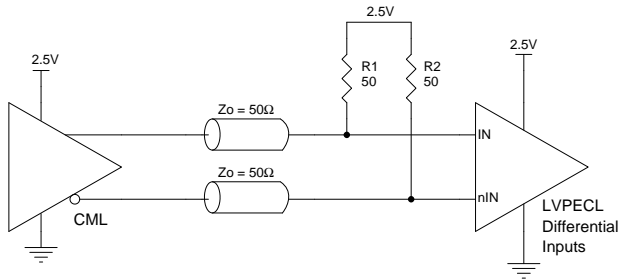


Figure 6. ON/nIN Input Driven by a 2.5V LVPECL Driver

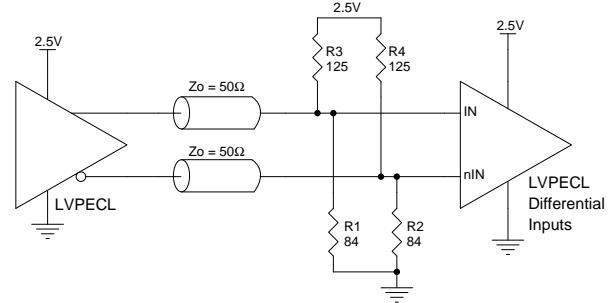


Figure 7. IN/nIN Input Driven by a 2.5V LVDS Driver

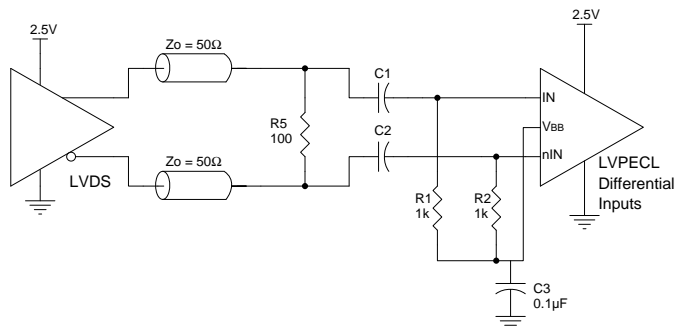


Figure 8. IN/nIN Input Driven by a Built-In Pullup CML Driver

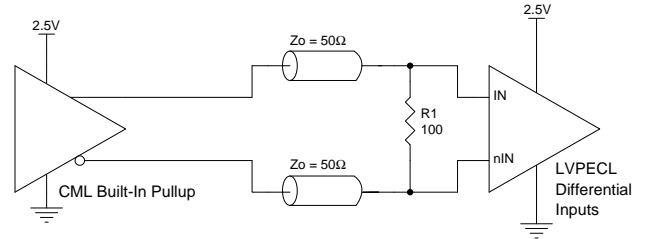
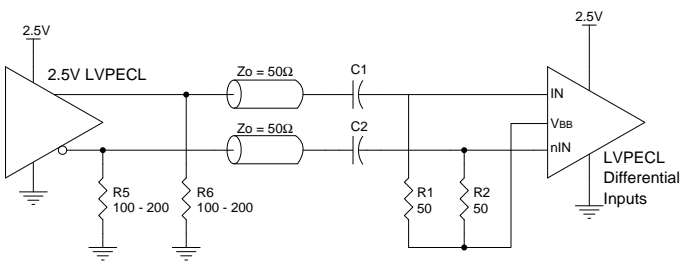


Figure 9. IN/nIN Input Driven by a 2.5V LVPECL Driver with AC Couple

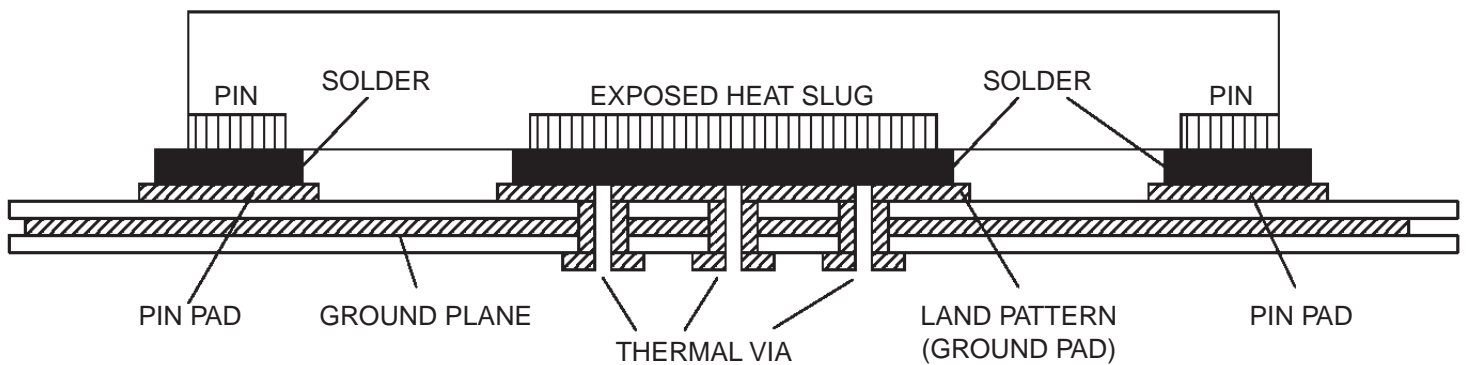


## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in [Figure 10](#). The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead-frame Base Package, Amkor Technology.

Figure 10: P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)



## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between  $90\Omega$  and  $132\Omega$ . The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a  $100\Omega$  parallel resistor at the receiver and a  $100\Omega$  differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in [Figure 11](#) can be used with either type of output structure. [Figure 12](#), which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately  $50\text{pF}$ . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 11: Standard LVDS Termination

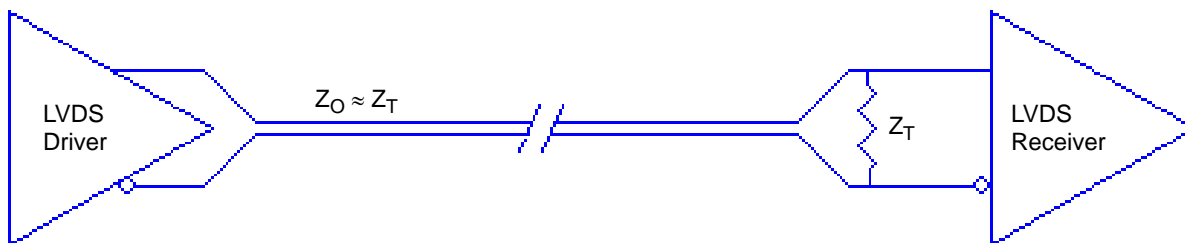
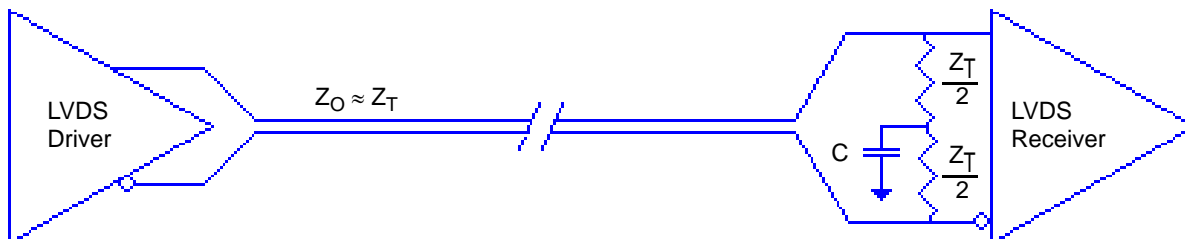


Figure 12: Optional LVDS Termination



## Power Considerations

This section provides information on power dissipation and junction temperature for the 8S89296. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 8S89296 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 2.5V + 0.125V = 2.625V$ , which gives worst case results.

The maximum current at  $-40^{\circ}C$  is as follows:

$$I_{DD\_MAX} = 158mA$$

- $Power_{MAX} = V_{DD\_MAX} * I_{DD\_MAX} = 2.625V * 158mA = 415mW$

The maximum current at  $85^{\circ}C$  is as follows:

$$I_{DD\_MAX} = 150mA$$

$$Power_{MAX} = V_{DD\_MAX} * I_{DD\_MAX} = 2.625V * 150mA = 394mW$$

### 2. Junction Temperature.

Junction temperature,  $T_J$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is  $125^{\circ}C$ . Limiting the internal transistor junction temperature,  $T_J$ , to  $125^{\circ}C$  ensures that the bond wire and bond pad temperature remains below  $125^{\circ}C$ .

The equation for  $T_J$  is as follows:  $T_J = \theta_{JA} * Pd_{total} + T_A$

$T_J$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is  $39.5^{\circ}C/W$  per [Table 14](#) below.

Therefore,  $T_J$  for an ambient temperature of  $85^{\circ}C$  with all outputs switching is:

$$85^{\circ}C + 0.394W * 39.5^{\circ}C/W = 100.6^{\circ}C. \text{ This is below the limit of } 125^{\circ}C.$$

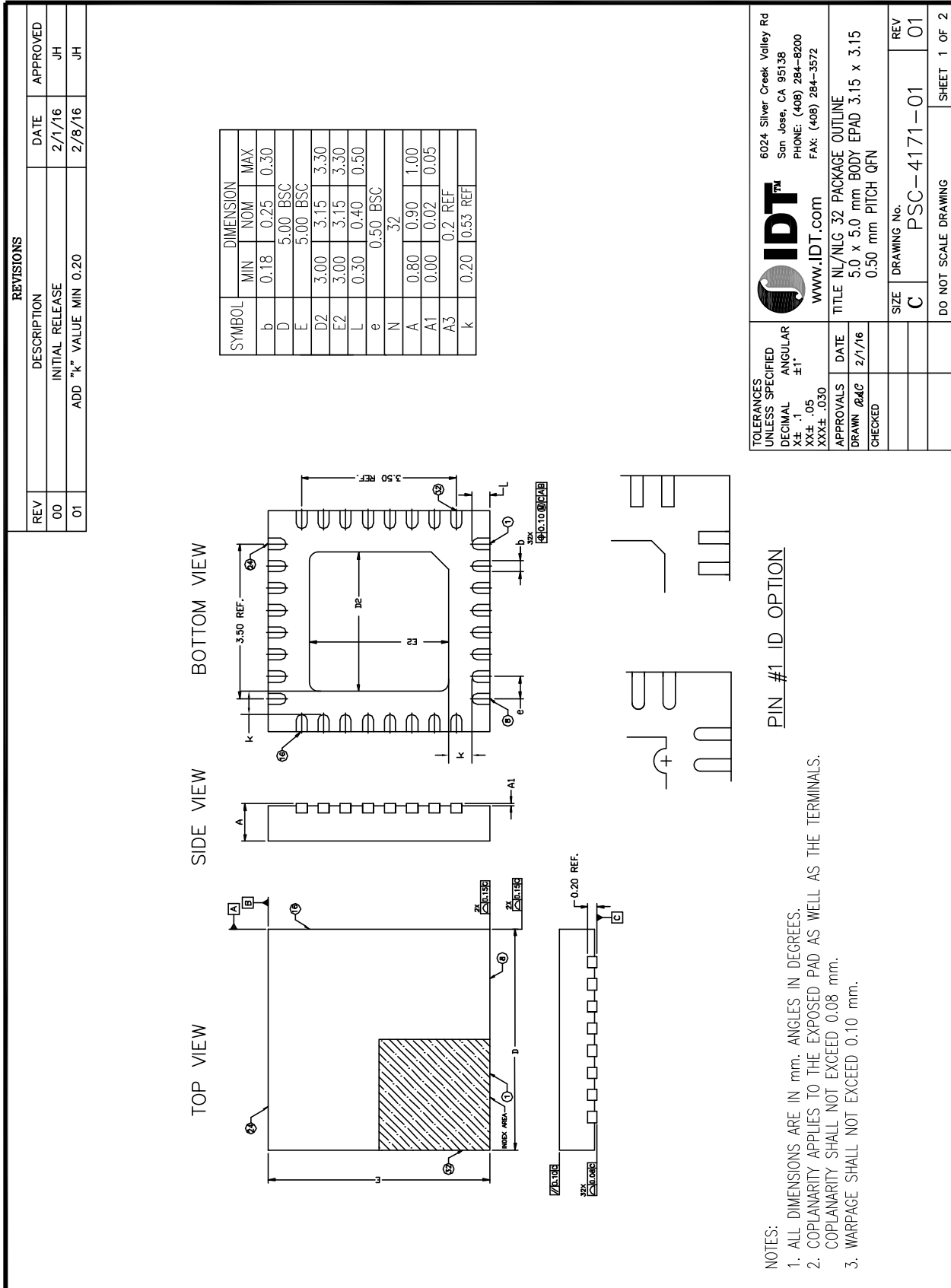
This calculation is only an example.  $T_J$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 14: Thermal Resistance  $\theta_{JA}$  for 32 Lead VFQFN, Forced Convection

| $\theta_{JA}$ by Velocity                   |                   |                   |                   |
|---|-------------------|-------------------|-------------------|
| Meters per Second                           | 0                 | 1                 | 2.5               |
| Multi-Layer PCB, JEDEC Standard Test Boards | $39.5^{\circ}C/W$ | $34.5^{\circ}C/W$ | $31.0^{\circ}C/W$ |

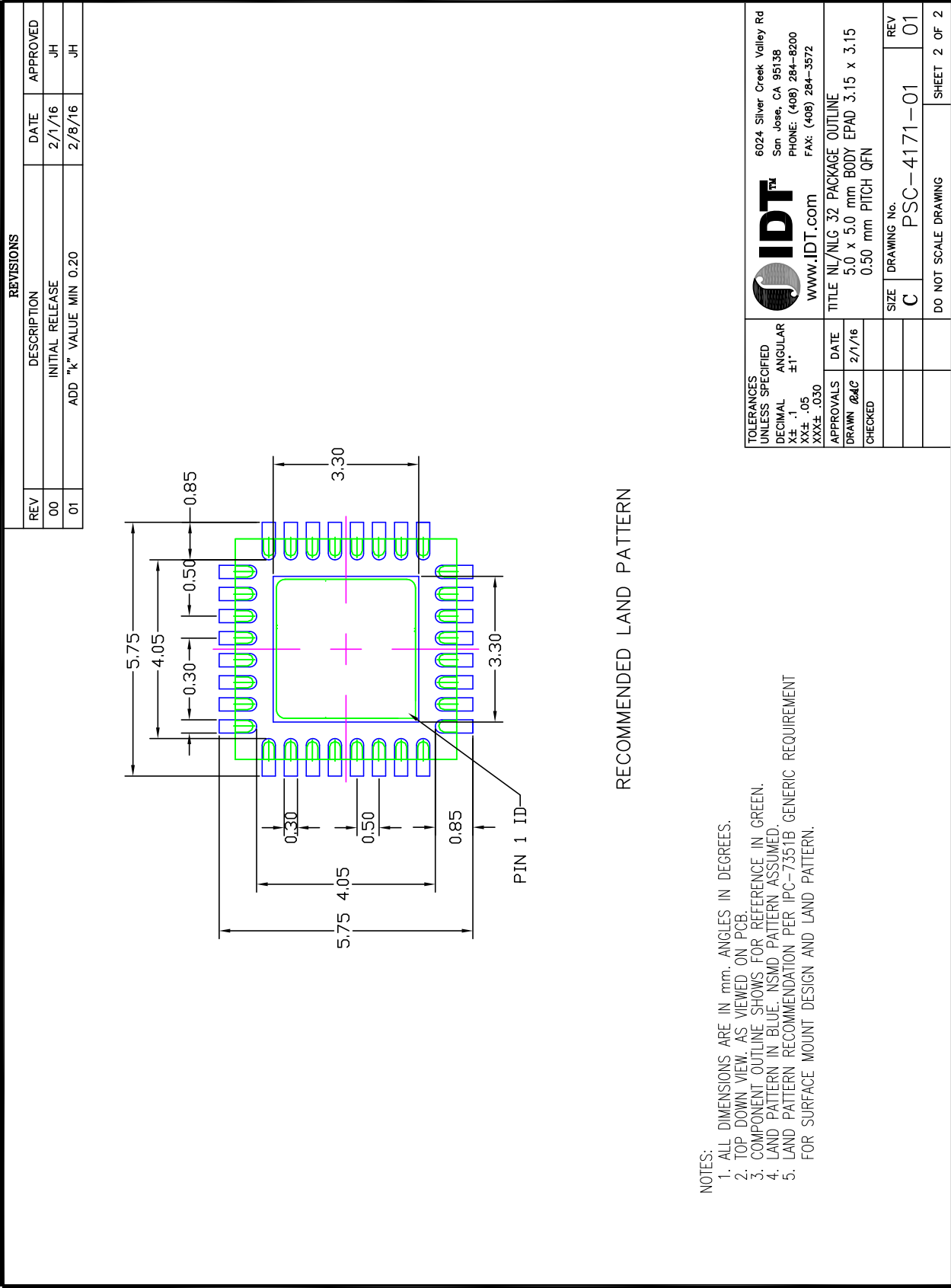
# Package Outline and Package Dimensions

Figure 13: 32-Lead VFQFN Package

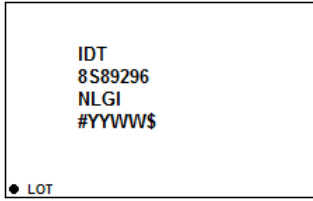


Package Outline and Package Dimensions, continued

Figure 14: 32-Lead VFQFN Package



## Marking Diagram



1. Line 1 IDT is the part number prefix.
2. Line 2 is the part number.
3. Line 3 is the package code.
4. Line 4:
  - # denotes stepping.
  - "YWW" is the last digit of the year and week that the part was assembled.
  - "\$" denotes mark code.

## Ordering Information

| Part/Order Number | Marking        | Package                  | Shipping Packaging | Temperature    |
|-------------------|----------------|--------------------------|--------------------|----------------|
| 8S89296NLGI       | IDT8S89296NLGI | 32 Lead VFQFN, lead-free | Tray               | -40°C to +85°C |
| 8S89296NLGI8      | IDT8S89296NLGI | 32 Lead VFQFN, lead-free | Tape & Reel        | -40°C to +85°C |

## Revision History

| Revision Date     | Description of Change |
|-------------------|-----------------------|
| February 14, 2017 | Initial datasheet.    |



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